GLASSY – ELECTRET FERROELECTRIC RANDOM ACCESS MEMORY (GERAM)

by

Vasileia Georgiou

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DEDICATION

This dissertation is dedicated to my loving husband, Christoforos, for his support, his patience, and his faith in me. Because he is the reason I did not give up. I am truly thankful for having you in my life.

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LIST OF ABBREVIATIONS

Glass transition temperature ..... T_g
Ferroelectric field effect transistor ..... FeFET
Complementary metal–oxide–semiconductor ..... CMOS
Metal–Oxide–Semiconductor Field-Effect Transistor ..... MOSFET
Random Access Memory ..... RAM
Static Random Access Memory ..... SRAM
Dynamic Random Access Memory ..... DRAM
Resistive RAM ..... RRAM
Conductive Filament ..... CF
Low Resistance State ..... LRS
High Resistance State ..... HRS
Spin Torque Transfer Magnetic Random Access Memory ..... STT-MRAM
Magnetic Tunnel Junction ..... MTJ
Magnetic Random Access Memory ..... MRAM
Phase Change Random Access Memory ..... PCRAM
Ferroelectric Random Access Memory ..... FeRAM
Ferroelectric Field Effect Transistor ..... FeFET
Alternating Current ..... AC
1 Capacitor-1 Resistor 1C-1T
Ferroelectric ..... FE
Polyvinylidene Fluoride ..... PVDF
Glassy-polymer electret Random Access Memory ..... GeRAM
Langley Research Center-Colorless Polyimide 1 ..... LaRC-CP1
Polyimide ..... PI
N-methyl-2-pyrrolidone ..... NMP
Characteristic frequency ..... f_c
Atomic Force Microscope ..... AFM
Laboratory Virtual Instrument Engineering Workbench ..... LabVIEW
Secondary Ion Mass Spectrometry ..... SIMS
Scattered Electron Mecroscopy ..... SEM
Focused Ion Beam ..... FIB
Organic Field Effect Transistor ..... OFET
Flat band ..... FB
Flat band voltage shift ..... ΔV_{FB}
Drain current – gate voltage ..... I_d-V_g
Clockwise ..... CW

Counter-clockwise ..... CCW
Melting temperature ..... T_m
Triangular Voltage Sweeps ..... TVS
Self-heating Effect ..... SHE

ABSTRACT

GLASSY – ELECTRET FERROELECTRIC RANDOM ACCESS MEMORY (GERAM)

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Ferroelectric memory devices based on polar polymers are currently the focus of multiple studies. In these devices, the program/erase of memory involves the physical rotation of dipoles by an applied electric field. In the common approach, to obtain fast programming speed the operating temperature needs to be well above the polymer glass transition temperature (T_g) because at temperatures below T_g the dipoles are locked in place. However, fast programming achieved this way means the dipole are easy to rotate, leading to a short retention time.

In this dissertation, we demonstrate a radically new ferroelectric memory device concept based on polar polymers with T_g well above operation temperature. To achieve fast programming, we momentarily elevate the local temperature to well above T_g while applying a programming electric field. At the normal operation temperature, well below T_g, the dipoles are locked in their position. Neither depolarization field nor READ

operation can disturb the memory state. This dual-condition programming (temperature and electric field) with long retention time is demonstrated using a thin-film ferroelectric field effect transistor (FeFET) with LaRC-CP1 polyimide ($T_g \approx 265\ ^oC$) gate dielectric (≈15 nm) and a doped polysilicon (≈15 nm) channel. Retention of the memory states with different programming conditions is studied. This new promising memory technology can lead to a universal memory with arbitrary number of memory states that exhibit extremely long retention times and are immune to depolarization fields, while using low cost processing materials that are CMOS compatible and highly scalable.

CHAPTER ONE INTRODUCTION

In the present information years, there is an enormous amount of information that is generated and requires being stored. With the use of mobile device, such as smartphone, cameras and tablets, in our everyday life this amount of date that needs to be stored and retrieved fast is continuously increasing making memory elements one of the most essential and challenging components of the electronic circuits. It is thus apparent the need for memory cells which consume as less power as possible, can write and retrieve data fast, have the maximum memory cells in a unit area, exhibit good reliability, while the production cost is kept sufficiently low. So far, the density growth, speed, and the cost reduction of memory have been enabled by scaling the underlying technologies to ever-smaller feature sizes and therefore smaller memory-bit sizes. However, this scaling is starting approaching the limitations of storage physics.[1][2] While it is agreed that the memory technologies are still scalable, those limitations will soon be reached.

The currently dominant solid state memory technologies store data as a charge state. These technologies are: (1) Static Random Access Memory (SRAM), (2) Dynamic Random Access Memory (DRAM), and (3) Flash memory. Each of them exhibits some great characteristics that need to be inherited in the future memory technologies. However, their reliability becomes questionable as their physical limitations are

approached. Thus, a number of new memory technologies based on different memory mechanisms have been proposed and investigated in order to overcome those limitations.

In this introductory chapter, the characteristics of the leading memory technologies, as well as the most promising evolving ones, are introduced.

1.1 SRAM

SRAM is a volatile memory, retaining the stored information for as long as power is supplied, and is usually employed as an on-chip cache. Figure 1.1 illustrates a typical SRAM cell; it stores data in flip-flops consisting of four to six transistors. The flip-flops may be in either of two states that correspond to a 1 or a 0. SRAM is fastest among the dominant memory technologies (GHz operation speed), does not require frequent refreshing, has great endurance, and can be directly incorporated on a logic chip. However, it has a large layout footprint leading to a higher cost per bit, and the standby power consumption becomes problematic when the transistors are scaled down, resulting to high leakage currents.

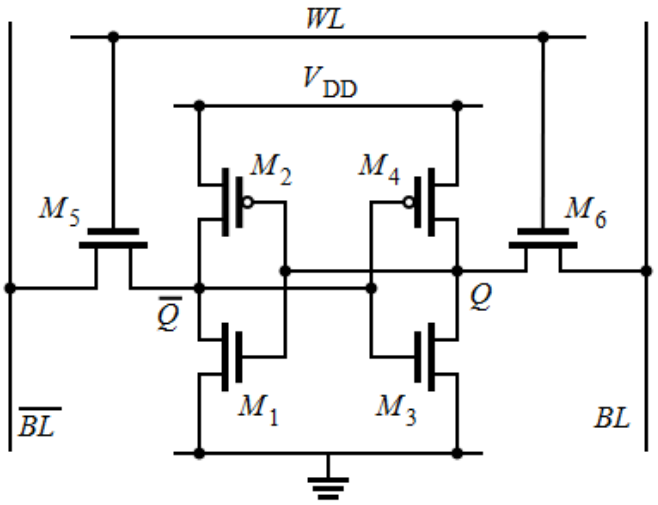

Figure 1.1: SRAM memory cell

1.2 DRAM

DRAM is a volatile memory, but it needs to be periodically refreshed to hold the data as long as power is applied. This refresh results in relatively high power consumption for maintaining the memory state. DRAM is the most common memory for main code and data storage, since its invention in 1966.[3] Figure 1.2 represents the basic DRAM memory cell; it consists of one address transistor and one capacitor, where the information is held. It is obvious that DRAM has a smaller foot-print than that of the SRAM, resulting in a lower cost per bit. It is actually the memory with the best scalability among the current dominant ones, and at a reasonable cost. However, apart from the mentioned higher power consumption, the conventional DRAM fabrication process is not compatible with the standard CMOS logic.

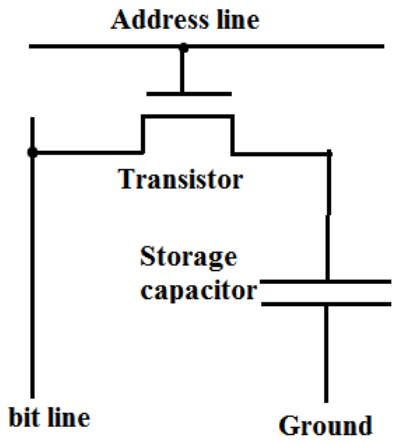

Figure 1.2: DRAM memory cell

1.3 Flash Memory

Flash memory is a dense memory technology, making it a cheap storage media. Its main advantage is the fact that it is non-volatile, meaning that the information is retained without the need of a refresh and with no power supply required; data is stored in an array of memory cells made from floating-gate transistors (Figure 1.3). NAND Flash memory is mainly used in mobile devices, such as smartphones, digital cameras, and mobile music players. Write operation is a relatively slow process for the Flash memory and also consumes a lot of power. Another disadvantage of the Flash memory is the high operating voltages and the short endurance.

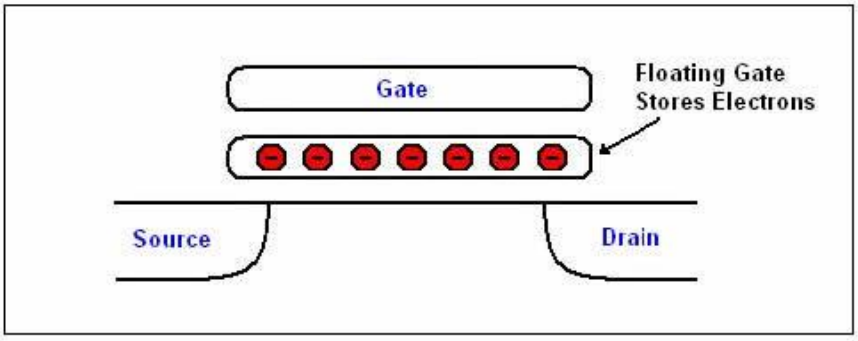

Figure 1.3: Flash memory floating cell

1.4 Emerging Memory Technologies

In order to overcome the physical limitations of the current memories, an extensive research and development of new types of memory technologies that are based on different storage mechanisms has been conducted in the last two decades.[4][5][6][7] There has been proposed a number of new memory technologies in order to replace one or more of the currently dominant ones, trying to combine the speed of SRAM, the density of DRAM, and the non-volatility of Flash memory at a reasonable and competitive integration cost. However, it is difficult to satisfy the requirements for a universal memory (low operating voltages and power consumption, high write and read speed, good scalability, non-volatility and high endurance). Among all these proposed emerging memory technologies, only a couple is rather promising and is presented in the following pages.

1.4.1 Resistive RAM

The Resistive RAM (RRAM) cell is a capacitor-like device that consists of an insulator layer sandwiched between two metallic electrodes, and information is stored as

two or more resistance states of the memory device.[8] The insulator layers commonly used in RRAM are the metal oxides and perovskite oxides. The change in the resistance of the device usually is either filament-based or interface-based and it is induced by thermal, chemical or electronic mechanisms. In case of the filament-based RRAM, a conductive filament (CF) is either formed or ruptured. Figure 1.4 shows the structure of an RRAM cell, as well as the created CF (formed, causing a low resistance state (LRS), and ruptured, causing a high resistance state (HRS)). This CF is generally believed to be formed by localized oxygen vacancies. The conduction is due to electron hoping between these vacancies due to a redox reaction in the oxide layer under a voltage bias. Electronic carriers, mobile ions or ionic defects contribute to the current transport in the case of the interface-based RRAM. RRAM is a typical example of unipolar switching. Even though RRAM exhibits high operation speeds, low power consumption, operates at low voltages, and it is highly scalable and easy to fabricate, the conducting mechanisms are yet to be fully understood, and the fabrication cost is excessively high, making the technology not very competitive.

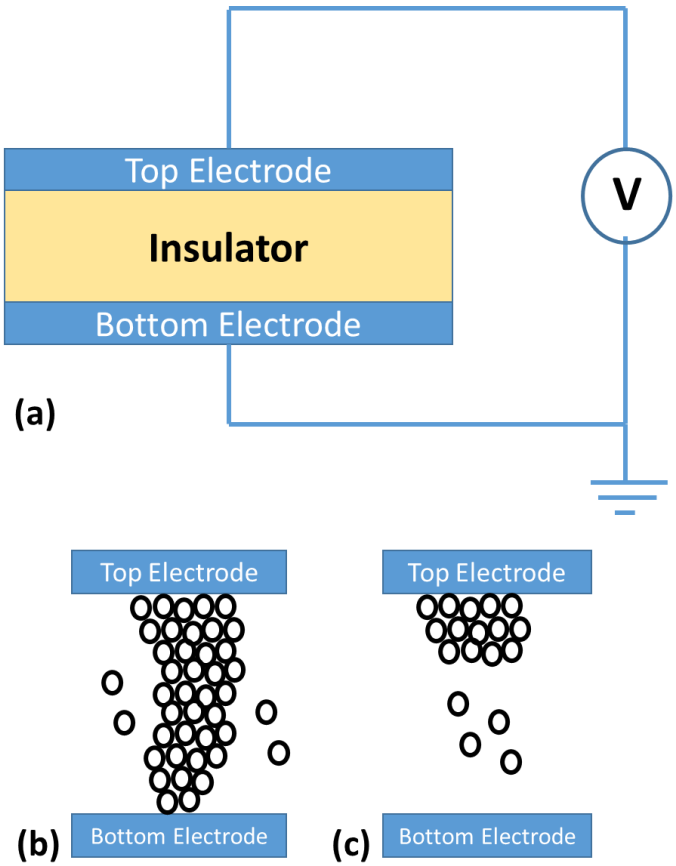

Figure 1.4: (a) RRAM cell schematic, (b) LRS, and (c) HRS.

1.4.2 Magnetic RAM

Spin Torque Transfer Magnetic RAM (STT-MRAM) memory cell's basic element is a magnetic tunneling junction (MTJ), which actually is two thin films of altering ferromagnetic materials and an ultra-thin tunneling dielectric sandwiched between them (Figure 1.5). One of the ferromagnetic layers has a pinned magnetization, while the magnetization of other one is allowed to be flipped. While in conventional MRAM this unpinned layer can acquire one of the equally probable polarizations depending on the application of an external magnetic field, in case of the STT-MRAM,

this external field is not required. Switching between the two possible states is performed by running a spin-polarized current through the MTJ.[9] The resistance of the junction has a low resistance, related to high tunneling probability, when the magnetization of the two ferromagnetic layers exhibits the same polarity, whereas it becomes higher when the polarity is opposite. Thus, information in this technology is represented by the angular spin momentum, not by the electron charge. STT-MRAM exhibits great endurance, good scalability and read and write operations are symmetrically fast. The programming current correctly scales with the device size and the thermal stability is properly maintained. However, the amount of current needed to reorient the magnetization is at present too high for most commercial applications, making the technology an unrealistic alternative.

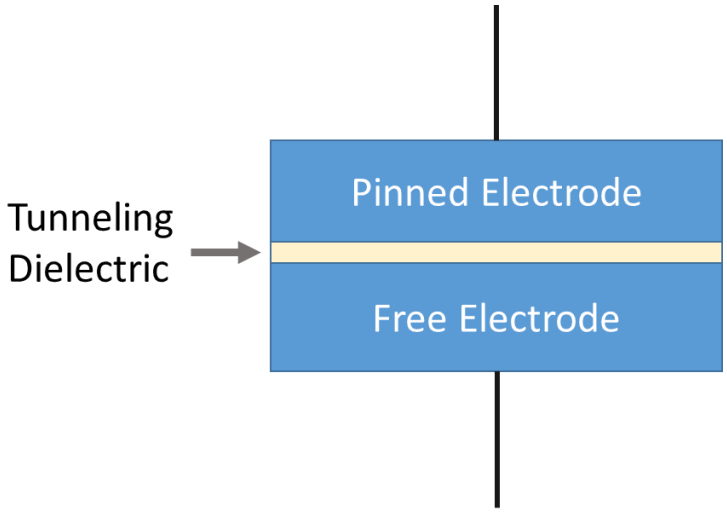

Figure 1.5: Schematic of the MTJ in a STT-MRAM.

1.4.3 Phase Change RAM

Phase Change RAM (PCRAM) is a kind of resistive non-volatile memory, typically based on chalcogenide alloy materials and the resistance difference between an amorphous (high-resistivity) and a crystalline (low resistivity) phase as shown in Figure 1.6. The difference in resistance between the crystalline and the amorphous state is typically five orders of magnitude.[10] The reversible change in the resistance is performed by heating the device using a current pulse leading to Joule heating in a significant portion of the cell above its crystallization temperature. The duration of this pulse depends on the crystallization speed of the phase change material and dictates the write speed of the memory technology. In order to switch to the amorphous state, a larger current pulse is applied and then abruptly removed to melt and quench the material. In order to sense the device's state, a very low power pulse is applied across the device and the corresponding current is monitored. Though the developed PCRAM is fast, non-volatile, exhibits good scalability, and uses low operating voltages, it exhibits a long-term resistance and threshold voltage drift, which translates in low memory endurance.

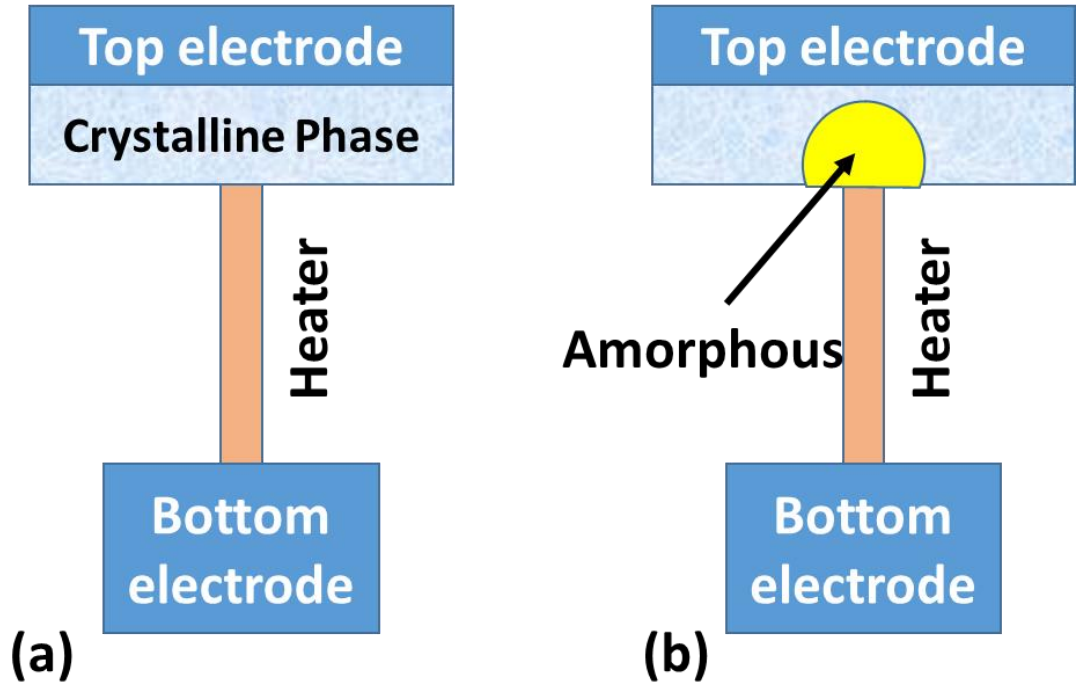

Figure 1.6: Cross-section of two PRAM memory cells: a) cell is in low resistance crystalline state, b) cell in high resistance amorphous state.

1.4.4 Ferroelectric RAM

Ferroelectric RAM (FeRAM) is the focus of the present dissertation. It stores information as the spontaneous polarization of the ferroelectric material, which is caused by a sufficiently strong applied electric field.[11] Actually, it is the position of atoms within the material structure that is stored. FeRAM is realized by either a capacitor with the ferroelectric material (organic or inorganic) sandwiched between two metallic electrodes (in fact it consists of the ferroelectric capacitor and an access transistor), or a ferroelectric field effect transistor (FeFET) with the ferroelectric material incorporated in the gate dielectric stack. These two configurations of the FeRAM are shown in Figure 1.7. This memory technology has the potential to be fast, have a great endurance and

retention, is highly scalable, while the production cost is kept low and exhibits a large range of operating temperatures. All these promising characteristics of FeRAM make it qualify as a potential universal memory.

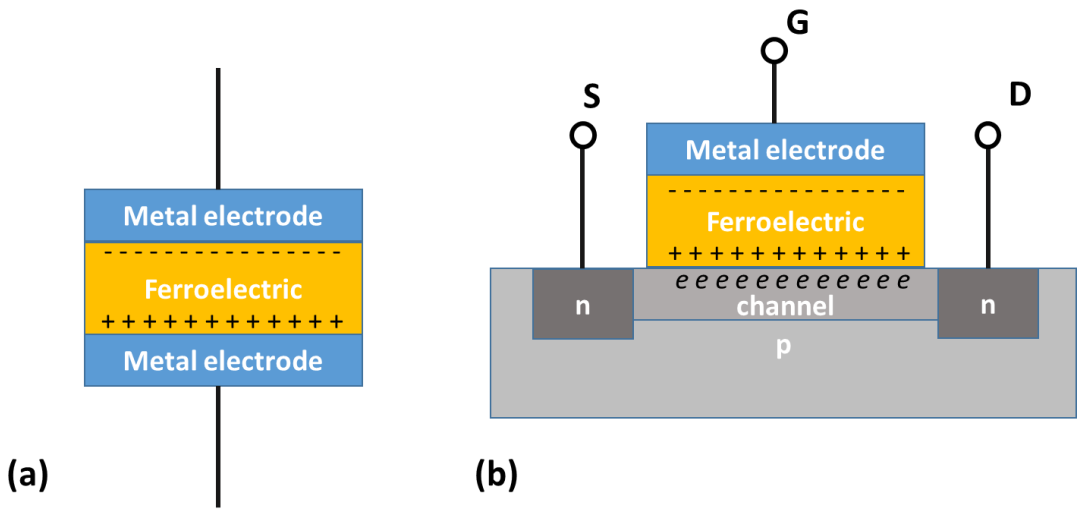

Figure 1.7: (a) Ferroelectric Capacitor, and (b) Ferroelectric Transistor.

1.5 Dissertation Overview

This dissertation focuses on overcoming the main drawbacks of the state of the art ferroelectric memory based on polar polymeric dielectrics. A new concept of ferroelectric memory that utilizes polar polymers with T_g well above the operating temperature is introduced. This proposed new approach is investigated and is shown how it can lead to a *real* non-volatile memory technology which exhibits low power dissipation and allows arbitrary programming states.

Following the introduction chapter, Chapter 2 presents the characteristics of the state of the art ferroelectric memory technologies, while pointing their main

disadvantages. Chapter 3 introduces the new ferroelectric memory concept that incorporates a polar polymer with high T_g in the gate dielectric stack. Chapter 4 presents and further explores the properties, such as T_g and characteristic frequencies, for the specific polyimide used in this dissertation. Chapter 5 focuses on the fabrication process of the FeFET memory cells made for demonstration of the proposed memory concept. Chapter 6 describes in details the efficient annealing of the fabricated FeFET devices at or even below T_g. Chapter 7 explores the mechanisms that can confound the proof of the ferroelectric effect, and presents a simple methodology to distinguish ferroelectricity among the other parasitic mechanisms. Chapter 8 demonstrates the novel ferroelectric memory technology proposed in this dissertation, while findings of Chapter 6 and 7 are used to prove the presence of the ferroelectric effect and its memory characteristics. Finally, a summary of the dissertation and a discussion for future research is presented in Chapter 9.

CHAPTER TWO FERROELECTRIC RANDOM ACCESS MEMORY (FERAM)

Ferroelectricity is a property of certain materials that exhibit spontaneous electric polarization. This polarization can be reversed by the application of an external electric field. The term of ferroelectricity is used in analogy to ferromagnetism, in which the materials exhibit a permanent magnetic moment. In Ferroelectric Memory (FeRAM) data is stored as a dielectric polarization state.

Ferroelectric Memory (FeRAM) has been known since 1950s, when MIT alumna scholar Dudley Allen Buck proposed this memory technology in his master's thesis "Ferroelectrics for Digital Information Storage and Switching", published 1952.[12] However, research groups started the development of FeRAM in 1980's. Currently, FeRAM is being used in production and is being embedded into chips using CMOS technology, but it is not as widely used as more established technologies like DRAM, SRAM and NAND-Flash.

2.1 Dielectric Polarization

A dielectric material is an electric insulator that can be polarized by an applied electric field. When the dielectric is placed in an electric field, electric charges shift from their equilibrium positions and cause a dielectric polarization, which creates an internal electric field that reduces the overall field inside the dielectric.

Let first introduce the electric susceptibility χ_e of a dielectric material which is a measure of how easily it can be polarized in response to an applied electric field ($\boldsymbol{E}$). This, in turn, determines the electric permittivity of the material and thus influences many other phenomena in that medium, such as the capacitance of capacitors. The susceptibility of a medium is related to its relative permittivity ε_r by

$$\chi_e = \varepsilon_r - 1.$$

The dielectric polarization density $\boldsymbol{P}$ is given by the formula:

$$\boldsymbol{P} = \varepsilon_0 \chi_e \boldsymbol{E},$$

where ε_0 is the electric permittivity of free space. Consequently, the electric displacement $\boldsymbol{D}$ is related to the polarization density P by

$$\boldsymbol{D} = \boldsymbol{P} + \varepsilon_0 \boldsymbol{E} = \varepsilon_0 \varepsilon_r \boldsymbol{E}$$

The polarization of the materials arises from four different effects. The *Electronic* polarization originates from the displacement of the electrons in an atom relative to the nucleus it surrounds. In the case of the *Atomic* polarization, the nucleus of the atom reorients due to the applied field. This type of polarization is usually small compared to the *Electronic* one. The *Ionic* polarization is caused by relative displacements between positive and negative ions in ionic crystals. At last, but not least, the *Dipole* polarization is a polarization caused by the alignment of the permanent and induced dipoles to the external applied electric field. The local viscosity of the material effects the time the dipoles need to rotate and relax, while the thermal noise disturbs the alignment of the dipoles. This makes the dipole polarization to heavily depend on temperature and chemical surroundings.

In most dielectric materials, the induced polarization is proportional to the applied electric field (linear relationship). In some specific materials that are called paraelectric, the slope of the polarization versus the applied external electric field, is not constant as in dielectrics but it is a function of the applied electric field. In case of ferroelectric materials, the mentioned slope is not linear and polarization exists even in the absence of the externally applied electric field, unlike in case of the dielectric and paraelectric materials. The spontaneous polarization in these materials can be reversed by the application of a sufficiently strong applied electric field with the opposite direction. This means that the polarization depends not only on the applied electric field, but also on its history, resulting in a hysteresis loop.

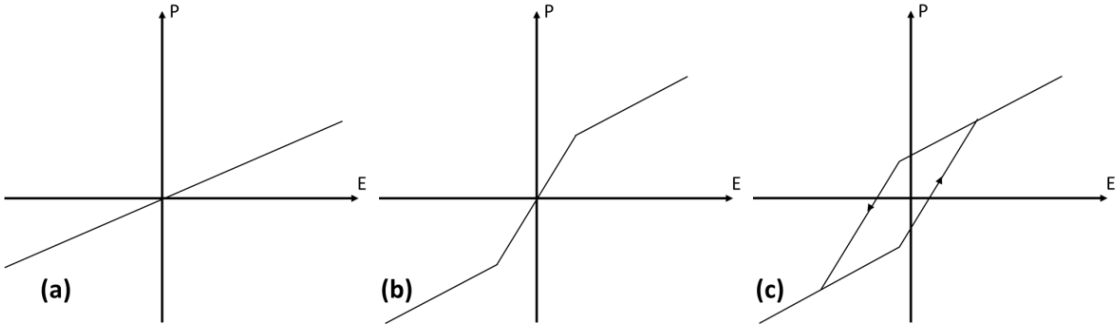

Figure 2.1: Polarization (P) versus applied electric field (E) in a (a) dielectric, (b) paraelectric, and (c) ferroelectric material

2.2.1 Dielectric Spectroscopy

Dielectric Spectroscopy is a powerful tool for the electrical and dielectric characterization of non-conducting or semiconducting single crystal, polycrystalline, and amorphous materials. It measures the dielectric permittivity of a medium as a function of

frequency. It actually expresses the response of the electric dipole moment of the material to the external field, as permittivity.

The complex dielectric permittivity relative to vacuum is given by equation (2.1):

$$\varepsilon^*(\omega) = \varepsilon'(\omega) - i\varepsilon''(\omega) \quad (2.1)$$

The complex permittivity ε*(ω) spectra is easily evaluated from the sample impedance, Z*(ω), with the help of sample dimensions. Impedance is the opposition to the flow of the alternating current (AC) in a complex system. A complex electrical system consists of both elements, resistor that acts as energy dissipater and capacitor that stores energy.

When characterizing a dielectric film sandwiched between two electrodes, the equivalent circuit is not just a capacitor element, but a resistor ($R_p = 1/G$) in parallel with a capacitor (C_p) as shown below can be used.

Figure 2.2: Dielectric capacitor and equivalent circuit.

In general, for a capacitor with area of electrode plates A, and dielectric film thickness t, the capacitance value (C_p) is equal to the vacuum capacitance (C_0) with the same dimensions multiplied with the relative permittivity of the dielectric material (ε_r).

$C_p = \varepsilon_r C_0$ (2.2), where $C_0 = \varepsilon_0 \frac{A}{t}$ (2.3), and ε_0 is the dielectric constant of vacuum.

The admittance of the circuit is given by $Y = \frac{I}{V}^{\lfloor\theta} = G + j\omega C_p$ (2.4), where I is the total current through the sample, V is the potential difference across the sample, θ is the angle between $\vec{I}$, and $\vec{V}$.

From equation (3.4), we can extract:

$Y = j\omega C_0 \left(\frac{C_p}{C_0} - j\frac{G}{\omega C_0}\right)$ (2.5).

Comparing (2.2) and (2.5), we can get the complex permittivity

$\varepsilon_r^* = \frac{C_p}{C_0} - j\frac{G}{\omega C_0}$ (2.6), where the real and the imaginary (or loss) part are given by:

$\varepsilon'_r = \frac{C_p}{C_0} = \frac{tC_p}{A\varepsilon_0}$ (2.7), and $\varepsilon''_r = \frac{G}{\omega C_0} = \frac{t}{\omega R_p A\varepsilon_0}$ (2.8).

The real part of the complex permittivity, ε', is related to the energy stored reversible in the material, while the imaginary part, ε", is the proportional to the energy which is dissipated per cycle (energy loss). Figure 2.3 presents the dielectric spectroscopy response of a material.

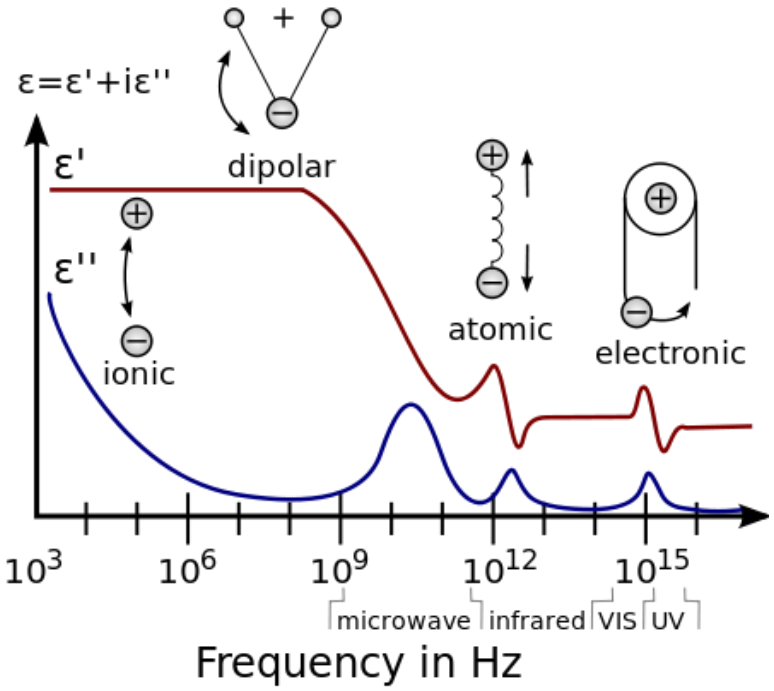

Figure 2.3: Dielectric permittivity spectrum

There are a number of different dielectric mechanisms, connected to the way a medium reacts to the applied field. Each dielectric mechanism is exhibits a characteristic frequency, which is the reciprocal of the characteristic time of the process. The most common of these dielectric mechanisms are the ionic, dipolar, atomic and electronic.

Ionic relaxation is the result of the movement of electric charges in the medium due to an applied alternating field. It mainly dominates at low frequencies and introduces only losses to the system. The charge carriers are trapped at interfaces of heterogeneous systems, and this leads to a separation of charges. The charges may be separated by a considerable distance and therefore make contributions to the dielectric loss that are orders of magnitude larger than the response due to molecular fluctuations.

The dipolar relaxation originates from permanent and induced dipoles aligning to an applied electric field. The time needed for dipoles to relax (so the characteristic frequency) is determined by the local viscosity, which makes dipole relaxation heavily dependent on temperature, pressure and chemical surrounding.

Atomic polarization is observed when the nucleus of the atom reorients in response to the electric field. This is a resonant, not a relaxation, process, and it is intrinsic to the nature of the atom.

The electronic mechanism is a resonant process that refers to the electron density and occurs in a neutral atom when the electron density relative to the atomic nuclei it surrounds is displaced due to the applied electric field.

At the characteristic frequency of each mechanism, the real part of the complex dielectric permittivity exhibits a drop, while the imaginary part exhibits a peak. This is actually the frequency of the ac applied electric field that the mechanism can no longer completely respond. In case of atomic and dipolar mechanisms, it highly depends on the temperature of the measurements, since temperature affects the medium viscosity and, consequently, the speed the charge carries and dipoles move.

To be complete a dielectric experiment can also be carried out keeping the frequency fixed while sweeping the temperature.

2.2.1.1 Dielectric Spectroscopy Measurements for Ferroelectric Polymers

In the frequency domain, at a given temperature, the output of the dielectric spectroscopy measurements should look like Figure 2.4, where one characteristic (or

corner) frequency, f_c, appears. As we described in the previous section, f_c is the frequency of the applied external ac field at which the medium cannot respond. In case of polar polymers, the dipole rotation to align and satisfy the applied filed is the response. At low frequencies (how low depends on the temperature), the dipoles can rotate faster than the alternating applied field, and thus they can completely follow it. This results in a constant ε' (as long as dipoles can completely follow the field, the medium response to frequency does not change) and a low ε" since there is low resistance to the field. As the frequency increases approaching f_c, the dipoles cannot rotate as fast as the field alternates, meaning that they can partially follow it, and this is when the transition in ε' and the peak in ε" appear, the sign of the relaxation process. The drop in ε' indicates that the response to the field changed/got reduced and the peak in ε" is due to domain vibrations, meaning that there was loss introduced in the system.

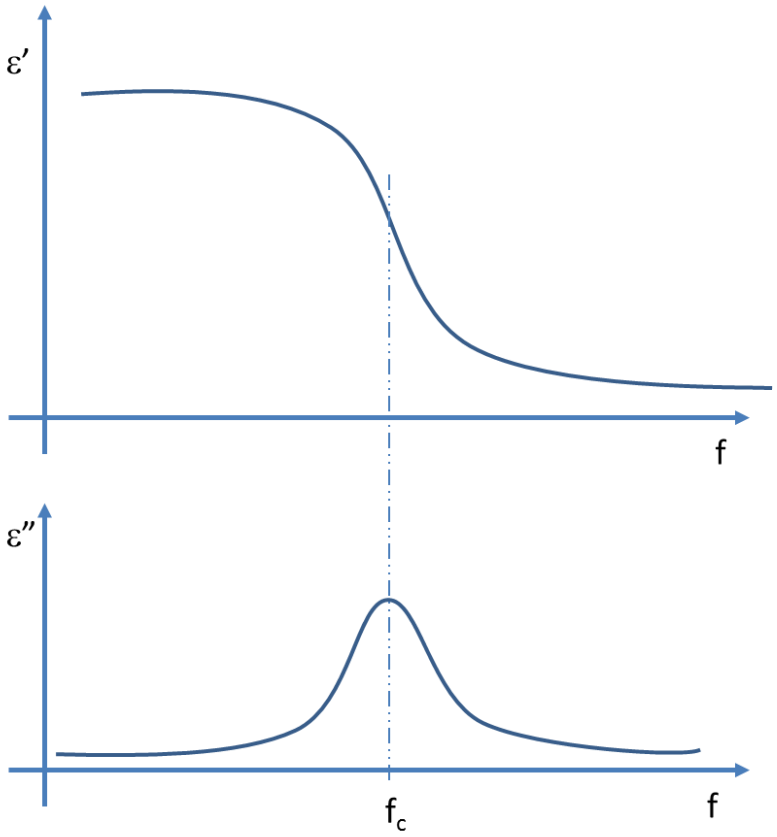

Figure 2.4: Dielectric Spectroscopy Measurements, frequency spectrum

2.2.1.2 Operation of an Impedance Analyzer

The most standard methods of measuring a system impedance is by using an automated or semi-automated Impedance Analyzer. This class of ac analyzer operates with a so-called auto-balance bridge (Figure 2.5). A signal is applied to the unknown impedance of the sample under test (Z_x), an operational amplifier effectively constrains all the current flowing through this impedance (I_x) to flow through the range resistor (R_r) of the setup, presenting a virtual ground at the device terminal marked as "low" (I_r is equal to I_x). [13]

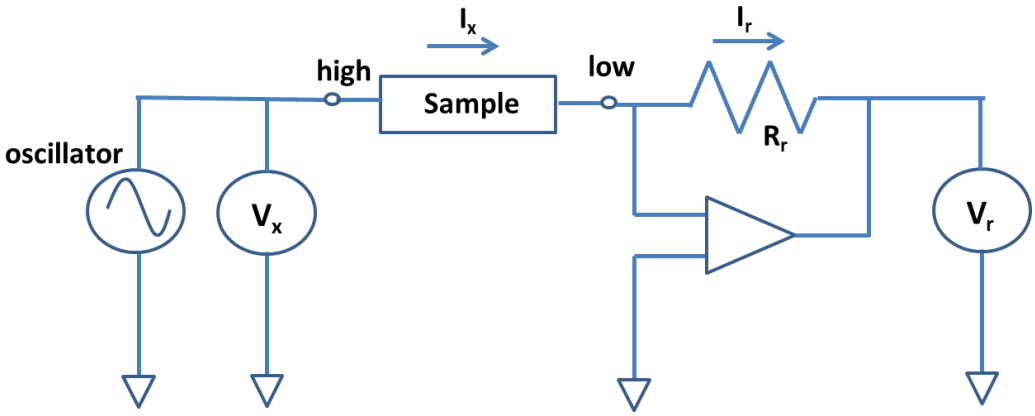

Figure 2.5: Principle of auto-balance bridge.

For this circuit, the impedance can be obtained as $Z_x = \frac{V_x}{I_x} = R_r \frac{V_x}{V_r}$ (2.9).

The vector voltages V_x and V_r are measured with the vector voltmeters. Since the value of R_r is known, the complex impedance Z_x of the sample can be calculated by using equation (2.9). The range resistor (R_r) is the key circuit element, which determines the impedance measurement range.

After acquiring Z_x in form of G and C_p (of Figure 2.2) from the parameter analyzer, ε' and ε" can be subtracted from equations (2.7) and (2.8) respectively.

2.3 FeRAM configurations

In this section the different configurations of the FeRAM are discussed. As we mentioned in the previous chapter, the ferroelectric memory configuration can either be a ferroelectric capacitor, or a (Ferroelectric Field Effect Transistor) FeFET. These configurations, as well as their advantages and drawbacks are introduced.

2.3.1 Ferroelectric Capacitors

In case of a ferroelectric capacitor, the ferroelectric material, organic or inorganic, is sandwiched between two metallic electrodes (Figure 2.6). By applying a sufficiently large bias, the ferroelectric layer is polarized in one of two possible states. The ferroelectric effect is observed through the resulting hysteresis loop of polarization (total charge stored on the plates of the capacitors per unit area) as a function of the applied voltage across the capacitor. The commonly used method to read the memory state is by the detection of the polarization reversal current. The device is driven to one of the two states (one of the two opposite polarizations of the dipoles), and the resulting current is detected. This current depends on the initial memory state. Depending on whether the polarization was initially aligned or not with the direction of the applied field, a low or a high charge displacement current response is observed. If the directions of the internal polarization and the applied field were opposite, readout changed the polarization state and the displacement current is high. It is clear at this point that the readout technique for the ferroelectric capacitor memory element is destructive, since every time that information is needed to be read, the device is forced at the same state (regardless the initial one) to sense displacement current. Thus, each read operations should be followed by a rewrite operation to return the cell to its initial state, leading to higher operating power consumption and longer sensing times. Moreover, this configuration consists essentially by a one capacitor to store the information, and one transistor for the word line (1C – 1T), occupying a significant amount of valuable layout area. Fatigue, the decrease of the remanent polarization with cycling, and retention, the loss of stored polarization over time are some more of the additional drawbacks of this configuration, which

compensate for the easy fabrication process, the main advantage of this memory configuration.

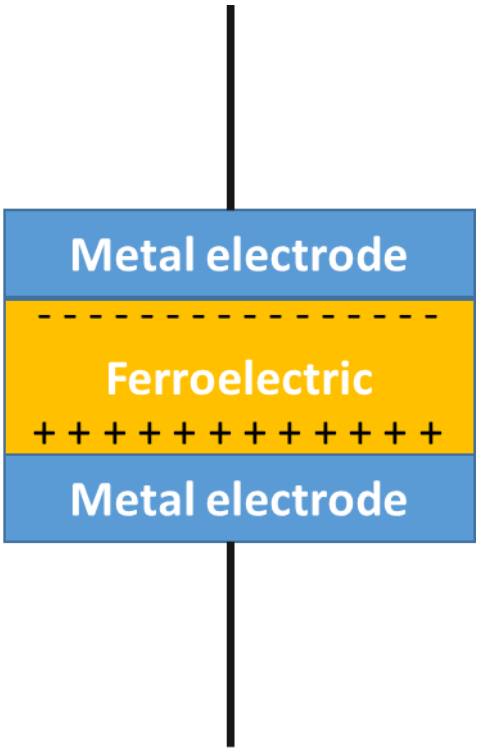

Figure 2.6: Ferroelectric capacitor memory cell.

2.3.2 Ferroelectric Field Effect Transistors (FeFETs)

The device is essentially a conventional FET in which the usual gate insulator is replaced with a ferroelectric insulating layer (Figure 2.7). Sometimes another dielectric layer is inserted between the semiconductor and the ferroelectric to improve the interface and reduce gate leakage current. Switching from one polarization state to the other is performed by applying a sufficiently large gate bias. The conductivity of the FET channel is determined partially by the remnant polarization formed in the ferroelectric layer

following the application of a gate voltage sufficient to exceed the coercive voltage of the ferroelectric layer. Thus, the read operation is performed by reading the device drain current, which is a non-destructive operation.

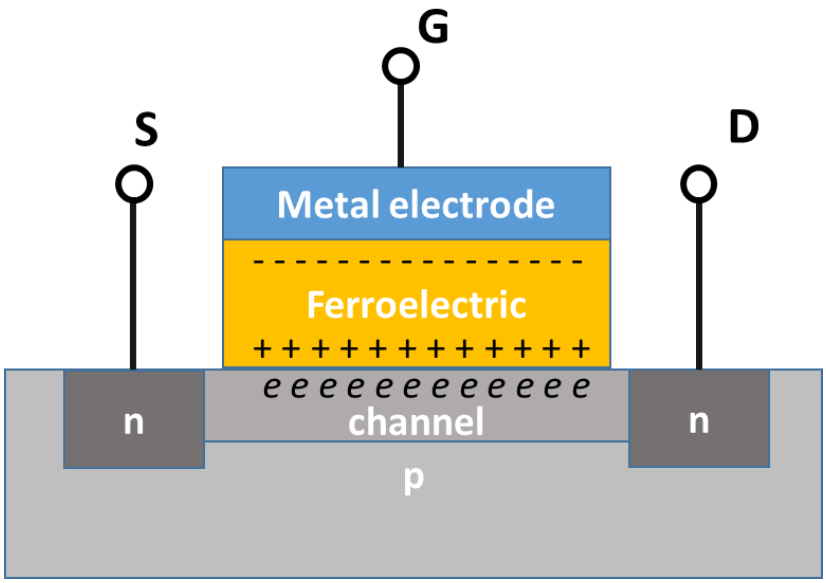

Figure 2.7: FeFET memory cell configuration.

This configuration exhibits two main advantages over the capacitor configuration, which are the non-destructive read operation along with the smaller layout footprint, since only one transistor device is required in this case. However, this memory cell exhibits the drawback of retention of just a few days, much shorter than the expected.[14] The factors that shorten the retention times are the presence of depolarization field and the gate leakage current.

The inherent depolarization field exists due to the incomplete charge compensation (not enough free carriers available) at the interface of the semiconducting

transistor channel. The gate stack can be simulated as the ferroelectric capacitance (C_F) in series with the semiconductor capacitance (C_{IF}) as shown in Figure 2.8.

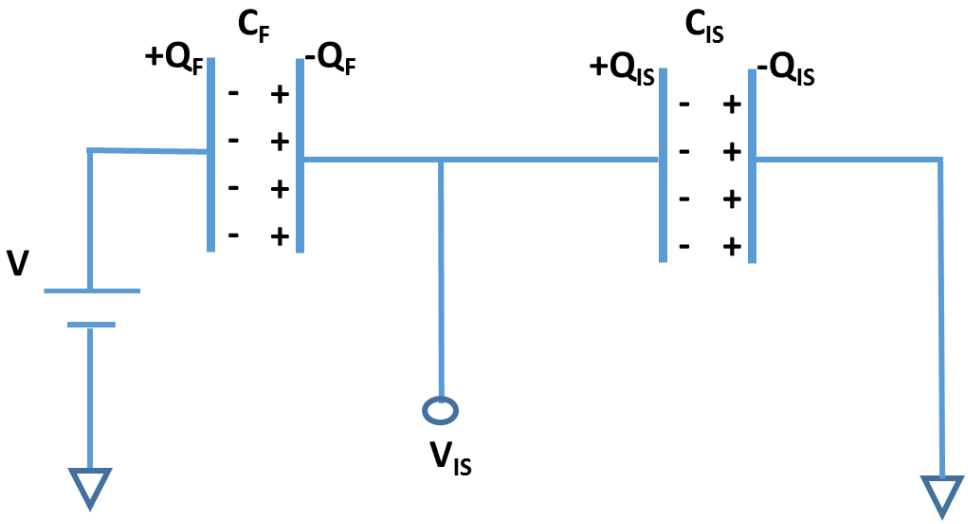

Figure 2.8: Gate stack represented of the FeFET transistor as a ferroelectric capacitance (C_F) in series with the semiconductor capacitance (C_{IS}).

A gate voltage V is applied across the gate dielectric stack, and it introduces a polarization (P) and a voltage (V_F) across the ferroelectric layer:

$$V_F = C_{IS}\frac{V}{C_F + C_{IS}} - \frac{P}{C_F + C_{IS}}$$

When there is a zero bias applied across the gate:

$$V = V_F + V_{IS} = 0 \Rightarrow$$

$$\frac{Q_F - P}{C_F} + \frac{Q_{IS}}{C_{IS}} = 0 \Rightarrow$$

$Q_F = \frac{PC_{IS}}{C_{IS}+C_F}$, which concludes to a depolarization field:

$$E_{dp} = -\frac{P}{\varepsilon}\frac{C_F}{C_F + C_{IS}}$$

This indicates that a larger C_{IS} leads to a smaller depolarization field.

As we mentioned above, apart from the intrinsic depolarization field, the leakage current and charge trapping in the gate dielectric stack reduces the memory retention time too. The field that is induced in the dielectric field due to ferroelectric polarization attracts electron from the gate electrode, as well as the semiconductor side. This charge injection is followed by trapping in the gate dielectric stack which leads to local charge compensation and gradually diminishes the polarization effect. The leakage current and charge trapping can be reduced by the introduction of thick buffer layers at both interfaces of the dielectric (gate and semiconductor side), however, this will eventually increase the depolarization field, which leads to reduced retention time too.

2.4 Ferroelectric Memory based on Polar Polymers

Ferroelectricity is known to be a property of crystal materials. The majority of applicable and well-studied inorganic FE materials belong to the perovskite oxide ferroelectrics, where the ion displacement in their crystal structure is responsible for their ferroelectric behavior. A typical inorganic perovskite is $BaTiO_3$, which crystal structure is shown in Figure 2.9.

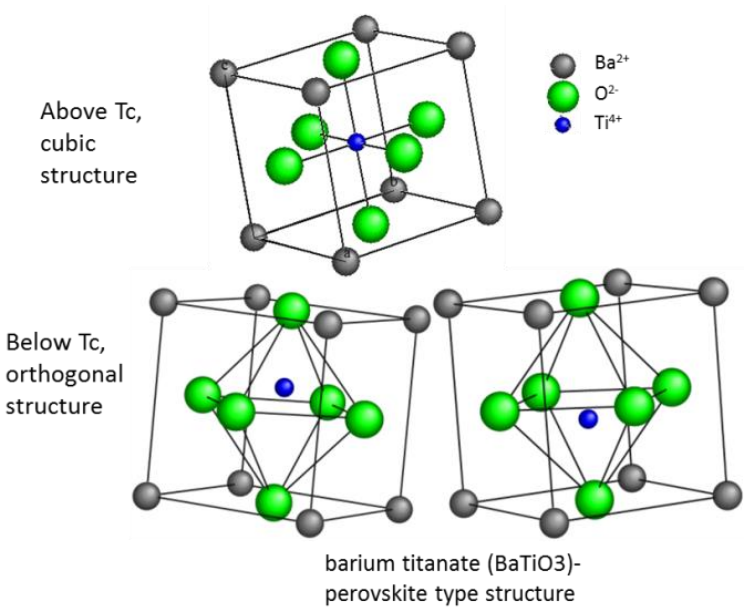

Figure 2.9: $BaTiO_3$ crystal structure, and the ion displacement.

In the cubic form, all the Ba^{2+} ions occupy eight corners of an elementary cubic cell, whereas single Ti^{4+} ion is in the center of the cube and the O^{2-} ions in the center of each surface of that cube. However, below the Curie temperature ($T_{C)}$) $BaTiO_3$ exists in a distorted tetragonal structure with a displacement of the centers of positive and negative charges within the sub-lattice.

In the case of the distorted tetragonal structure, polarization occurs as a result of the unit shift of axially elongated Ti^{4+} ion crystal. This is a "spontaneous polarization", since it occurs without applying an external electric field or pressure, and it is the origin of the material's ferroelectric behavior.

However, researchers have worked not only with inorganic FE materials but also with FE polymers. Ferroelectricity in polymers is due to rigid rotation, where a branch of the chain or even the backbone rotates to align with the externally applied electric field.

PVDF is the most well-known and studied FE polymer, its two most common conformations are shown Figure 2.10.

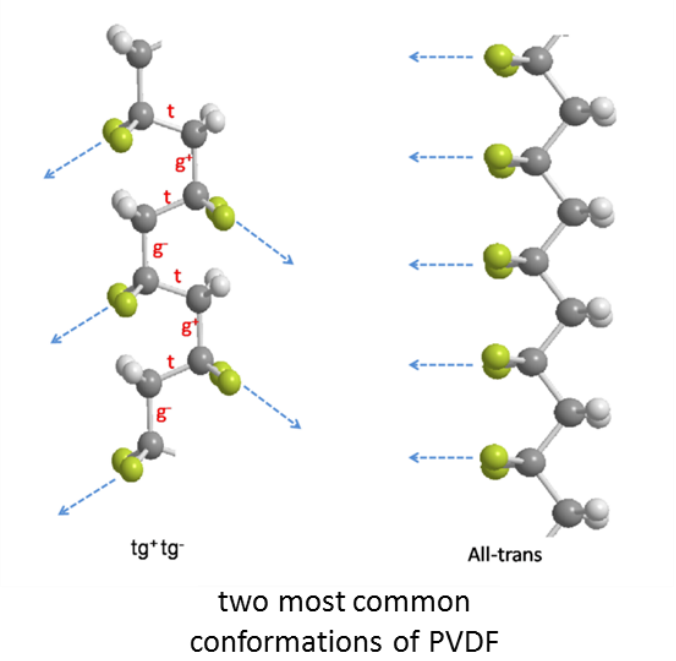

Figure 2.10: PVDF chain structure.

In the $tg^{+}tg^{-}$ conformation, the inclination of dipoles to the chain axis leads to the polar components of both perpendicular and parallel to the chain. However, in the all-trans structure, the alignment of all its dipoles is in the same direction normal to the chain axis. In this way, it can be expected that the all-trans is the most highly polar conformation in PVDF (the polar phase with a large spontaneous polarization). These polar conformations are the crucial factors that lead to the ferroelectric properties.

2.4.1 Advantages of Ferroelectric Polymers

To begin with, the high processing temperatures used for the deposition (metal-organic chemical vapor deposition process) and/or the crystallization of the inorganic ferroelectric materials are particularly problematic given that normally the ferroelectric films have to be integrated on a chip with several other electronic elements.

Furthermore, as the size of the devices scales down, the ferroelectric film used has to be thinner too. As we already mentioned, ferroelectric inorganic materials are crystal materials and since using single crystalline films is not practical, the polycrystalline ferroelectric films used must have an average grain size much smaller than the device size. While in the case of ferroelectric polymers, the material is amorphous or semi-crystalline, allowing thin films with reliable devices.

Moreover, organic materials are extremely desirable in current device technologies, since they allow the realization of flexible electronic circuits. The materials used in flexible circuit construction must work reliably and in harmony with the rest of the elements integrated in the flexible circuit to assure ease of manufacture and reliability.

Finally, since the polarization switching in the ferroelectric polymeric materials is due to the rigid rotation of the polymer's chain, the device endurance is expected to be much longer than that of an inorganic material device where the switching is due to an abrupt ion displacement.

To summarize, organic ferroelectric memory devices have potentially better scalability, endurance, allow fabrication process that is CMOS compatible, and can be applied in emerging technology applications such as flexible electronics.

2.4.2 Glass Transition Temperature

At low temperatures, due to their amorphous section, all polymers exhibit a glassy (vitreous) state, meaning that they assume the characteristics of glasses, including hardness, stiffness, brittleness, and transparency. Thermal energy is required for segments of a polymer chain to move with respect to one another. While the temperature rises, the polymer obtains sufficiently high thermal energy that allows segments of its chain to move, acquiring a rubbery (viscoelastic) behavior, like a viscous liquid. The temperature at which this transition happens is called glass transition temperature (T_g), and the transition is a relaxation transition. This means T_g depends on the effective frequency of the measurement. The importance of this temperature point is based on the fact that at this point the polymer material undergoes a marked change in properties, such as specific volume, refractive index, dielectric constant and loss, and density, change. It is worthy to mention here that this is typically not a specific temperature, but a temperature range.

Since space charge polarization involved migration and reorientation of charge carriers, it is significant only above T_g. Dipole polarization in polymeric materials can also be observed below T_g, if the polymers have flexible polar side chains that contribute to dipolar polarization. In polymers in which polar side group is rigidly attached to the main chain, dipolar orientation is possible only in case of cooperative motion of the main chain segments.

Now that we have introduced T_g, we can discuss the dielectric spectroscopy measurements in case the frequency of the applied field is kept constant while we sweep

the operating temperature of the material, a representation of the resulting real and imaginary part of the dielectric constant versus temperature plot is shown in Figure 2.11. While the temperature is low, well below T_g, the dipoles are locked in their position and cannot rotate to align with the applied field. In this case, the real part of the complex permittivity is almost constant and really low since no dipoles can follow the field. At the same time, since nothing moves, there is no energy loss, so the imaginary part stays low too. While approaching T_g, segments of the polymer chain can move, and the dipoles rotate and align with the field. Thus, ε' that describes the degree at which the medium responds to the field, starts increasing exponentially, and at temperatures well above T_g, where the dipoles can freely rotate, it saturates. As for ε", it starts increasing along with ε' since the dipoles rotate but they find resistance – as the medium has not yet completely exited the glassy state. Consequently, it reached a maximum at T_g, when it enters the viscous-liquid state, and then drops again, while it increases again as the dipoles environment starts interact (e.g. vibrations) and reaches a second peak when dipoles move freely.

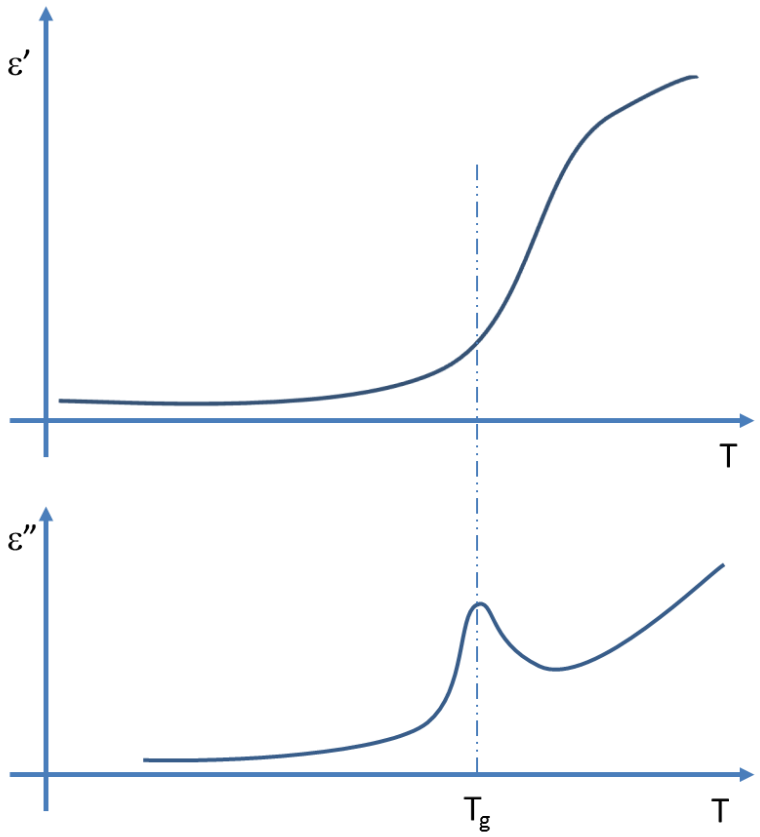

Figure 2.11: Dielectric Spectroscopy Measurements, temperature spectrum

Since the increase in temperature, leads to easer movement of the segments of the polymer chain (so the rotation of the polymer dipoles), the characteristic frequency, f_c mentioned in Figure 2.4, also depends on the polymer temperature. To be more specific, f_c increases with the rise of the temperature.

CHAPTER THREE GLASSY-POLYMER ELECTRET RANDOM ACCESS MEMORY (GERAM)

Polymer memory devices have attracted extensive attention [15],[16],[17],[18],[19],[20] due to easy processing, low cost, flexibility, scalability, and easily tailored properties. More specifically, ferroelectric field effect transistors (FeFETs) incorporating a polar polymer film in the gate dielectric stack have attracted significant research interest as ferroelectric random access memory (FeRAM) elements.[15],[21] While FeRAM, organic or otherwise, is designed to be non-volatile, the reported memory retention time of polymer-based FeRAM is not much longer than a few days.[14],[15],[21],[22],[23] This is significantly shorter than what is needed for an efficient nonvolatile memory. The main causes that reduce the retention time are mentioned in section 2.3.2, and they are depolarization fields, leakage current through the polymeric dielectric,[14] and mobile ions. Mobile ions are a material purity/fabrication issue and therefore not intrinsic, and can easily be avoided during processing. The leakage current may be reduced by inserting additional buffer layers in the gate dielectric stack and/or careful choice of the operation voltage range through device optimization. However, the depolarization field is the result of incomplete charge compensation in the semiconducting substrate that forms the transistor channel and is therefore a universal intrinsic problem,[14] which tends to get worse in the presence of interfacial layers added to suppress the gate leakage.

Moreover, one has to consider that a memory cell is not a stand-alone device, but it belongs in a memory array (Figure 3.1). This means that when a specific cell is accessed in order to write/erase or read the stored data, there is bias applied to neighboring cells that are connected on the same word or bit line. Thus, every time a memory cell is accessed the state of the neighboring cells is disturbed and eventually their retention time is reduced.

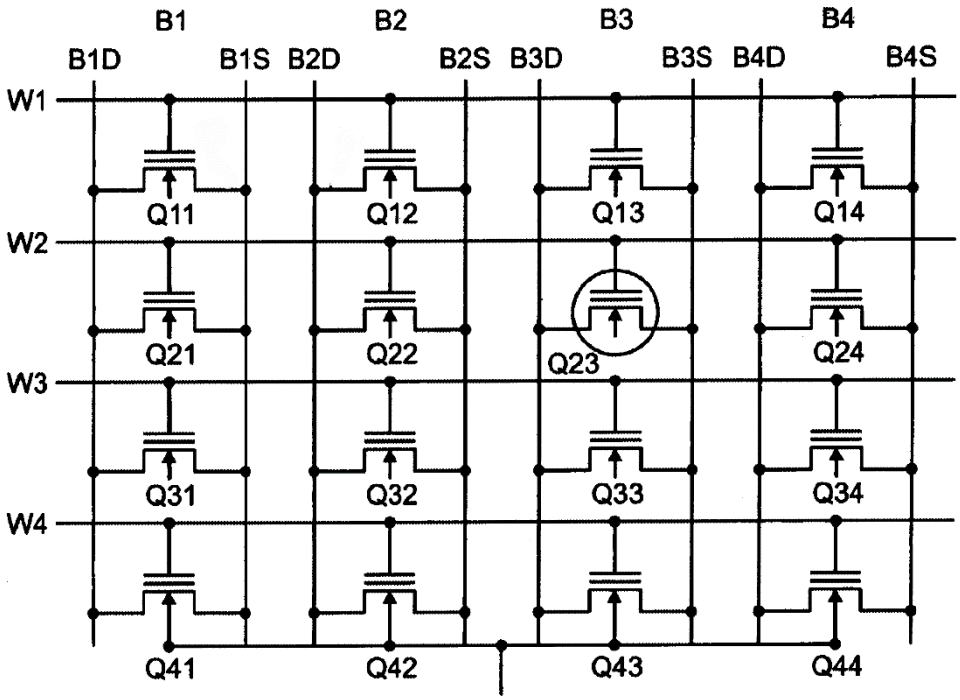

Figure 3.1: Example of memory cell array.

The polar polymers currently used in FeRAM research have a T_g below room temperature, or even below 0^oC. As we mentioned in section 2.4, when we are operating at temperatures above T_g, segments of the polymer chain can easily move and dipoles can

rotate, this leads to fast programming speed. However, the easier they can rotate, the easier it is to depolarize the polymer too.

Apart from the temperature, the applied electric field affects the dipoles rotation rate too. The stronger the field, the more the dipoles rotate. This characteristic is currently used in order to overcome the short retention problem. In other words, the programming fields are required to be much higher than the fields that can possibly destroy the memory retention. This increases the power consumption and it can never allow to meet the need of nanosecond programming time and ten years retention time.

In this thesis, we propose a novel class of ferroelectric memory technology that uses a polar polymer with high glass transition temperature in the gate dielectric stack. The high T_g of the polar polymer is a property that has never before been used in ferroelectric memories. The polymer can be poled to create remanent polarization (performing write/erase) at temperatures above T_g, where the dipoles can rotate quickly, leading to short programming times – even picoseconds. This means that a dual condition is required to program the memory – heating of the memory element to allow the dipoles to move while an electric field is applied in order to orient these dipoles. At operation temperature, well below T_g, the dipoles are locked in position which results in a long retention time even in the presence of strong depolarization fields. This immunity to depolarizing fields makes it a superior memory candidate against the conventional FeRAM, which is limited by the effect of these strong fields.

Below are presented the properties and advantages of proposed GeRAM over today's state-of-the-art memory technologies:

Scalability: SRAM, DRAM and Flash memory are so close to their physical scaling limits. The scalability of FeRAM is an important issue, the most advanced product is at the 130 nm node technology and no product has been introduced to the market in the last years. Resistive RAM (RRAM) is being used only as low density embedded memory. At issue is the fundamental mechanism of switching – the formation and dissolution of a random filament. This randomness poses serious issues for both yield and reliability. As for Phase Change RAM (PCRAM), its scalability is not clear yet, since the grain size is here an issue too. Thermal diffusion due to long RESET times on switching from amorphous state to crystalline state is the main concern. However, the scalability of GeRAM is very promising. It is based on polymers, and even a simple method like spin coating can lead to extremely thin films. The polymers dipole density varies from just one dipole every 0.2 nm (e.g. Polytrifluoroethylene) to greater than 1nm, meaning that for a 3nm square memory cell with 3nm thick polymer film, there are more than 3000 dipoles. Thus, GeRAM scales better than any of the already developed or under development memory technologies.

Speed: When the temperature is sufficient high, ~ $(T_g + 50)$ ^{o}C, dipoles in GeRAM are free to rotate making programming last only a few picoseconds. Read operation is similar to the one of DRAM and its speed dependent on the array size.

Power Consumption: The proposed GeRAM is a nonvolatile memory and, by nature, has low power consumption. The main energy consumption cause is the heat pulse that is used during programming. Since the program speeds are fast, the heated volumes are smaller and the required energy for the GeRAM devices is less. The

programming speed can potentially be as little as 10 ps, potentially making GeRAM the lowest energy consumption memory technology.

Retention: At temperature lower than T_g ($\approx T_g - 100\ ^oC$), the dipoles are locked in position. In this case, no external field can disturb the content of the memory cells, leading to extremely long retention time (electrets are known to be able to retain their polarization for over 100 years), no known memory technology can match this property. An example of the retention of an amorphous polar polymer is shown in Figure 3.2. This polymer has a T_g of 218 ^oC.

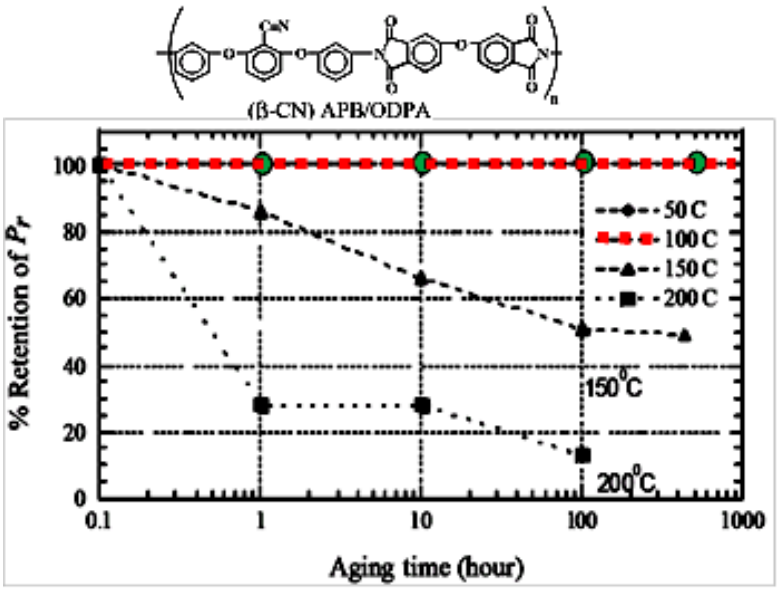

Figure 3.2: Example of polarization retention for a high T_g polymer.

As shown above, at operation temperature of 100 ^oC, no loss of remnant polarization is detected.[24]

Endurance: In an environment without oxygen, mass loss, or decomposition in other words, of the most polymers is negligible even at their melting temperatures. This means that in GeRAM devices where the polymer is fully encapsulates and programming is performed at temperatures well below melting, unlimited endurance is expected.

Density: Since the heat pulse can be so short (even a few picoseconds) and the heated volume is small, very high packing density is allowed. GeRAM can be 3-D stacked similar to NAND-flash technology.

Multi-bit programming: Multi-bit per cell is possible for GeRAM since the level of polarization can be controlled by the programming voltage, provided that saturation is not reached.

Radiation Resistance: FeRAM, PCRAM, and RRAM are expected to be sufficiently insensitive to radiation because they are non-charge based memories. FeRAM is sensitive to transient voltages developed on the CMOS peripheral circuit. GeRAM is FeRAM with this mode of sensitivity eliminated.

Operation Temperatures: Modern synthetic chemistry can tailor polymer properties virtually at will. GeRAM can be optimized for specific applications such as high temperature environments. For example, GeRAM with T_g = 400 ^oC (polyimide) can be used in an environment up to 300 °C.

Cost: The potential cost of the GeRAM devices is low since simple polymers are used and not some extraordinary/exotic materials that are hard to fabricate. Moreover, these polymers are applied with the spin-coating method, which is one of the most inexpensive methods to form thin films.

CHAPTER FOUR POLYIMIDE LARC-CP1

Polyimides (PIs) are a class of polymers that is produced by polymerization of imide polymers, and, depending on the composition of their main chain, can be linear, aromatic (ring-shaped chain), or semi-aromatic. Aromatic molecules are very stable, and it is not easy to break them apart to react with other substances. Organic compounds that are not aromatic might be cyclic, but only aromatic rings have the special low reactivity. Another classification of the polyimides arises from the type of interactions between the main chains. They can be either thermoplastics of thermosettings. Thermoplastic polymers become moldable above a specific temperature and solidify upon cooling. However, in case of a thermosetting polymer, once hardened a thermoset resin cannot be reheated and melted to be shaped differently.

Typically, polyimides are not affected by commonly used solvents and oils. They also resist weak acids but are not recommended for use in environments that contain alkalis or inorganic acids. They are also lightweight, flexible, and resistant to heat.

Polyimides are commonly used in industry for flexible cables, as an insulating film on magnet wire and for medical tubing. In semiconductor industry polyimide materials are used as high-temperature adhesives, and as mechanical stress buffers. They are also used as insulating and passivation layers in the manufacture of digital

semiconductor and MEMS chips. Finally, polyimide coatings are used as multi-layer insulation on spacecraft, since they exhibit good radiation and heat resistance.

4.1 LaRC-CP1 (Langley Research Center – Colorless Polyimide1)

The polar polymer selected to demonstrate our concept is LaRC-CP1 (2,2-bis(3-aminophenyl) hexafluoropropane+2,2-bis[4-(4-aminophenoxy) phenyl] hexafluoropropane), which is commercially available by NeXolve Corporation. LaRC-CP1, as well as LaRC-CP2, are colorless polyimides developed by NASA at Langley Research Center, to make transparent and flexible thin polymer films for applications such as large space reflector/collector inflatable antennas, solar arrays, and radiometers.[25] LaRC-CP2 has a lower breakdown field and glass transition temperature, so it was considered inferior to LaRC-CP1 and it is no longer commercially available. LaRC-CP1 films exhibit great temperature, chemical and radiation resistance, while they have the lowest moisture uptake among the commercial polyimides. Having a material that does not absorb much moisture is beneficial in case of electronics, where components heat, expand and contract.

Figure 4.1: NeXolve Corporation is using NASA-derived thin films to construct the five-layer sunshields—one of which is shown here on a test fixture—for the James Webb Space Telescope. Image courtesy of Northrop Grumman Aerospace Systems

LaRC-CP1 has high dielectric strength (> 2 MV/cm) and high T_g (~ 260 °C), making it a good candidate for demonstrating the thermal-assisted programming concept. Figure 4.2 illustrates the chemical structure of the LaRC-CP1 polyimide molecule, while the dipoles that can be responsible for ferroelectric behavior are noted in the dotted circles. LaRC-CP1 liquid resin was acquired by NeXolve Corporation, and was further diluted in anhydrous N-methyl-2-pyrrolidone (NMP) to the lower concentrations.

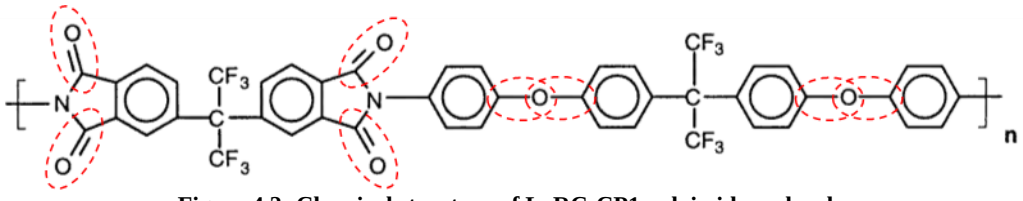

Figure 4.2: Chemical structure of LaRC-CP1 polyimide molecule.

When attempting to spin coat solutions with high concentrations, the result was polymer agglomeration (sticking of molecules to one another). Agglomeration (or flocculation) is the process of contact and adhesion of nearby particles and the formation of larger-size clusters. To reach an actual agglomeration the destabilized particles (or molecules in case of a polymer) need to collide with each other or get in range of mutual attraction. This is what happens during spin coating. The centrifugal force make the molecules move towards the edge of the sample, while colliding with each other.

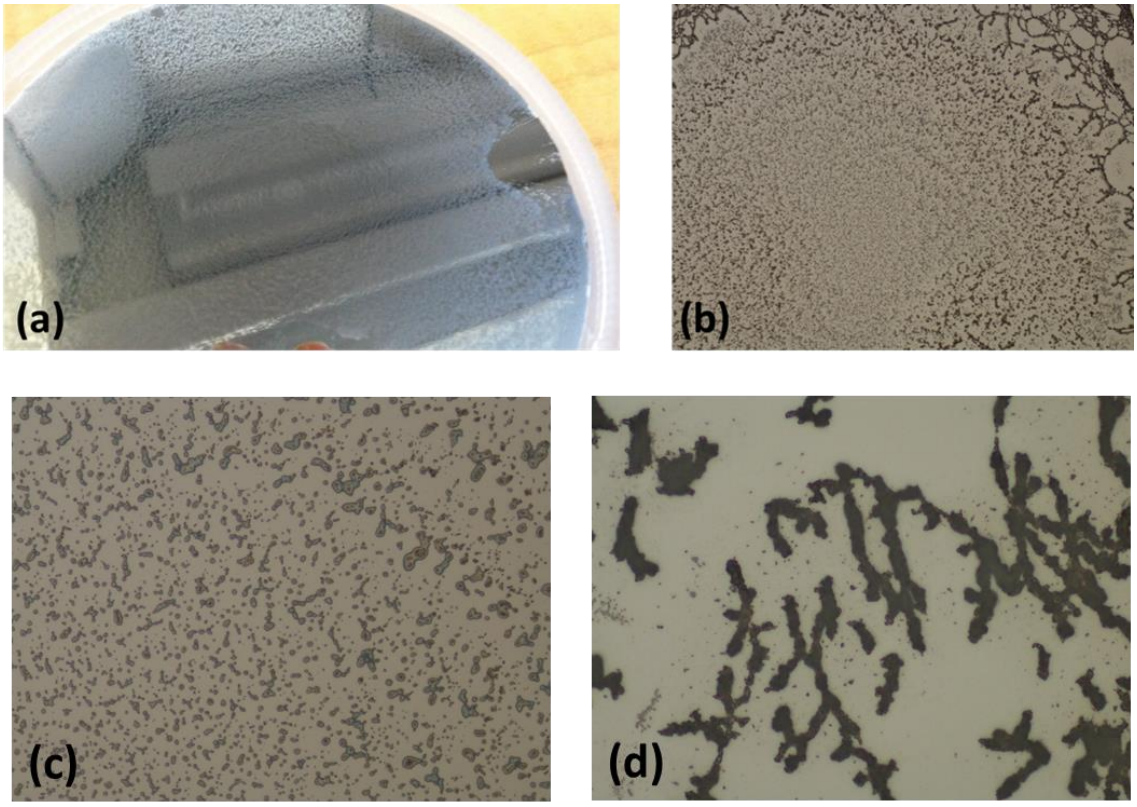

Figure 4.3: Polymer agglomeration after spin-coating of a 3% LaRC-CP1 solution on Si at 2500rpm (a) photo of the wafer, and optical image through microscope (b) x5, (c) x20, and (d) x50 magnification .

There are two agglomeration mechanisms. The first one is the charge mechanism for short-chain polymers, which attach themselves only to a particle and move its surface charge such that there is interaction with other particles. The other mechanism is the bond model in which multiple solid particles are grouped together by a polymer network of long-chain polymeric molecules to agglomerate.

Figure 4.4: https://www.afssociety.org/coagulation-flocculation-and-agglomeration/

The mechanisms depend on the material system and treatment of the sample. The results of agglomeration are highly variable and have many influencing parameters such as the amount and duration of energy input, the concentration of molecules in the solution, and the stirring force (spinning speed).

After several attempts with different solution concentrations, the specific concentration of 1.11% solution by volume was selected because it was the highest one that was not causing agglomeration during spin coating.

Spin coating to form continuous films was performed at 2500 rpm for 80 seconds and the resulting film thickness was ~2.6 nm. Figure 4.5 presents the optical image of the

formed continuous film. A scratch through the film is done using a razor blade in order to optically verify the existence of the polymeric film. In Figure 4.5(b), we can have a closer look at the scratch. We can distinguish the central mark that scratches not only though the polyimide, but also the Si surface. Around that deep scratch, we notice that another area is also defined. This is due to the part of the polymer film that was removed while scraping the sample with the razor blade.

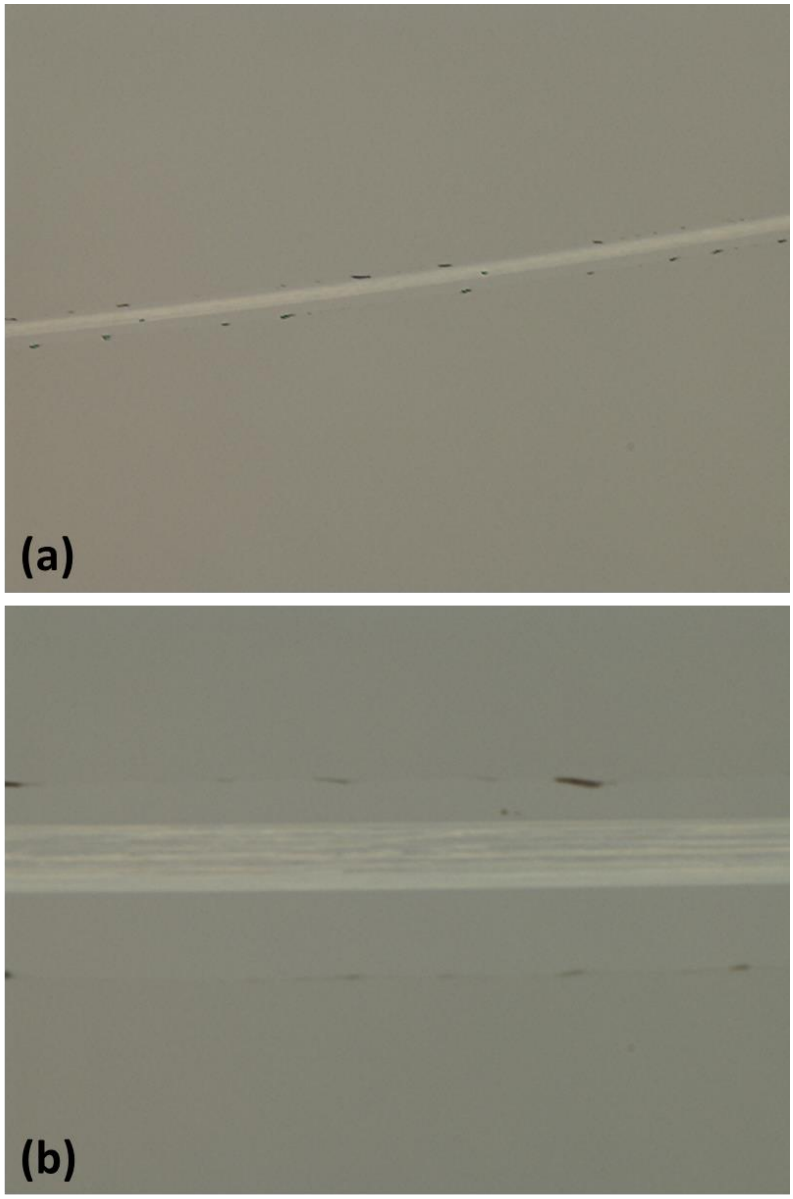

Figure 4.5: Spin-coated continuous LaRC-CP1 film on Si (a) x20 , (b) x100 magification.

While using the above mentioned concentration of 1.11% solution by volume and the 2500 rpm spin speed in order to acquire continuous polymer films without the presence of agglomeration, the resulting film thickness is ~2.6 nm. For a thicker film, consecutive spin coatings are required.

LaRC-CP1 is a polyimide that can be fully cured even at temperatures as low as 100 ^{o}C. This is a property that is highly preferable in case that there are metal patterns already deposited before the polymeric film is deposition, and metal migrations needs to be avoided. In our study, there was no concern for metal migration, and curing temperatures as high as 310 ^{o}C were used, which also shortened the curing process. The full curing recipe used is as follow (Figure 4.6): a 1-hour ramp to 100 °C; soak for 1-hour, another 1-hour ramp to 200 °C, soak for 1-hour, a final 1-hour ramp up to 310 °C, soak for 2.5-hours at 310 °C and as a final step, a 3-hour ramp down to room temperature.

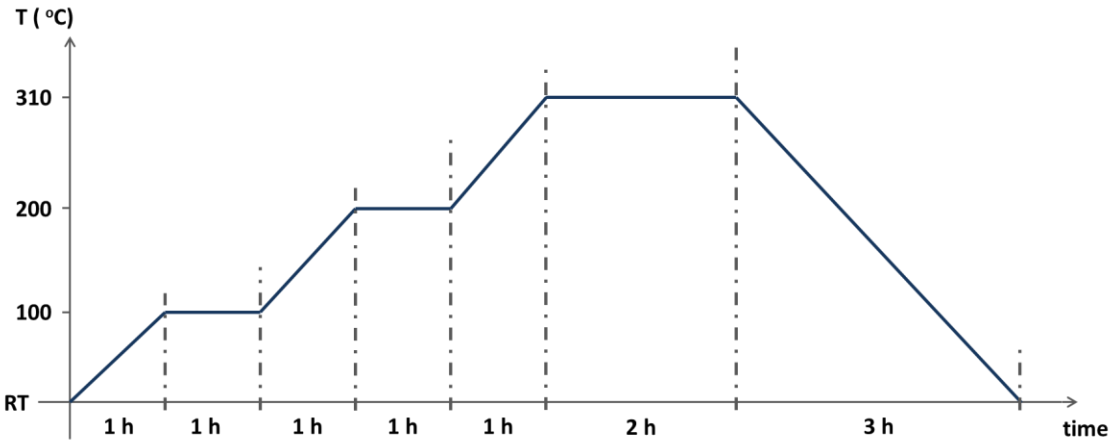

Figure 4.6: LaRC-CP1 curing process steps.

4.2 Dielectric Spectroscopy Experiment for LaRC-CP1

For the purpose of the dielectric spectroscopy measurements, capacitors with LaRC-CP1 polar polyimide as the dielectric material were fabricated.

Low resistivity p-type Si wafers were used as the substrate, and continuous films of 80 nm Al and 20 nm Cr were deposited using E-Beam Evaporator to form the bottom electrode of the capacitors. Next, four consecutive films of LaRC-CP1 were spin-coated and cured to form a ~11 nm thick film. For the top electrode, continuous films of 20 nm Cr and 100 nm Pt were deposited through E-Beam Evaporation. The top metals were then patterned with negative photoresist AZ5214E, and, as a last step, they were etched using Ion Mill to form the desirable electrode of area 30 x 30 μm^2 as shown in Figure 4.7.

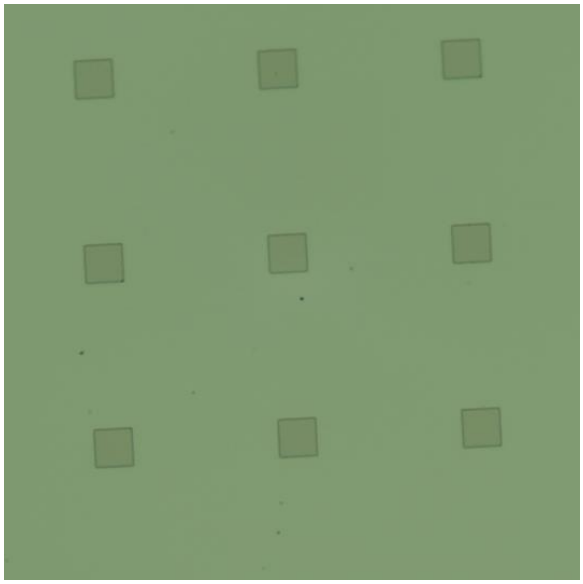

Figure 4.7: Microscope image of an array of fabricated capacitors.

A graphic representation of the cross-section of the fabricated capacitors as well as the experimental setup is shown in Figure 4.8.

The sample (a cleaved piece of the wafer containing the capacitor structures) is placed on a heating chuck, the temperature of which is accurately controlled through a LabVIEW program. An Agilent 4194A impedance analyzer is employed to carry out the measurements. Two probes are used, one that is landed on the continuous film bottom electrode, and one that is landed on the square pattern that forms the top electrode. The impedance analyzer applies an AC signal with 50 mV amplitude and sweeps the frequency from 6 kHz to 5 MHz. The measurements are performed at temperature range RT (room temperature) to 305 ^{o}C. The temperature of the chuck is kept stable during each measurement.

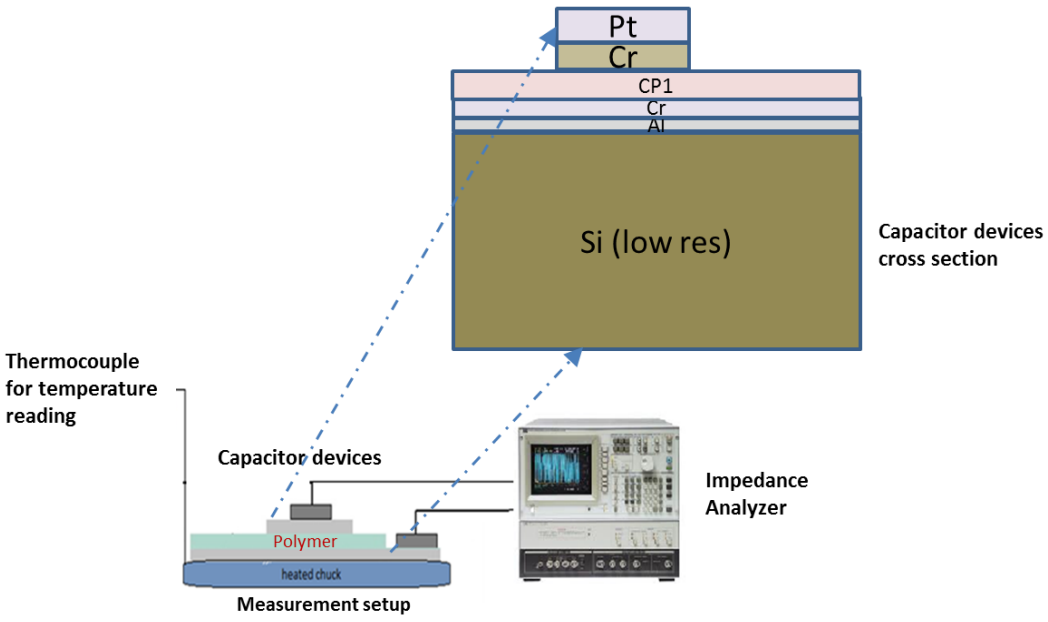

Figure 4.8: Samples and setup used for dielectric spectroscopy measurements.

As we described in the previous sub-section, G and R_p are given by the impedance analyzer, and using equations (3.7) and (3.8) ε' and ε" are obtained. The obtained data are shown below in Figure 4.9 and Figure 4.10.

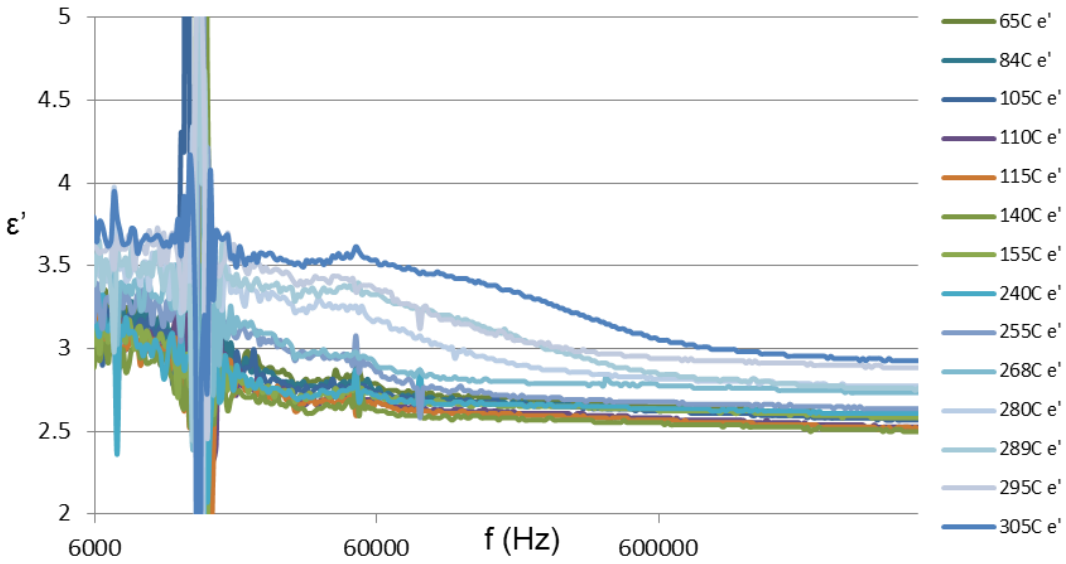

Figure 4.9: Measurement results of the real part of dielectric permittivity.

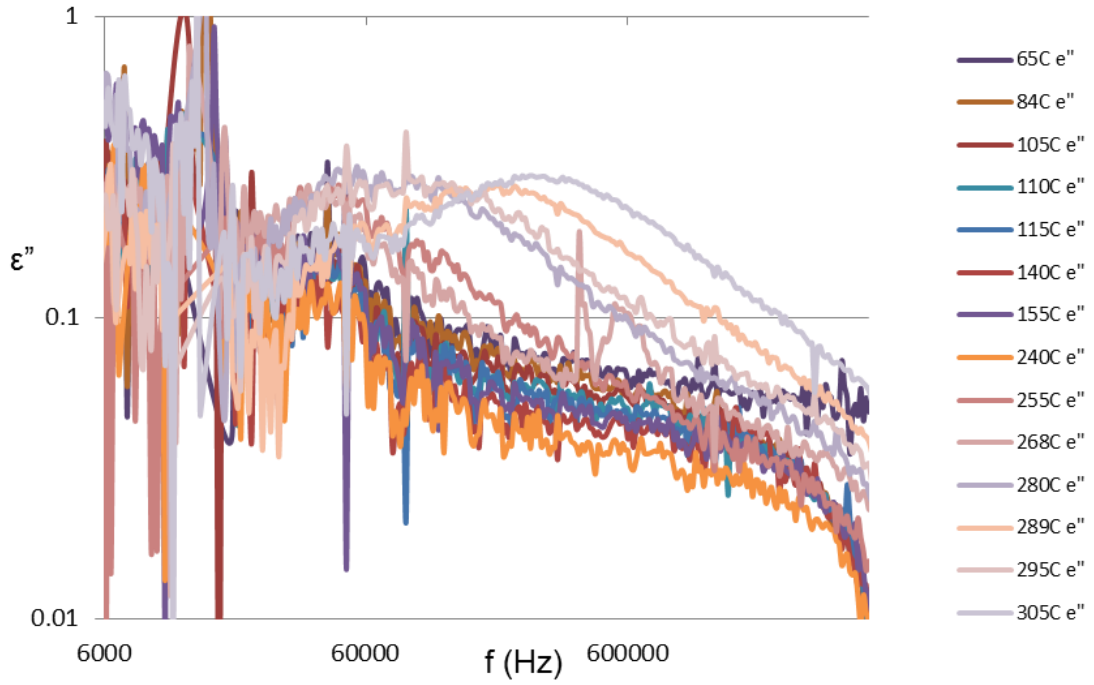

Figure 4.10: Measurement results of the imaginary part of dielectric permittivity.

We observe that for frequencies below 15 kHz, the system exhibits high noise and we cannot notice any changes in ε’ and ε”. Though, we note that at temperature below 240 ^{o}C, ε’ and ε” seem not to change with temperature. As temperature rises above 240 ^{o}C and approaches T_g (~265^{o}C), we observe that ε’ exhibits a drop while ε” a peak at f_c. It is seen, for example, that at 289 ^{o}C the characteristic frequency is ~196 kHz, and at 305 ^{o}C it is ~295 kHz.

Now we select one frequency and we plot the real and the imaginary part of the dielectric permittivity versus temperature. The chosen frequency is 65 kHz, where most of the curves are not yet past the characteristic frequency, and the dipoles still follow the field. The results are shown in Figure 4.11, where it is seen that the glass transition

temperature for the polymeric film is ~285 ^{o}C. The observed T_g is quite different from the expected bulk T_g, however, this is well known that the glass transition depends on the thickness of the polymer film.[26],[27]

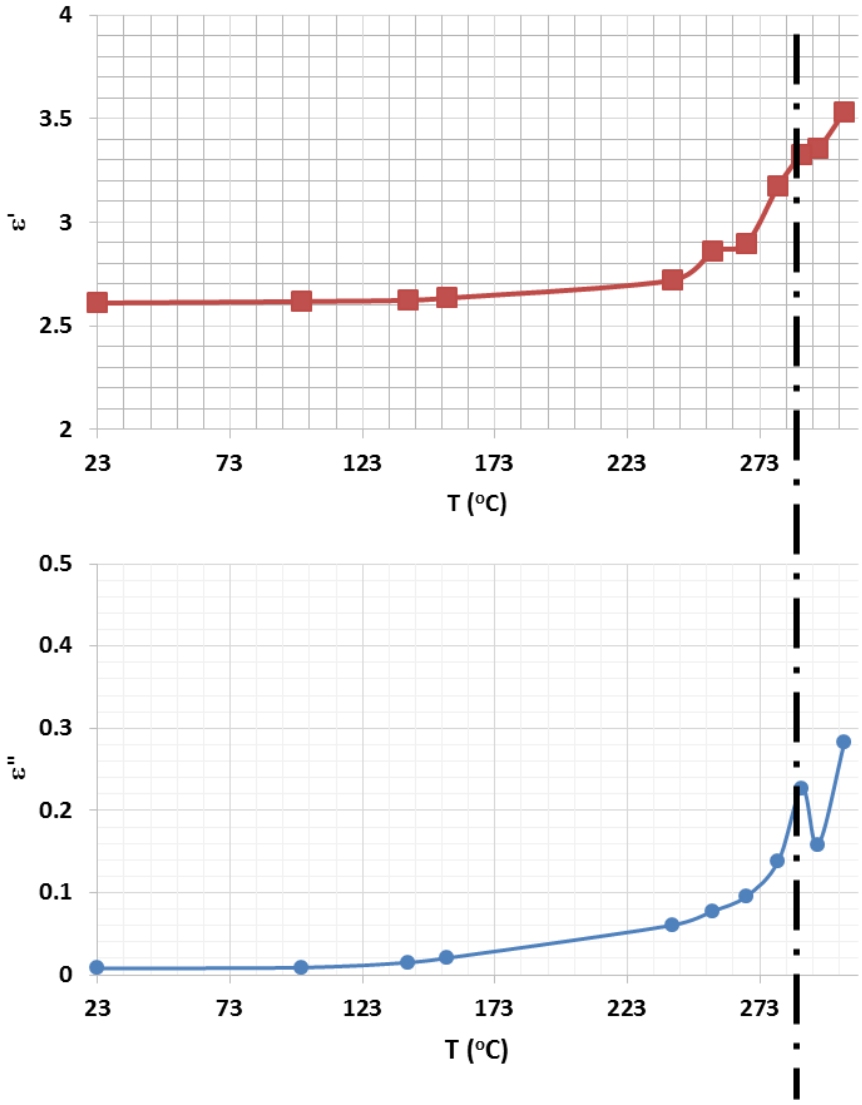

Figure 4.11: Real (ε') and Imaginary (ε'') part of dielectric permittivity versus temperature.

As we mentioned in the section discussing the dielectric spectroscopy in polar polymers, the characteristic frequency, f_c, depends on the operating temperature. This can be seen in Figure 4.12, where f_c is plotted versus temperature in logarithmic scale. Data are fitted to a straight line spanning 10 orders of magnitude to demonstrate that dipole rotation rates are indeed strongly dependent on temperature. This extended extrapolation might seem extravagant. However, it is reported that the viscosity of chalcogenide glasses vary smoothly as a function of temperature over 17 orders of magnitude. The reported viscosity/temperature dependence was not quite exponential (viscosity decreases somewhat faster than exponential for decreasing temperature).[28] Using this reported behavior as a reference, the exponential extrapolation presented in here is both justified and possibly even overly pessimistic. This plot is the most useful one produced in this section, since it can help us define how fast we can program the ferroelectric memory and it can give us a lead for the expected retention times.

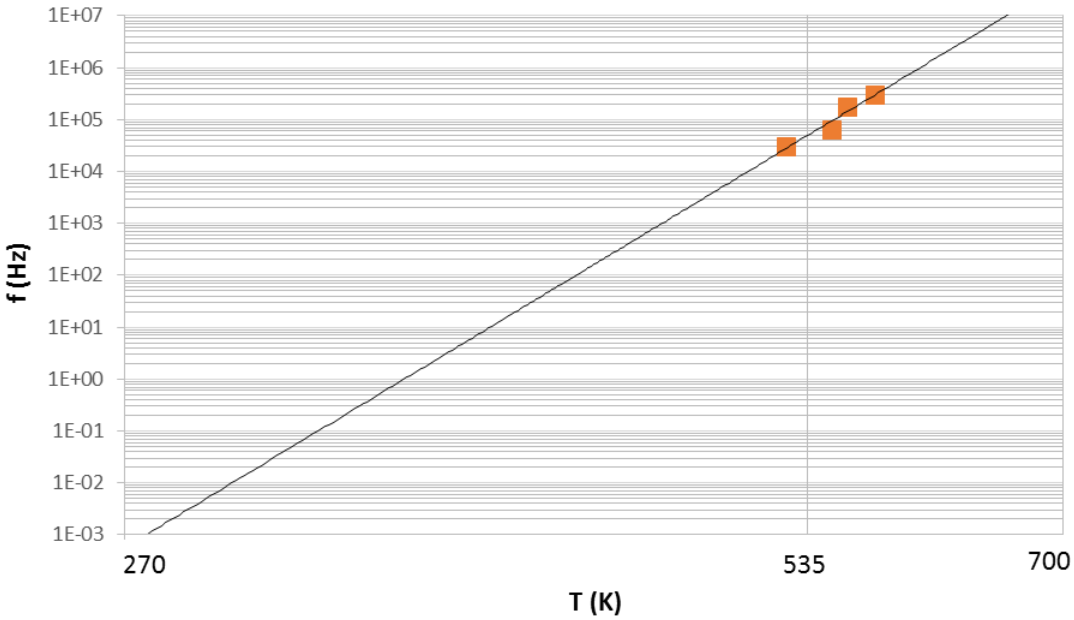

Figure 4.12: Characteristic frequency versus temperature.

CHAPTER FIVE FEFET DEVICE FABRICATION

A FeFET is similar to a MOSFET, with a Ferroelectric material as the gate dielectric. The organic FeFET can either be all-organic, meaning the gate oxide and the channel consist of organic materials, or have organic gate dielectric and inorganic semiconductor. While the all organic FeFET could, possibly, result in a better semiconductor channel/dielectric interface, usually the charge mobility in the organic materials is limited and the process of the fabrication of an organic semiconductor is not that advanced as that of the commonly used inorganic ones (e.g. Silicon).

For the purpose of demonstrating our proposed memory technology, we fabricated junction-less thin-film transistor with a n-type poly-Si layer as the device channel and a thin polar polymer (LaRC-CP1) as the ferroelectric gate dielectric.

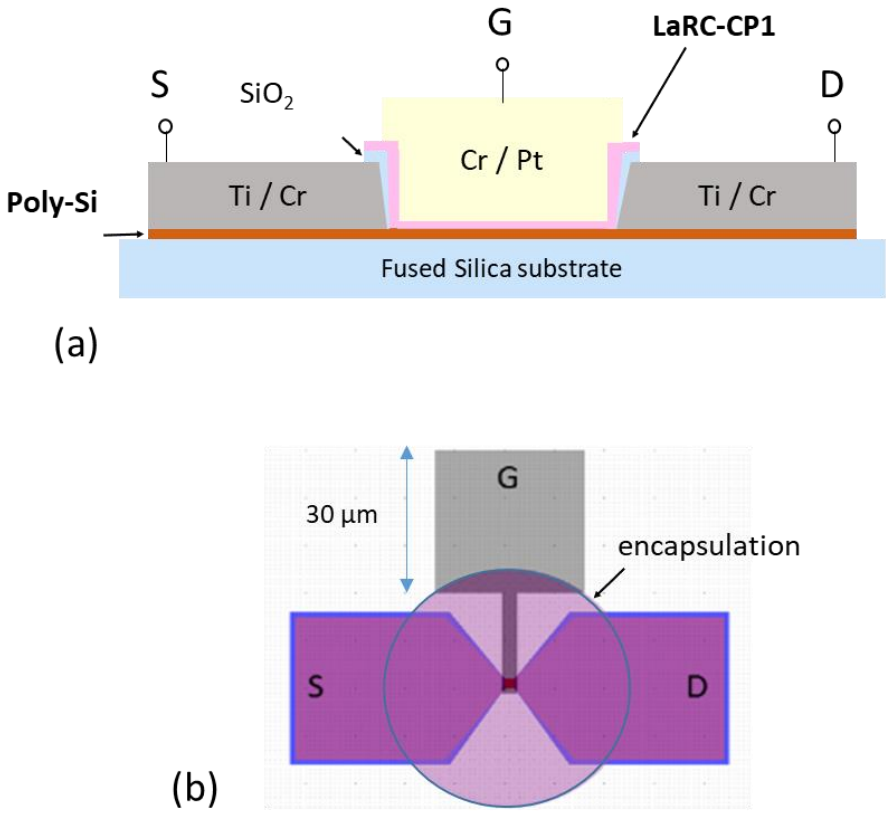

Figure 5.1: FeFET cross-section and device layout.

The fabricated junction-less transistor is schematically shown in Figure 5.1, while all the masks used for fabrication are presented in Figure 5.2. It is worthy to mention here that the specific structure of the junction-less FET is chosen for its simplicity to prove the concept of the proposed GeRAM, not due to its performance. The device substrate consists of a fused silica wafer which was initially RCA cleaned (without the HF dip). Fused silica was selected as a substrate in order to avoid the formation of parasitic capacitances from one contact pad to the other. 15 nm n-type poly-Si layer was grown by low-pressure chemical vapor deposition (LPCVD) at 650 °C. Though it is extremely difficult to control the resistivity of such a thin film (only 3 min deposition time), the

resulting resistivity was within our acceptable limits (0.25 MOhm-cm) for realization of a significant/noticeable channel depletion.

Following the poly-Si deposition, a 4-hour nitrogen flow anneal at 800 °C was performed to activate the dopants (phosphorus) inside the film. After the poly-Si deposition the grain boundaries are rich with incomplete bonds, which trap free carriers. For this reason, a 45-min forming gas (10% H_2 in N_2) anneal at 420 °C followed to passivate the interface defects. The poly-Si layer was then patterned and etched to form the transistor channel. The etching process was dry using a deep silicon etcher (inductively coupled plasma - ICP) which uses a fast switching Bosch process (almost anisotropic) that produces smooth sidewall profiles. The silicon to silicon oxide selectivity is 100 to 1, meaning that during this process, the silica substrate is not damaged and the actual step of the channel-to-substrate remained 15 nm, the thickness of the poly-Si layer. The ability to keep this channel-to-substrate step small is important in order to achieve a continuous polymer film through spin coating in a later process step.

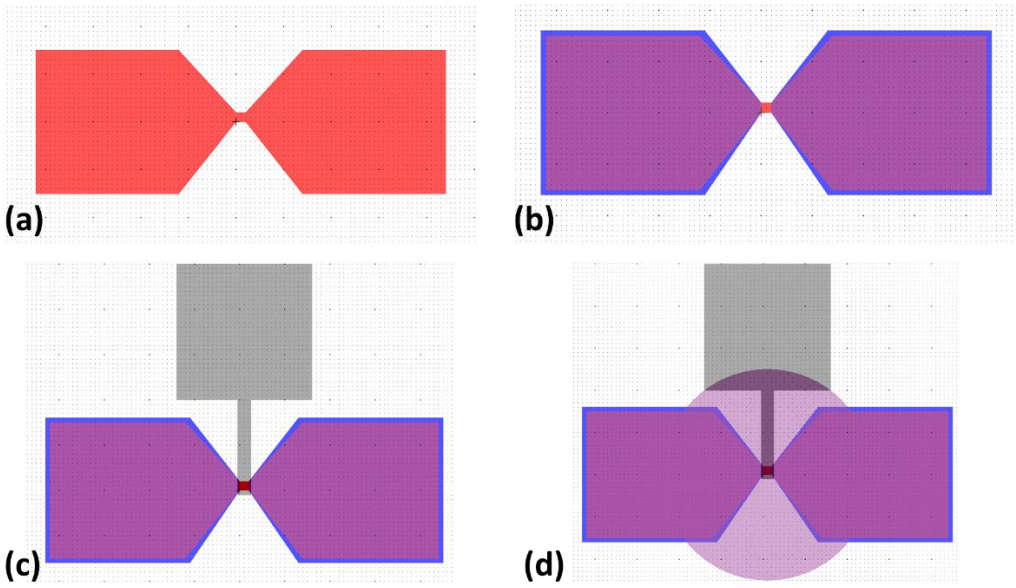

Figure 5.2: Masks used for FeFETs fabrication (a) formation of channel and source and drain, (b) mask for lift-off process for the source and drain metal pads, (c) etching mask for gate electrode, and (d) shadow mask for device encapsulation.

Sequentially, following a 10-sec 2% HF dip to remove the native oxide grown on the poly-Si, 30 μm x 30 μm source and drain metal pads (40 nm Ti /70 nm Al) were formed by E-beam evaporation and lift-off. During this deposition, a 110 nm SiO_2 layer was deposited on top of the metals as an isolation oxide layer in order to mitigate gate to source and gate to drain leakage. The deposition rate for the Ti and the SiO_2 was 1.0 Å/s, while for the Al film it was 5.0 Å/s.

The sample was then cleaned in N-Methyl-2-pyrrolidone (NMP) solvent and isopropyl alcohol (IPA), followed by a short (1 min) reactive-ion etching (RIE) descum process to prepare the substrate for the polymer adhesion. The LaRC-CP1 gate dielectric stack is formed next. The desired film thickness requires five consecutive spin coatings at 2500 rpm for 80 s to avoid agglomeration. Each coating is followed by a curing thermo-

cycle consisting of a 40-min ramp from room temperature to 120 °C followed by a 1-hour soak at 120 °C to avoid the formed polymer layer being dissolved by the next coating. For the last layer, the curing cycle was changed, to fully cure the polyimide, to a 1-hour ramp to 100 °C; soak for 1-hour; another 1-hour ramp to 200 °C; soak for 1-hour; another 1-hour ramp to 310 °C; soak for 2.5-hours; and finally, a 3-hour ramp down to room temperature. The thickness of the LaRC-CP1 polyimide films (15.5 nm) was verified by both profilometer and atomic force microscopy (AFM). Afterwards, the gate electrode (30 nm Cr /210 nm Pt, at 1.0 Å/s deposition rate) was deposited by E-Beam Evaporator and then patterned using negative resist AZ5214E and etched by ion milling. Cr was selected for good adhesion to polyimides.[29][30][31] This ion milling process consists of 5 etching steps that etch the platinum and chromium to form the gate electrode, and finally through the polyimide and oxide layers till the aluminum layer of the bottom electrode is reached, to gain access to the source and drain pads. The layers etched are detected using the secondary ion mass spectrometry (SIMS) endpoint detector, as shown in Figure 5.3. Finally, the active area was encapsulated by a 300-nm thick oxide layer deposited through a shadow mask (not shown in Figure 5.1b). The wafers were then diced into 5 mm x 5 mm pieces for electrical characterization.

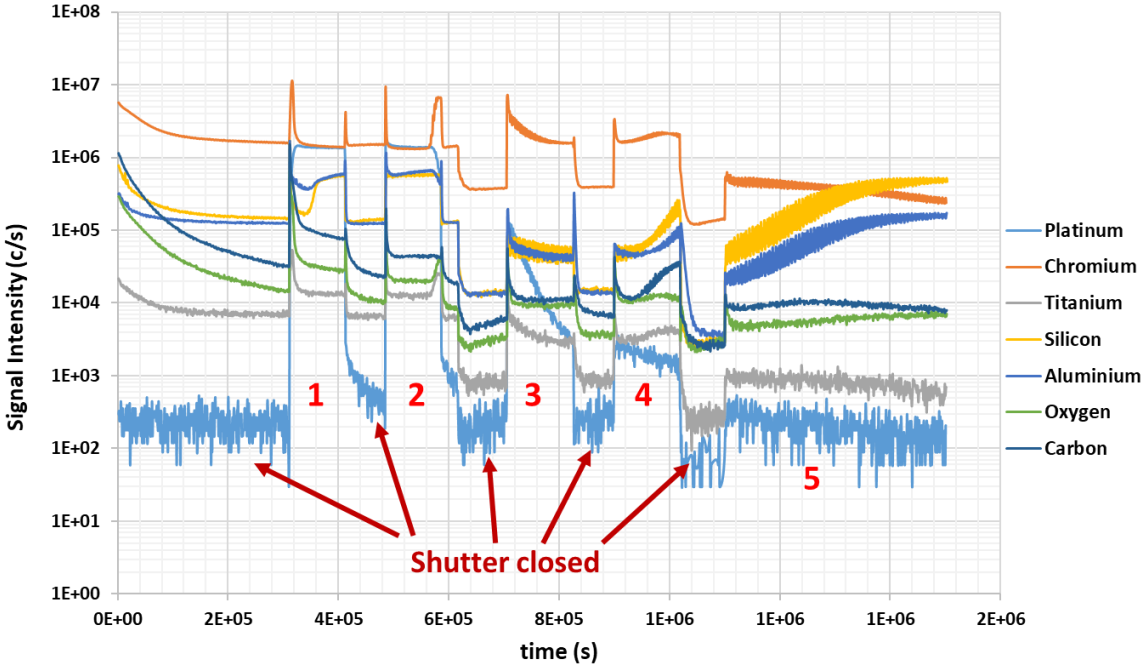

Figure 5.3: SIMS end-point detection

To minimize the defects created due to ion bombarding in the device active area (transistor channel) during Ion Milling, preventive measures were taken. First, when the platinum layer of the top electrode is etched through, the power used to mill is reduced as seen in third etching step in Figure 5.3, and then when the polyimide layer is reached the power is reduced further (fifth step). This way, when the top metals are milled and the power is reduced, the etching rates get slower and the depth of the damage induced by the ions is minimized. Another precaution taken is the designed overlap of the gate and source and drain as shown in Figure 5.1a, as well as in Figure 5.4. This 500 nm gate to source and gate to drain overlaps prevent any ion induced damage of the polyimide film to happen at the active area (channel) of the device. Moreover, this designed overlap

serves as a safeguard in case that there was a lithography mask misalignment to ensure that the whole channel area remains under the gate electrode.

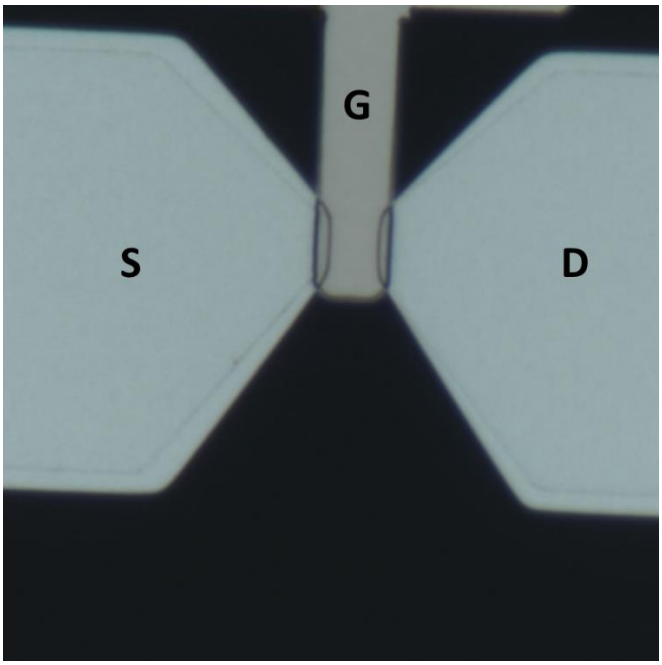

Figure 5.4: Optical microscope image of the fabricated device showing the gate-drain and gate-source overlap

One of the devices is selected to be used for extracting SEM (Scattered Electron Microscopy) images. Figure 5.5(a) presents the SEM image of the device top view, and Figure 5.5(b) is the top view of the same device after using the Focused Ion Beam (FIB) to mill through the device in order to acquire the cross section images.

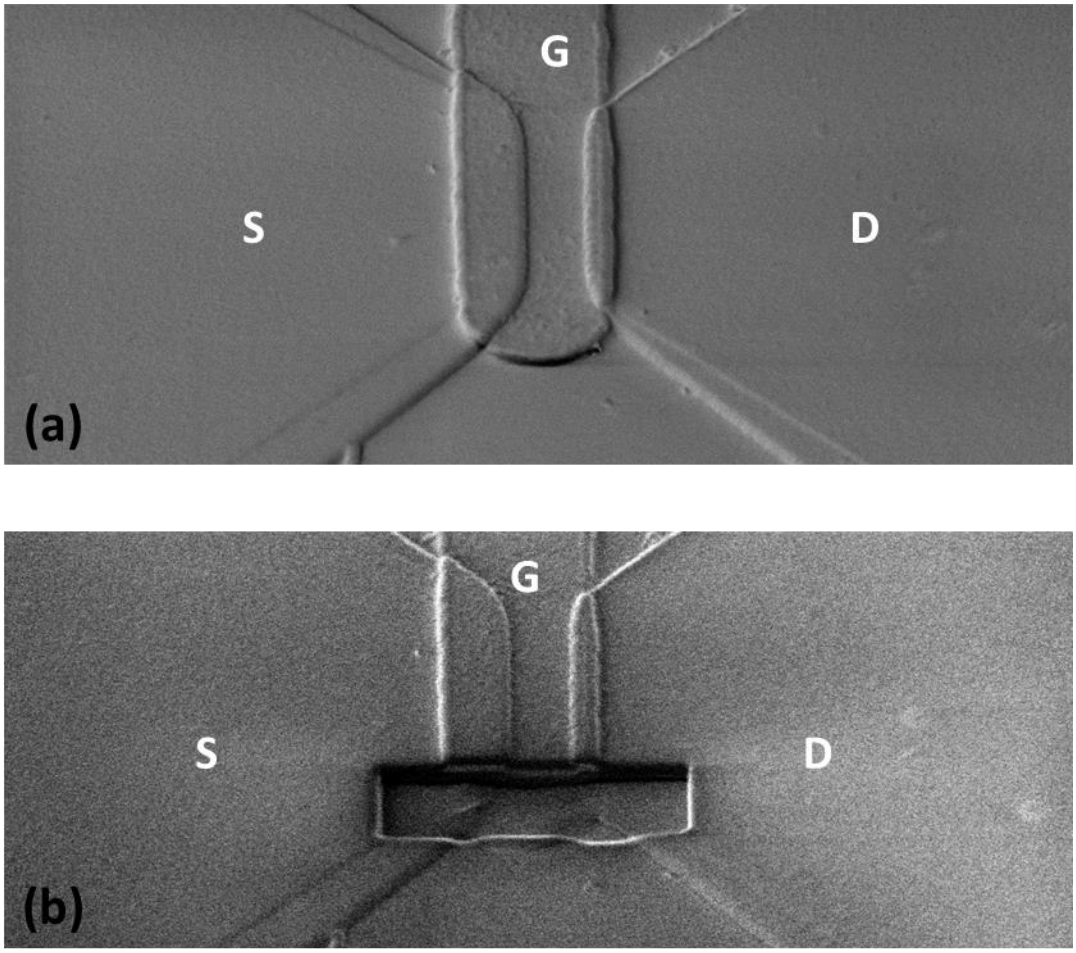

Figure 5.5 (a) SEM image of device top view, (b) device top view after FIB

Figure 5.6 shows the device cross section, where the different layer can be observed. The thickness of deposited polyimide (LaRC-CP1) is measured to be around 14 nm, which is close to what profilometer has also shown.

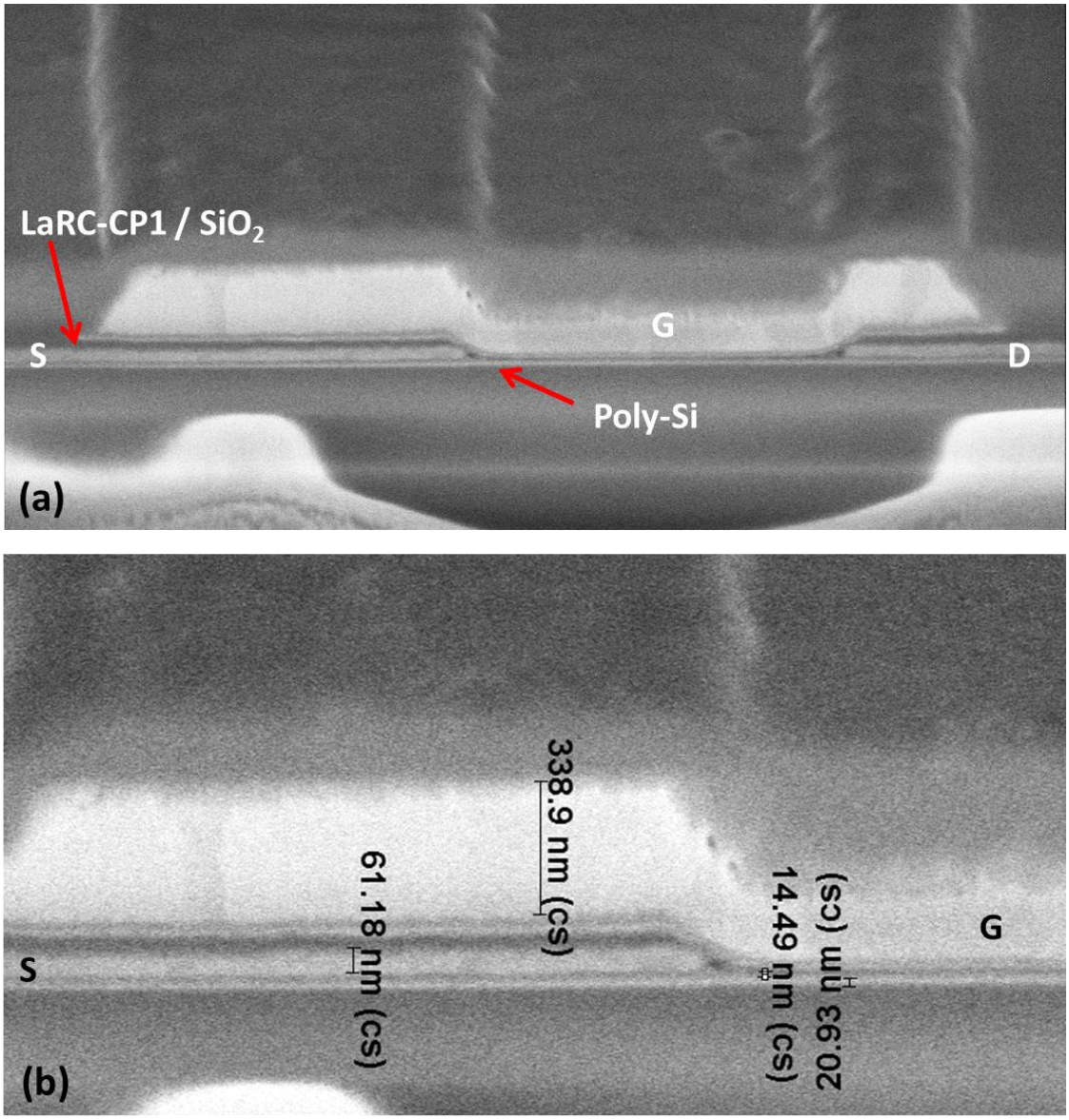

Figure 5.6. Cross-section of a fabricated device

CHAPTER SIX DEFECTS ANNEALING IN POLYMER FILMS

Leakage currents are undesirable when polymer films are used as insulators in electronic devices, especially in case of Ferroelectric Field-Effect-Transistors (FeFETs). [15][32] In FeFETs, the polar polymer incorporated in the gate dielectric stack is required to be extremely thin (of the order of nanometers). Even though a particular polymer may have very high intrinsic resistivity, many factors degrade this property when applying thin polymeric films.[33] These factors include residual water, solvents, impurities, mobile ions, and defects (electron traps). Thermal annealing treatments can be utilized to drive out water and solvents, as well as to repair defects created during device fabrication. Polymer defects have numerous forms but can be broadly defined as anything that upsets the regularity of the chain (kinks, folds, chain ends, or impurity atoms). All these irregularities can produce localized states in the energy gap.[33] In general, annealing of defects is a slow process even at temperatures above the glass transition temperature (T_g).[34][35] This is amply demonstrated in a recent report [36] which details two-step annealing at or near melting temperatures (T_m, ≈200 °C above T_g), that lasted over an hour. This annealing did reduce the leakage current through the polar polymer. By contrast, here, it is reported the unexpectedly efficient rapid reduction of the gate leakage current through short (minutes) and mild (at around T_g) annealing of a FeFET memory device with a ≈15 nm thick polar polymer (Langley Research Center-

Colorless Polyimide 1, LaRC-CP1) as the gate dielectric. The observed leakage reduction indicates that annealing leads to a rapid and drastic decrease in defect density. Considering the detailed process of the FeFET fabrication, we conclude that these particular defects were created by mechanical stress induced by the gate metal deposition, and that the defects are very local atomic displacements driven by the strain created in the polymer film. Upon heating, these highly local atomic displacements anneal rapidly. The strong correlation between the onset of defect annealing and the onset of dipole rotation supports this local atomic movement model.

6.1 Annealing Effect Measurements

Figure 5.1 in previous chapter illustrates a cross-sectional schematic of the FeFET memory devices used in this study. The devices are junction-less thin film FeFETs incorporating a fully cured ≈15 nm LaRC-CP1 film in the gate dielectric stack. Figure 6.1a shows a representative subset of gate leakage current density (J_g) characteristics of the fabricated FeFETs as a function of temperature for a device with a channel length of 3 μm and width of 3 μm. The device was heated from room temperature up to 270 °C (T_g ≈260 °C for LaRC-CP1) on a temperature controlled hot chuck. For each measurement, the temperature was risen to the target value by the controller and the measurement was immediately performed while the controller was holding the temperature stable. Immediately after the measurement, the controller drives the chuck (and so does the device under measurement) to the next temperature point. Initially, as expected for most insulating films, it is observed that J_g increases with increasing temperature. It is also noted that the drain current characteristics exhibit a clockwise (CW) hysteresis loop

(Figure 6.2a), which decreases in width as the temperature increases. This hysteresis width is the maximum lateral shift (amount of gate voltage shift for a constant current level) between the V_g sweeping up and sweeping down curves. It is observed that, in this subset of data, the leakage current reaches its highest point at a temperature ≈ 200 ^oC. At the subsequent temperature point (230 ^oC), it is seen that J_g is much smaller and, concurrently, the drain current hysteresis becomes negligible. At the next point (260^oC) the observed hysteresis loop reverses direction to a counter-clockwise (CCW) pattern (Figure 6.2b).

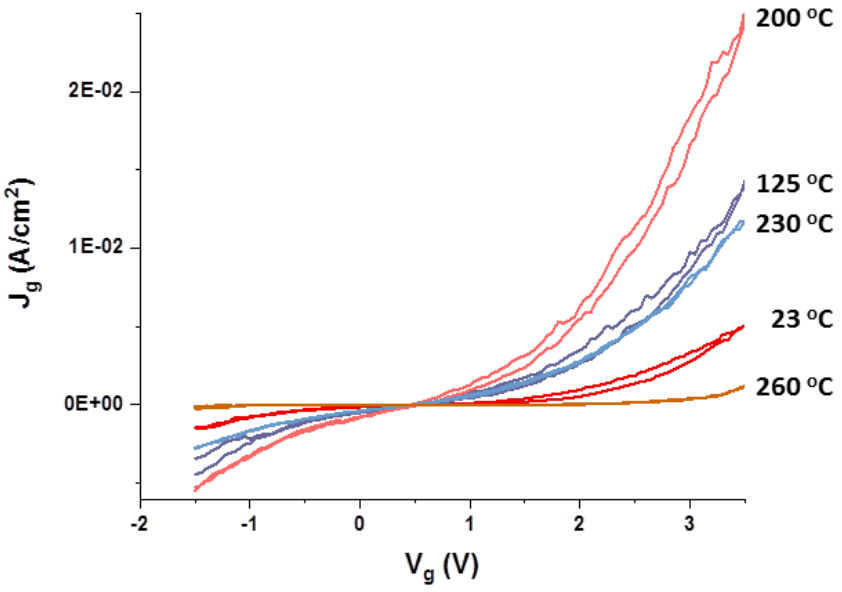

Figure 6.1: Heating of a virgin device with channel L = 3 µm, W = 3 µm: leakage current density versus gate voltage in a linear scale.

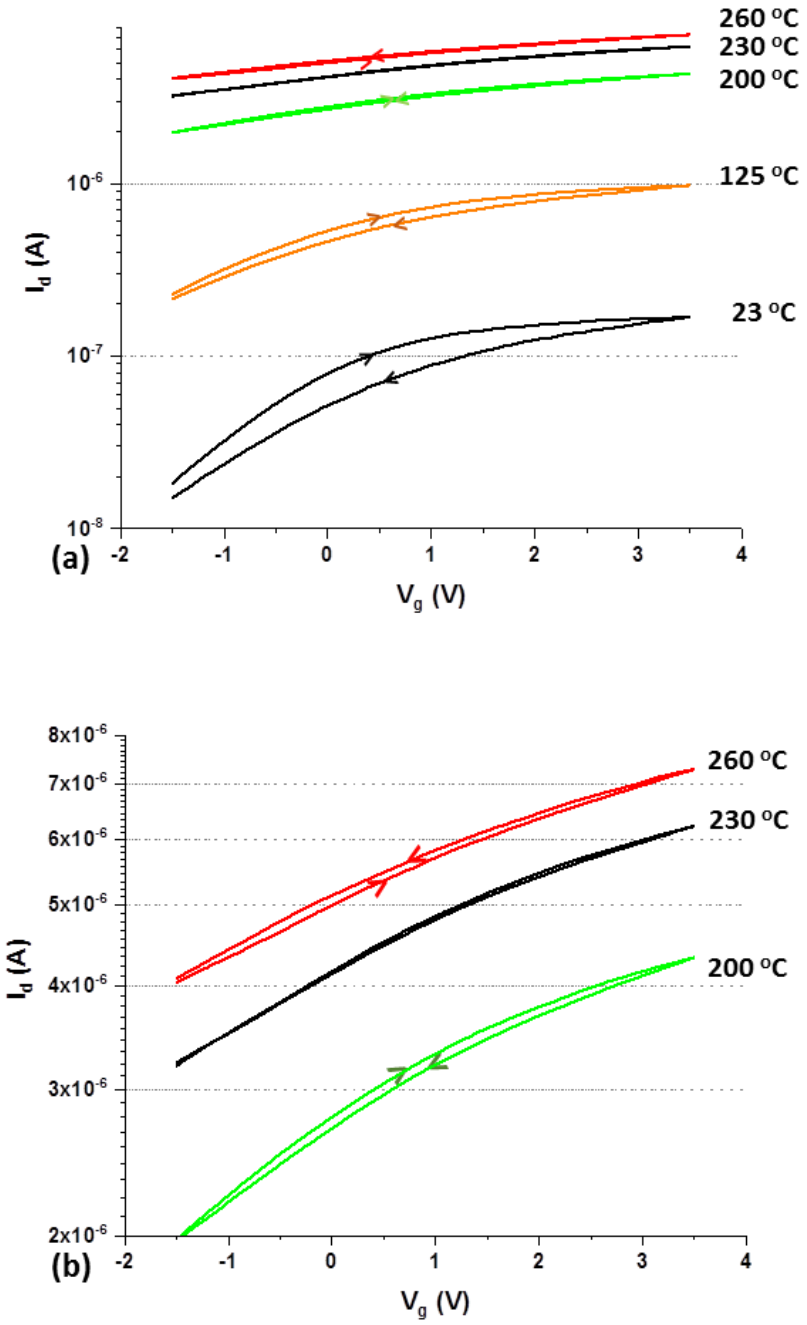

Figure 6.2: Heating of a virgin device with channel L = 3 µm, W = 3 µm: (a) I_d-V_g characteristics in a semi-log scale (direction noted by arrows), and (b) is an expanded scale view of the Id-Vg characteristics at the highest temperatures.

The above observations and especially the apparent correlation between the sudden drop in leakage current density and the change in direction of the $I_d - V_g$ hysteresis can be seen more clearly in Figure 6.3. In this figure, all measurements points are included, not only the subset used to construct Figure 6.1and Figure 6.2. As observed, after cooling the device down to room temperature, the leakage current remains low and the hysteresis loop direction remains CCW. This suggests that the annealing cycle has improved the film quality, and the process is irreversible.

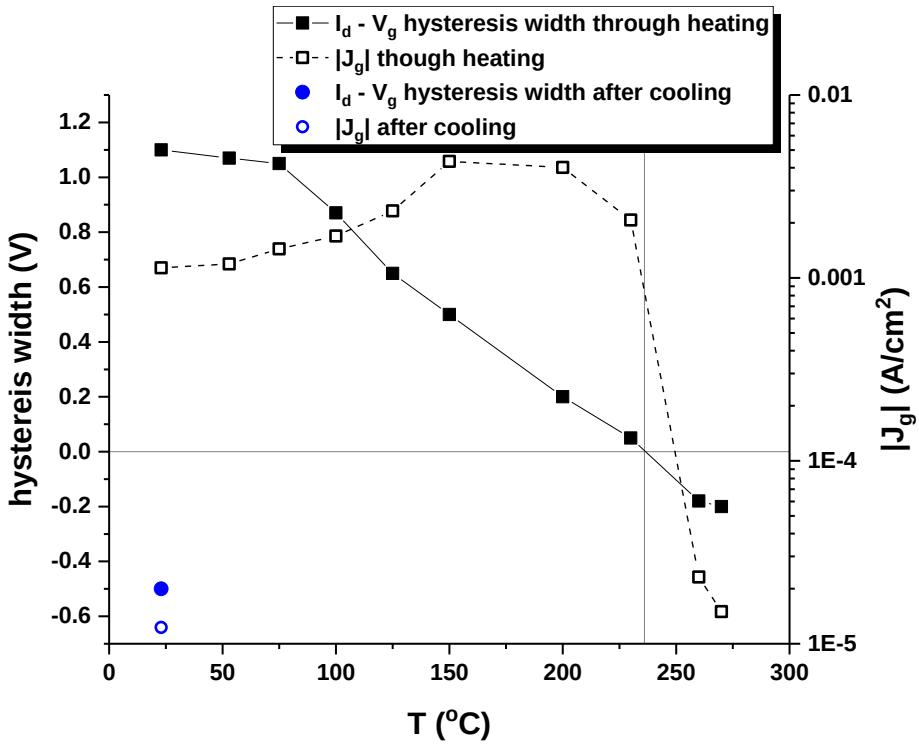

Figure 6.3: Evolution of leakage current density (absolute value of current density at V_g = -1.2 V for each temperature) and I_d-V_g hysteresis width through temperature. CW hysteresis loop is represented with a positive value, while the CCW one with a negative value, horizontal line indicates where hysteresis changes direction and vertical line indicates the temperature at which it happens.

The direction of the $I_d - V_g$ hysteresis loop carries important information on the mechanism responsible for the hysteresis.[37] We note that CCW I_d - V_g hysteresis loops can be linked to a variety of mechanisms: (1) the ferroelectric effect, (2) charge exchange between the metal gate and defect sites in the polymer, and (3) the presence of mobile ions. How these mechanisms can affect the $I_d - V_g$ characteristic curve is described in detail in the following chapter. However, only charge exchange between defect sites near the substrate and the substrate and the polymer (Figure 6.4) results in a CW hysteresis loop.[38] The observed CW hysteresis loop indicates that charge exchange between defects in the polymer and the substrate conduction band overwhelm all the other CCW hysteresis loop mechanisms in the fresh device. The CW loop increases in width as more charge is trapped in the polymer (at defect sites). As shown in Figure 6.4, charge carriers tunnel into the defect site from the substrate and then tunnel out of the defect site to the conduction band (or LUMO band - lowest unoccupied molecular orbital band) and end up at the gate electrode. This trap-assisted tunneling process, in the case of significant trap density, would be the main process supporting the observed gate leakage current. The net captured charge density is the steady-state balance of the two (or more)-step tunneling processes.

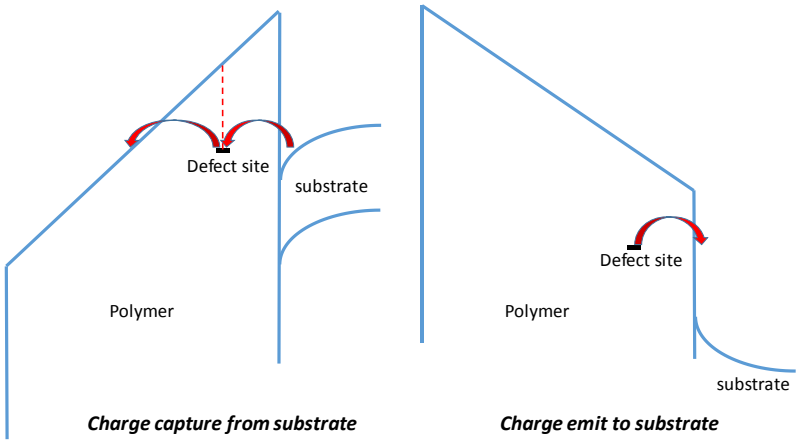

Figure 6.4: Schematic drawing of the device band diagram illustrating the charge capture process.

For polyimides on silicon, the tunnel barrier height is about 2.6 eV (energy gap for polyimides ~7.1 eV, and electron affinity ~ 1.4 eV), [39] whereas for the modified polyimide LaRC-CP1 the barrier height is expected to be lower. The effect of temperature on tunneling probability is higher for a lower barrier height, so one can expect a moderate temperature effect on the tunneling rate for the first step. For the second step, the barrier is significantly lower (the dashed line in Figure 6.4) and the temperature effect is therefore much larger. The net result is that when temperature rises, the second step tunneling rate increases faster than the first step, leading to a lower steady state captured charge density. This is one of the possible mechanisms which may explain the decreasing hysteresis loop width with increasing temperature. Another candidate mechanism could center on a reduction of the net trapped charge difference (between forward and reverse voltage sweeps). It is also quite possible to assume that it is easier for the net trapped charge density to follow the voltage sweep at higher temperatures and approach equilibrium values for both forward and reverse sweeps. This would counteract

the charge difference between forward and reverse sweeps and diminish the hysteresis loop width.

As the temperature continues to rise, the CW loop closes and then transforms into the CCW loop when the net trapped charge (forward and reverse sweep) changes sign. Since the tunneling rate increases with temperature, J_g also increases. Based on this argument, when J_g decreases, as is the case for the measurements between 150 °C and 200 °C in Figure 6.3, the defect density must have decreased. Thus, even though a clear decrease in J_g is only visible at 230 °C, defect annealing began below 200 °C. Given the short time associated with these measurements (≈120 s per temperature point), it is quite surprising to observe such defect annealing below 200 °C.

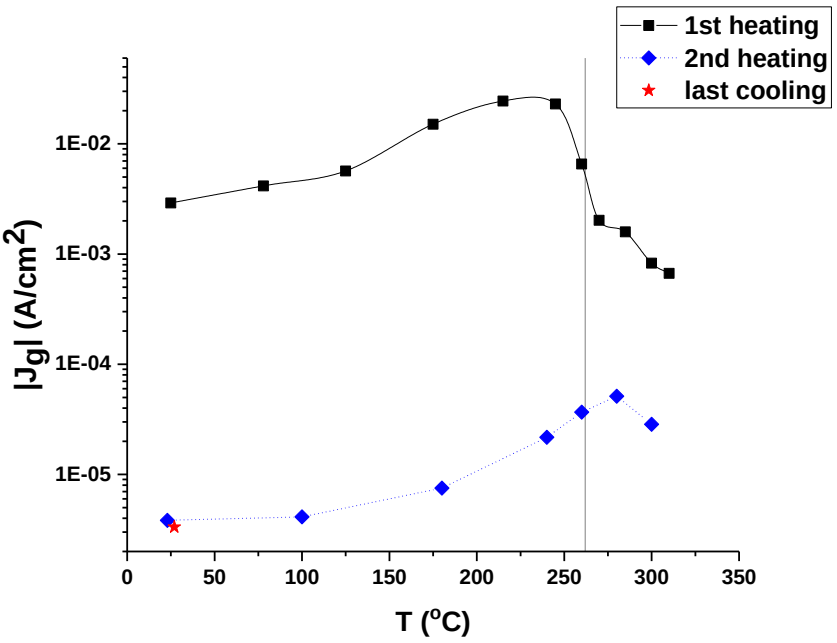

Figure 6.5: Leakage current density vs. temperature in semi-log scale (vertical line indicates temperature at which hysteresis loop changes direction). Device channel L = 3 µm, W = 3 µm.

The observed rapid annealing is reproducible from device to device. Figure 6.5 shows another representative J_g evolution during anneal, obtained from a second device. In this experiment J_g stopped increasing at ≈220 °C and the subsequent J_g decrease is a little less dramatic. However, the fundamental behavior is reproduced. For this device, a second heating cycle after cool down (overnight, at ambient conditions) was performed. The room temperature J_g of the second heating cycle is substantially lower than the room temperature J_g of the first cycle, indicating a much lower defect density after the first cool down cycle. This also rules out the possibility that the J_g decrease was due to driving off moisture during the first heating cycle because the overnight exposure to the air would have recovered most of the water. The second heating cycle does exhibit some minor turnaround at higher temperatures but it nevertheless serves as an indication of the near complete annealing achieved by the first rapid heating cycle.

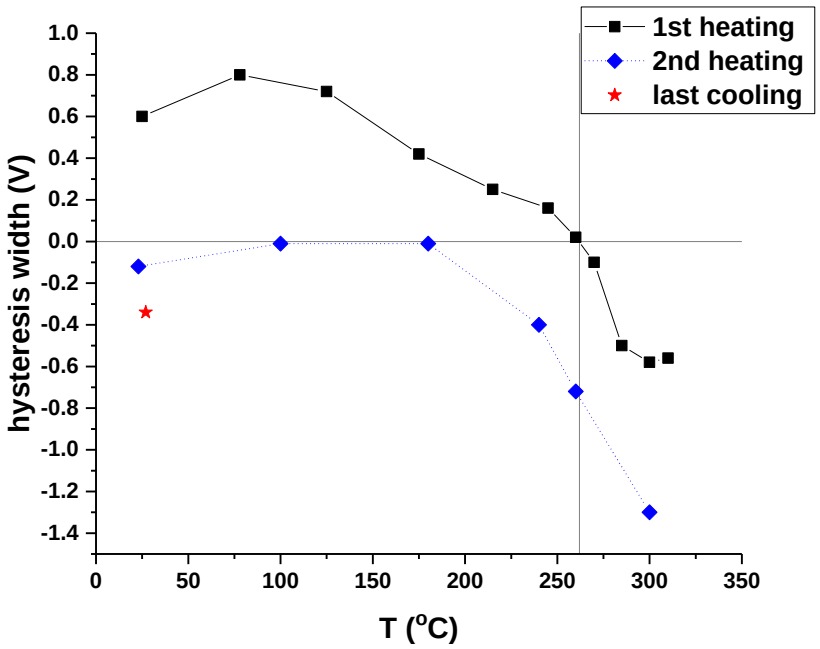

Figure 6.6: Hysteresis width vs. temperature (horizontal line indicates where hysteresis changes direction and vertical line indicates the temperature at which it happens).

An examination of the corresponding $I_d - V_g$ hysteresis lends further evidence of near complete annealing in the first rapid heating cycle (Figure 6.6). During the first heating cycle, the hysteresis loop changed over from CW to CCW. However, it remains CCW for all temperatures during the second cycle. This is consistent with the fact that the defect density remains low after an overnight air exposure.

A CCW hysteresis loop can be caused by the ferroelectric effect, charge exchange between the metal gate and the polymer, or the presence of mobile ions.[37][38] Even with the same defect density, the effect of charge exchange with the metal gate on I_d-V_g hysteresis is much smaller than with the substrate for the following two reasons. The first reason is that the tunnel barrier is higher for the metal gate (Cr work function = 4.5 eV,

and for n-type poly-Si with resistivity of 0.3 Ohm-cm, electron affinity = 4.05 eV). The second reason is that the captured charge is close to the metal/polyimide interface, too far from the substrate to have a significant impact of the flat-band voltage. Furthermore, given that the defect annealing has already taken place, the charge exchange with the metal gate is unlikely to be the cause of the observed CCW hysteresis.

It can thus be said with certainty that the CCW hysteresis at room temperature (the after-cooling points in Figure 6.3 and Figure 6.6) is due to mobile ions because at this temperature dipole rotation is not possible. In other words, the mobile ions are already quite mobile (the $I_d - V_g$ sweep rate is ~ 30 seconds per complete sweep in one direction). As higher temperatures lead to higher mobility for the ions, if the ions are not fully moved from one electrode to the other during the sweep at room temperature, one can expect the CCW hysteresis loop to increase continuously with increasing temperature. This is not the case in the second anneal cycle of Figure 6.6. Indeed, the second anneal hysteresis behavior strongly suggests that dipole rotation becomes possible at temperature > 175 °C and contributes to the increase in CCW hysteresis with temperatures beyond that point.

We note that the dipole rotation and defect annealing start at roughly the same temperature, which makes physical sense, as both phenomena involve movement of atoms in the polymer. However, it is still surprising that defect annealing takes place with such unexpected efficiency. Considering the extreme care taken during the annealing steps of the polymer during fabrication, we are confident that the defect density is very low at the completion of the polymer deposition. The subsequent deposition of the metal

gate and patterning could potentially cause damage to the polymer at the edge of the device. However, we are careful to design the device such that the gate edge overlaps the source and drain (separated by an oxide layer). Thus, damage at the gate edge cannot degrade the device. We therefore speculate that the defects are formed by strain imposed by the metal gate deposition. Similar observations were reported for PVDF.[36] Even though we do not expect thermal expansion mismatch induced stress because the metal film was deposited at room temperature, intrinsic stress can still form by the growth process (e.g. transition from islands to continuous film). It is known that strain can cause chain movement [40][41][42] and therefore introduce defect energy levels in the band gap. We speculate that the strain induced defects are very localized atomic movements. Since annealing of these defects involves highly localized atomic movements, it must be very efficient.

Clearly, the observed rapid annealing of defects cannot be expected to apply to all defect types in the polymer. On the other hand, it may be generally applicable to defects created by stress (provided yield stress has not been reached). This is a highly useful approach for making polymer-based electron devices, such as the FeFET used in this study.

6.2 Conclusion

In summary, we have fabricated FeFETs incorporating a polar polyimide in the gate stack, and we have observed surprisingly efficient annealing of polymer defects at temperatures close or below T_g, well below the melting temperature, T_m. We observed a drastic reduction of leakage current density in such short “low” temperature anneals. The

reduction of defect density was confirmed by the joint behaviors of leakage current density and $I_d - V_g$ hysteresis. This rapid annealing property is believed to be applicable only to defects created by small atomic displacement, such as elastic stress arising from metal contact deposition on the fully cured polymer film. The finding that such defects can easily be annealed is important knowledge for the organic electronics community where polymers are used as gate dielectrics or as insulating layers.

CHAPTER SEVEN HYSTERESIS MECHANISMS

The most common investigated configuration of ferroelectric memory is, as discussed in section 2.3, the ferroelectric field effect transistor (FeFET) with the polar polymer incorporated in the gate dielectric stack. The READ operation of the memory state is performed via monitoring of the transistor current. More specifically, the observation of hysteresis in the drain current -gate voltage (I_d - V_g) characteristics curve is used as proof of the ferroelectric state polarization. However, as it has been pointed out by a number of research groups,[15][43][44][45][46] hysteresis can originate from other mechanisms that are not associated with the rotation of the dipoles in the polar polymer film. These mechanisms that are confounding the proof of the ferroelectric effect include charge-trapping/-detrapping and/or the presence of mobile ions in the polymeric dielectric. Without being able to distinguish the effect of these parasitic mechanisms from the presence of the ferroelectric phenomenon, the polar polymer-bases FeRAM is vaguely demonstrated.

One of the most common arguments used in order to demonstrate the ferroelectric memory effect is that proof of the presence of the ferroelectric effect is the steepness of the jump of the observed hysteresis loop.[15] As it will be shown in this work, charge trapping can create this steep jump at the hysteresis loop for polymer thicknesses common employed. Another common argument that is claimed to differentiate the

ferroelectric effect from the other mechanisms is that the polarization eventually saturates[44] while other mechanisms do not. However, saturation should be expected from charge trapping and mobile ions as well. In reality, proving the observation of ferroelectric switching from I_d-V_g measurements has been less than convincing.

Egginger *et. al.*'s review [38] is an attempt to present all the possible mechanisms to be considered when an I_d-V_g hysteresis is observed on an organic FET (OFET). While this complex work has shown that it is easy to misread hysteresis as proof of the ferroelectric effect and how important it is to differentiate other mechanisms, so far there was no methodical analysis of the effect of each mechanism on the device characteristics and no guidelines to distinguish one mechanism from the other. In this chapter, we systematically show that it is possible to unambiguously differentiate the ferroelectric effect from other sources of hysteresis in polar polymer-based ferroelectric memory cells. Factors such as the direction of the hysteresis loop, the effect of the gate voltage ramp rate, the thickness of the polymer insulating layer, and the symmetry of the hysteresis curves, when considered collectively, allows the unmistakable differentiation of the mechanism responsible for an observed hysteresis loop curve. It is worth to mention that the measurement sequence needs to be carefully controlled to avoid further confusion of the mechanisms. At the end of the chapter, two simple examples are used to demonstrate the methodology. As most reports in the literature use thick polymer layers (on the order of hundreds of nm), the discussion here focuses on unambiguous identification in these samples. In addition, since thin polymer layers are ultimately more technologically relevant, the examples used to demonstrate the methodology enable thin polymer films.

Thin polymer layers add some complications to the discussion; however, their impending technological relevance deems this endeavor worthwhile.

7.1 Characteristics of hysteresis mechanisms

A thorough analysis of the hysteresis producing factors requires a detailed understanding of the underlying mechanisms. Thus, we first present a brief review of each mechanism. Our interest is in how polymer dipoles, charges or mobile ions affect the surface potential of the device channel. The relevant quantity is the flat band voltage shift (ΔV_{FB}) or threshold voltage shift (ΔV_{th}), manifesting as lateral shift of the I_d-V_g curve. During an I_d-V_g sweep, V_{FB} can shift continuously, leading to the observed hysteresis. All of the analysis presented in this section (6.1) is, for simplicity, based on n-type channel FETs, and positive gate bias leads to accumulation. In the case of p-type channel FETs, the negative/positive voltages as well as clockwise/counter-clockwise hysteresis loop analyses, are all reversed.

7.1.1 Ferroelectric effect (Polarization of the dielectric)

When an electric field is applied across a ferroelectric film, a torque acts on the dipoles in the polar polymer which are not already aligned with the field. If the temperature is sufficiently high to permit dipole rotation, they will rotate to align with the applied field. As the dipoles are distributed throughout the polymer layer, the effect is the development of a uniform internal field that satisfies the externally applied field. The rate of dipole rotation depends on the specific polymer chain, the temperature, and the

amplitude of the applied field. When rotation is very slow compared to the observation time, and/or the V_g sweep time, no hysteresis will be observed. However, the remnant polarization of the polymer may not be zero. This affects the location of the drain current transition in the I_d-V_g curve (turning on point, or threshold). When dipole rotation can follow the applied field sweep rate perfectly, the result is also no hysteresis. Note that when sweeping the field between two polarities, the field crosses zero and at that point the dipole rotation rate is also zero. Thus, in theory, the hysteresis will never be zero when the dipoles can follow the field. However, it can be small enough to be considered insignificant. In between these two extreme cases (extremely slow to no dipole rotation and dipoles that can completely follow the field), hysteresis is observed. Since hysteresis is only observed when the dipoles can partially follow the field sweep rate, the shape of the hysteresis loop is unsurprisingly dependent on the measurement details.

Let's start with a sufficient negative bias applied to the gate electrode for a long enough duration to align all the dipoles. Figure 7.1a illustrates how the dipoles inside the polymer will orient. While the dipoles are driven by the sweeping field, the dielectric constant of the polymer becomes higher. The result is that a greater portion of the applied voltage drops across the polymer (gate dielectric) layer than across the depletion layer in the semiconductor substrate. The field inside the polymer as well as at the interfaces becomes higher, leading to stronger band bending in the semiconductor at the interface. Next the gate voltage is swept towards positive values. As mentioned before, the dipoles set up an internal field that satisfies the externally applied electric field. As the applied voltage continues to become less negative, it eventually becomes less than the saturation field and

is no longer balanced by the internal field. As a result, a depolarization field develops and depolarization starts to take place. In other words, the dipoles must reorient to satisfy the new externally applied field. Since the field is swept faster than the dipole rotation rate (dipoles partially follow the applied field), when the applied voltage is zero, the internal field is still negative and the energy bands at the substrate interface still bend upward. The internal field becomes zero (flat band - FB condition) only when the applied voltage has already reached some positive value. Thus, a positive ΔV_{FB} is realized. As the applied voltage continues its sweep toward more positive biases, the dipoles start to align with the positive applied field. At some larger positive applied voltage, the alignment is (approximately) complete. Now the sweep direction is reversed and depolarization begins. Again, since the sweep rate is faster than the rotation rate, depolarization is not complete until the applied voltage has crossed back to negative values, resulting in a negative ΔV_{FB}. The net result is an I_d-V_g hysteresis loop like that schematically shown in Figure 7.1b, where the arrows indicate the direction of the loop (sweep).

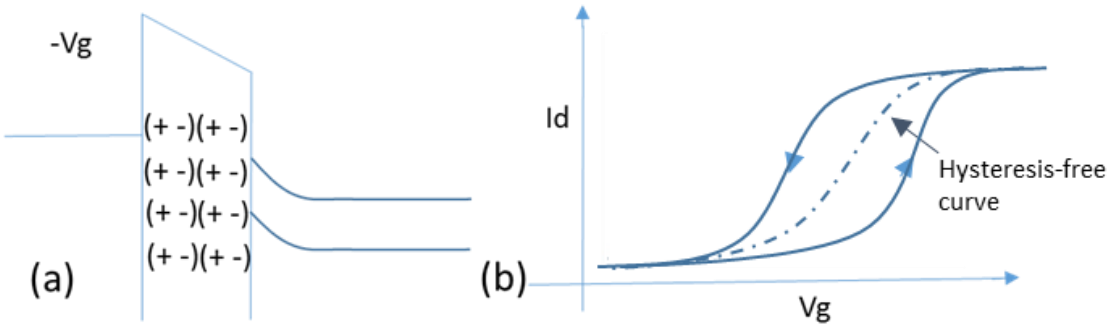

Figure 7.1: Ferroelectric effect on device (a)band bending, and (b)flat band voltage.

The shape of the hysteresis loop is always steeper than the ideal (hysteresis-free) curve because the responding dipoles increase the band bending for a given applied voltage. The abruptness of the hysteresis jump and the width of the hysteresis loop depend upon: (1) the dipole rotation rate as a function of the applied field, (2) the applied voltage sweep rate, (3) the dipole density, (4) the polymer thickness, and (5) the semiconducting channel doping concentration.

For a reasonable experimental sweep rate, the dipole rotation rates that result in hysteresis loops are limited to those active at temperatures near the glass transition temperature (T_g). Thin polymer layers complicate this understanding somewhat as the interface regions can now modify T_g as well as broaden the transition range.[26][47]

7.1.2 Charge-trapping

Due to the relatively small band gap of most polymers,[48][49] both electron and hole injection into the polymer from the semiconductor are highly probable. However, on the gate side only electron injection needs to be considered (since metal gates are commonly used).[15][18] Injected charges can be trapped at defect sites (energy levels inside the band gap of the polymer). These captured charges modify the field distribution inside the polymer in a complex way that is determined by the distribution of the trapped charges. A common method to understand this problem is to find the centroid of the charge distribution and assume that all the charges form a single 2-D sheet of charges located at this centroid location. The effect of the sheet charge on ΔV_{FB} of the transistor is then given by [50][51]:

$$\Delta V_{FB} = -\frac{1}{C_{ox}} \int_0^{x_{ox}} \frac{x}{x_{ox}} \rho(x) dx = -\frac{Q x_C}{\varepsilon A} \qquad (6.1),$$

where C_{ox} is the capacitance of the dielectric (polymer), x_{ox} is the thickness of the dielectric, x_c is the centroid distance from the gate electrode, ρ(x) is the arbitrary distribution of the trapped charge, ε is the dielectric constant of the polymer, A is the area and Q is the total number of trapped charges.

From equation (6.1), it is clear that the location of the trapped charge is important. The biggest impact on ΔV_{FB} occurs when the centroid is located at or close to the polymer/semiconductor interface. The impact decreases to zero when it is located at the gate interface. The negative sign indicates that electron trapping produces positive ΔV_{FB} and hole trapping produces negative ΔV_{FB}. Figure 7.2 schematically illustrate how the sheet charges modify the internal field of the polymer.

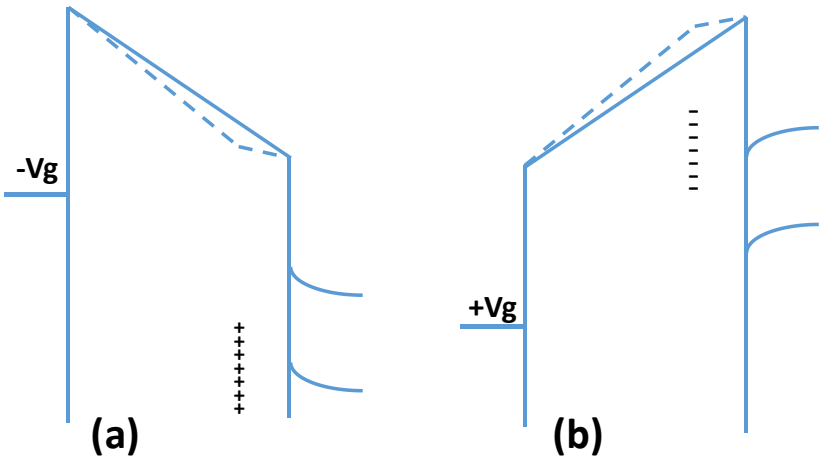

Figure 7.2: Effect of charge trapping on device band bending.

As the centroid of the trapped charge is clearly important, it is most beneficial to first determine the probable location in the polymer film, and then attempt to analyze the hysteretic effects of charge injection. Charge trapping involves electron injection or hole injection via a tunneling process, provided the polymer is of sufficient quality to rule out thermionic emission injection. The distance the electron or hole can tunnel into the polymer is well described by the tunneling front model [52][53]. According to this model, the tunneling time-distance relationship is given by:

$$t = t_0 e^{2x\sqrt{2m(\varphi - E)/\hbar^2}} \qquad (6.2),$$

where t is the time needed to fill traps at distance x, φ is the barrier height, E is the electric field in the polymer, m is the electron effective mass in dielectric, and t_0 is an initial time constant, which is the mean time between electron-phonon collisions. Thus the penetration depth of the injected charge is a logarithmic function of available time for injection. Armed with this formalism, it is instructive to analyze several quantitative examples [53]. For SiO_2 with a barrier of 3.1 eV[54] that is subject to 5 MV/cm electric field, the tunneling depth of injected electrons reaches 2.2 nm in 5 ms, and 2.7 nm in 500 ms. For HfO_2 with a 1.13 eV[55] barrier and the same electric field, the tunneling depth is 9.7 nm in 5 ms and 10.8 nm in 500 ms. So, for realistic barrier heights, where leakage is insignificant, the tunneling depth for realistic measurement times is on the order of 10 nm or less. This means that the centroid will be 5 nm or less from the injecting interface. For a 1 μm thick polymer, the centroid of the trapped charge that was injected from the metal gate side is at least 995 nm away from the channel, while the centroid of the charge that was injected from the semiconductor side is no more than 5 nm away from the

channel. In other words, according to equation (6.1), the charge injected from the gate side is at least 200 times less effective than charge injected from the semiconductor side. Since most reports in the literature utilize these thicker polymers, charge injection from the gate side is considered negligible.

Let's now assume that a sweep measurement starts with negative gate voltage. The band diagram of Figure 7.2a shows that hole injection from the substrate valence band leads to a positive sheet charge somewhere in the polymer, close to the semiconductor interface. This produces a negative ΔV_{FB}. As the gate voltage is swept toward more positive values, charge de-trapping begins. However, de-trapping does not become rapid until the internal field turns positive. The resulting I_d-V_g curve turns on at an earlier voltage than the charge-free characteristic.

As the gate voltage becomes more positive, hole de-trapping gets more efficient and electron injection from substrate conduction band begins (Figure 7.2b). At the positive end of the sweep, a sheet of negative charge is trapped in the polymer near the semiconductor interface resulting in a positive ΔV_{FB}. Now the sweep changes direction towards negative values. Similar to the positive sweep situation, de-trapping is not complete until the internal field is already substantially negative, thus the I_d-V_g curve turns off later than the charge-free case. The net result of the up and down sweep is a hysteresis loop as shown in Figure 7.3. Notice that the loop direction is opposite to Figure 7.1b. This is a characteristic of charge injection from the substrate.

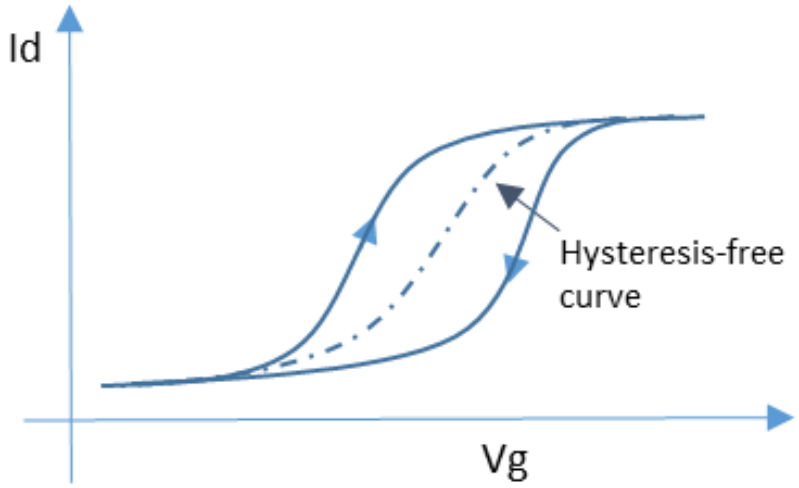

Figure 7.3: Id-Vg hysteresis loop resulting by charge-trapping injected from the semiconductor side.

Although Figure 7.3 shows a hysteresis loop that is symmetric about the charge-free curve, this is not accurate. Assuming the forward and reverse voltage sweep rates are symmetric (not easy to do with the commonly employed semiconductor parametric analyzer), hole injection and electron injection are still asymmetric due to differences in barrier height, defect energy etc. Thus, one should not expect the loop to be symmetric about the charge-free curve. The width and abruptness of the hysteresis loop also depends on several factors. The defect density and energy distribution near the interface affects the size of the I_d-V_g loop. As the gate voltage is swept through the region where rapid trapping and de-trapping occurs simultaneously, one can expect an abrupt jump in the hysteresis curve. The steepness though, depends on the voltage sweep rate, the defect density, the polymer thickness and the transistor design. Since the centroid distance from the interface is a logarithmic function of time, one would also expect strong saturation for thick polymers. So neither abruptness of the jump nor the saturation tendency can be used

to rule out charge trapping as the cause of the observed hysteresis [15],[44]. For thick polymers, only the direction of the hysteresis loop is a discerning factor.

As mentioned above, charge injection from the gate is usually ignored for thick polymer films. However, if the polymer defect density near the gate side is orders of magnitude higher than at the substrate side, gate injection must be considered. Gate injection should also be considered when the polymer is very thin (on the order of a few nm). In cases where gate injection cannot be ignored, the resulting hysteresis loop is in the same direction as the ferroelectric switching. As only electron injection can occur when using a metal gate, the hysteresis loop is always positively shifted. In other words, the loop is entirely on one side of the charge-free curve (Figure 7.4). This feature could be used to distinguish it from ferroelectric switching. The charge-free curve, for the gate injection case, can be approximated by performing a fast gate voltage sweep. During a fast sweep measurement, the tunneling depth reduces, the centroid location moves closer to the gate and the effect of charge injection diminishes. Of course, the charge-free curve can also be predicted theoretically.

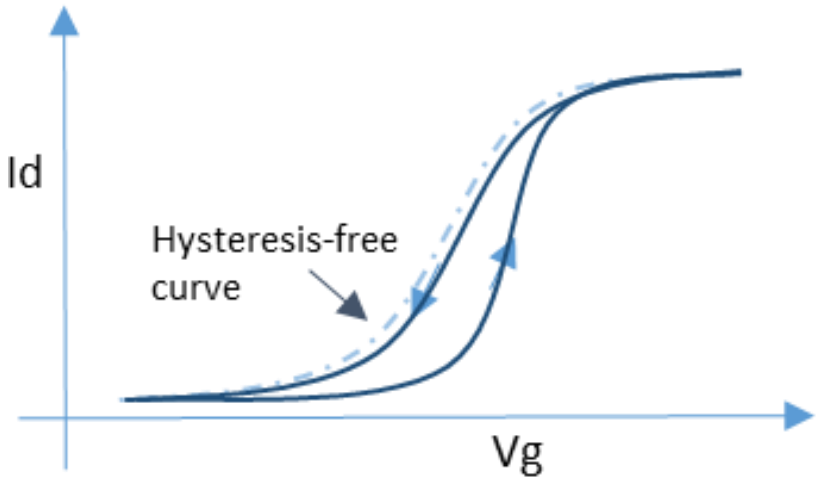

Figure 7.4: I_d - V_g hysteresis loop resulting by charge-trapping injected from the metal gate electrode side.

One more factor that needs to be considered when analyzing charge injection is the measurement sequence control. Most semiconductor parametric analyzers ground the terminal when a voltage is not specifically forced by the program. Thus, in between sweeps or during the change of sweep direction, there is an uncontrolled period of grounding the device under test. As seen in the discussion, grounding the gate leads to de-trapping of charges, positive or negative from the polymer. Assume, for example, that at the beginning of the sweep, the traps are mostly empty instead of fully charged. The traps will be filled instead of being emptied as discussed above. This will produce strange-looking I_d-V_g curves that are difficult to explain. As one sweeps back and forth with an uncontrolled amount of de-trapping during direction change, the resulting hysteresis may even change sign. Even if the terminals are allowed to instead float, the internal field of the polymer still changes drastically and de-trapping can still occur. Most reports in the literature do not give this experimental detail its proper due [15][46][38].

The result is that the I_d-V_g curve can be very misleading. Thus, if the goal is to understand the hysteresis, then one must precisely define the measurement.

7.1.3 Mobile Ions

It is sometimes argued that mobile ions are not important at room temperature because they cannot move [44]. However, it has been shown [45] that mobile ions can move and produce hysteresis in polymeric materials even at room temperature. While the commonly considered mobile ions are positive ions such as Na^+, K^+, Li^+, H^+, negative mobile ions can also exist in polymers such as OH^-. Unlike injected charges that stay near the channel/polymer interface, mobile ions can move through the entirety of the polymer layer under the applied field. Also unlike injected charges, their density does not change with applied bias. So the hysteresis is caused by the relocation of the charge centroid under the applied field only.

We assume that only negative mobile ions are present in the gate polymeric dielectric. Starting with the application of a sufficient positive gate voltage for a sufficiently long time, all the negative mobile ions that are present in the polymeric film are attracted at the gate interface, and so is the centroid. As the gate bias is swept toward less positive voltages, the field still pushes the mobile ions toward the gate, but the distribution will broaden due to Coulombic repulsion between ions acting against a weaker field. This means that the centroid location starts to slowly shift toward the substrate side. As the gate voltage sweeps past zero toward negative values, the electric field changes from pulling against the spreading ions to pushing the ions away from the

gate. At this point, the centroid rapidly moves past the mid-point of the polymer and a positive ΔV_{FB} becomes significant. As the charge centroid continues to move toward the substrate, ΔV_{FB} continue to become more positive, reaching a maximum when all the ions are at the polymer dielectric/substrate interface. Sweeping back towards the positive gate voltage, the process is reversed.

For both mobile ion types (positive and negative), if the sweep rate is very slow the ion distribution is always at equilibrium with the applied field. This will lead to the observation of a hysteresis-free I_d-V_g curve, even though it looks different from the mobile ion-free curve (ΔV_{FB} still happens, just no observed hysteresis). Similarly, if the sweep rate is very fast so that ion movement is negligible before the field reverses direction, no hysteresis will be observed and the I_d-V_g curve resembles the ion-free curve. In between these two extremes, there will be hysteresis. This note indicates that the hysteresis originating from either the ferroelectric effect or the presence of mobile ions can be observed only for a range of field frequencies (or voltage sweep rates). This range of frequencies is, in general, different for either of the mechanisms.

For negative mobile ions, ΔV_{FB} is always positive. Starting from negative gate voltage and sweeping towards positive gate voltage, ΔV_{FB} becomes less positive. Since ΔV_{FB} always lags the voltage sweep, the hysteresis loop will be in the same direction of the ferroelectric switching as shown in Figure 7.5b. Since a one-sided ΔV_{FB} is induced (on the same side of the voltage sweep), the hysteresis loop is not simply a parallel shift of the I_d-V_g curve. An asymmetry as shown in Figure 7.5b is expected.

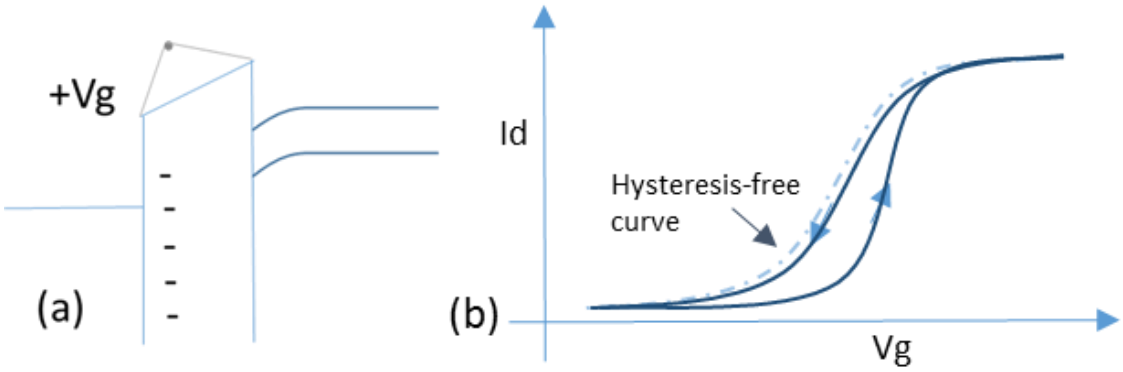

Figure 7.5: band bending and Id-Vg hysteresis caused by the presence of negative mobile ions

For positive mobile ions, the whole discussion just changes sign and ΔV_{FB} occurs at the positive voltage sweep side instead of the negative one. The ΔV_{FB} is always negative, regardless of the sweep direction. When sweeping from positive gate voltages towards negative gate voltages, the charge centroid moves toward the gate and the negative ΔV_{FB} becomes less significant. Since the sweep is faster than the centroid movement, the I_d-V_g curve position, while on the negative side of the ion-free curve, is more negative than when sweeping the other way. The result is again a hysteresis loop with the same direction as the ferroelectric switching and a-symmetrical (Figure 7.6b).

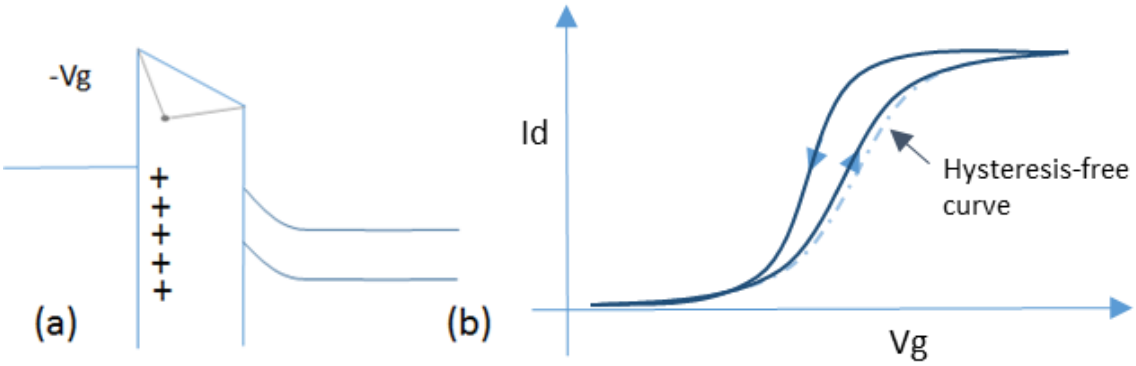

Figure 7.6: band bending and I_d-V_g hysteresis caused by the presence of positive mobile ions.

Of course, positive and negative mobile ions can exist in the polymer at the same time. Na^+ concentration can dominate as happens with inorganic dielectrics, however metallic ions (cations) diffusing away from the electrodes might also be present. OH^- and other anions can be present as well, when precursors such as the group of carboxylic acids are used for the polymerization. However, it is highly unlikely that they exist in equal concentrations or have similar mobilities. Thus, even if they exist in similar concentrations, the sweep rate dependent behavior will not be the same. Only in very rare situations, the concentration and mobility of both types of ions balance to result in a symmetric hysteresis loop and confounds identification of ferroelectric switching. For the rare case when both types of mobile ions coexist and their concentration ratio and mobility ratio just happen to result in the same shape of hysteresis as the ferroelectric effect, additional measurement such as triangular voltage sweeps (TVS) [56] will be required to further pinpoint the cause, even though it may require the fabrication of larger area test devices for TVS measurement.

The shape of the hysteresis loop can clearly lead to saturation when the concentration and mobility of the mobile ions are compatible with the sweep rate. As mentioned above, charge trapping can also lead to saturation, the claim that current saturation is an indication of ferroelectric polarization [44] is clearly not justified.

An argument used in literature [57] claims that the device frequency response can be used to differentiate the ferroelectric from the mobile ions mechanisms. Given the discussion above, this is not possible without prior knowledge of how mobile ions and ferroelectric polarization respond to sweep rate at given temperatures. As such prior knowledge is rarely available, this method is not practical.

At this point we should mention that mobile ions can not only be present in the polymeric dielectric, but also in the device channel. In this case, the mobile ions can either be pulled close to the dielectric/semiconductor interface or pushed farther away in the channel. The ions affecting the flat band voltage are, again, those close to the interface. Since these mobile ions are located in the channel region (on the other side of the interface), their response to the gate voltage is opposite to that of those in the dielectric. In other words, the application of a negative gate bias pulls positive mobile ions toward the interface while the application of a positive gate bias pulls negative mobile ions toward the interface. This means that for positive mobile ions, a negative ΔV_{FB} appears when sweeping the gate voltage from negative toward positive voltages. For negative ions, a positive ΔV_{FB} appears when sweeping the gate voltage from positive voltages towards negative voltages. According to the above discussion, one would expect

the channel mobile ion (negative or positive) hysteresis loop is always clockwise. This is opposite to the hysteresis direction of the ferroelectric switching as shown in Figure 7.1.

7.1.4 Summary

Summarizing the discussions and arguments made above, it has been shown that the observed shape, position and direction of the hysteresis loop contains very specific information to remove various potential factors that confound the confirmation of ferroelectric switching, at least for thick polymer dielectrics. However, the measurements must avoid undefined states (hold time). This important control is largely overlooked in the literature, contributing to much of the confusion. For rare cases, such as, when both positive and negative mobile ions coexist and their concentration ratio and mobility ratio happen to produce a hysteresis that resembles the ferroelectric switching, the unique identification becomes more challenging.

7.2 Demonstration of the methodology

Since thin polymer films are more desirable for low voltage operation, our methodology to identify ferroelectric switching will be demonstrated on junction-less FeFETs with thin (15 nm) polar polymer dielectrics. The FeFETs were fabricated on fused silica substrates. 15 nm thick LPCVD n-type poly-Si layer forms the channel and a spin cast 15-nm thick LaRC-CP1 polar polymer film serves as the gate dielectric. Figure 7.7 schematically illustrates the fabricated device layout and cross-sectional views. The details of the device and fabrication are described in the experimental section. The chosen

polymer has a glass transition temperature (T_g) of ≈260 ^oC and ferroelectric switching is not possible at room temperature at any realistic gate voltage sweep rate. In this demonstration, we discount the role of any channel mobile ions. Since the channel consists of a poly-Si layer grown in a high purity LPCVD furnace, the mobile ion concentration is expected to be extremely low. In examinations of deposited organic channel materials, this mechanism should be considered.

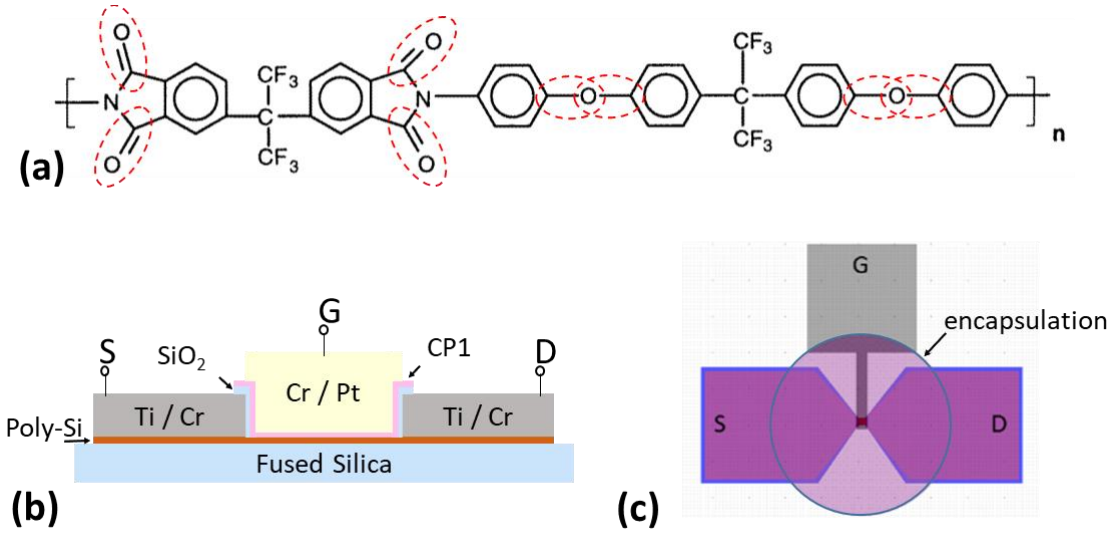

Figure 7.7: (a) LaRC-CP1 chemical structure, and fabricated devices cross-section (b) and layout (c).

7.2.1 Case #1

A sinewave voltage (V_{gs}) was applied at the gate terminal while the current through the device channel was monitored at a drain bias of 1.6 V (source grounded). The sine wave amplitude extended from -3 V to +3 V at various frequencies in the range 0.1 Hz to 100 Hz. Thus, at the drain end of the channel, the voltage across the polymer varies

from -4.6 V to 1.4 V while at the source end from -3 V to +3 V. The sine wave is continuous and the I_d-V_g characteristics were recorded by using a digital storage oscilloscope. This experimental setup results in highly repeatable measurement conditions with no unknown hold times at any point of the voltage sweep. As discussed above, this is an important factor for the interpretation of the results. The I_d-V_g curves were averaged 20 times, to measure the steady state shape of the hysteresis characteristics. This approach is particularly useful when sweeps do not reach saturation in one or both sweep polarities. Since the polymer is thin, saturation may require electric fields above breakdown. With this added complication, ensuring steady state hysteresis characteristics greatly aides the interpretation of results. All measurements were performed at room temperature.

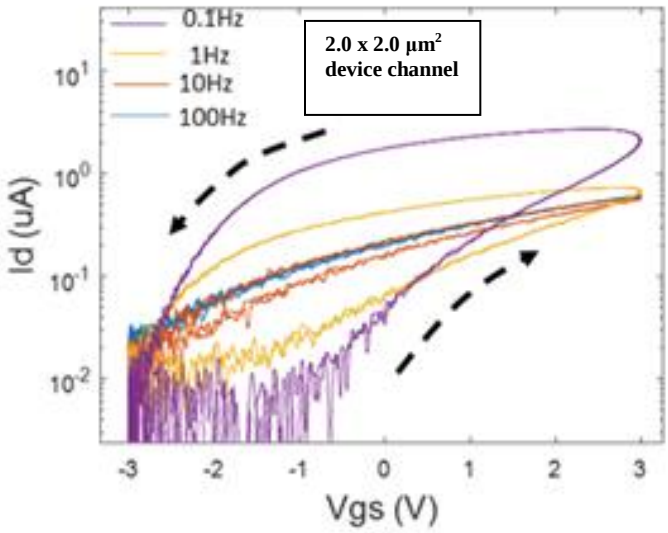

Figure 7.8: Id-Vg hysteresis at corresponding frequencies

Figure 7.8 shows the observed I_d-V_g hysteresis loops for four different sweep rates. Since this is a high T_g polymer, ferroelectric switching does not take place (at room temperature) for these measurements. The remaining factors which contribute to hysteresis are therefore charge trapping and mobile ions. From the direction of the hysteresis loop (counter-clockwise), charge-trapping due to injection from the substrate side (both electrons and holes are considered) can be ruled out as the cause of the observed hysteresis. This is not to say that there is no substrate charge injection, it just does not dominate the observations. As discussed above, charge-trapping due to gate injection can generally be ignored for thick polymer gate dielectrics. However, with the polymer film being ≈15 nm thick, we must consider gate injected charge-trapping, mobile ions, and the possibility of both existing simultaneously.

Upon inspection of Figure 7.8, we notice that the fastest loop (100 Hz) is practically hysteresis-free while all others exhibit clear hysteresis. However, the 10 Hz loop (the next slower one after the 100 Hz loop) appears to expand only on the positive side (more positive voltages, positive ΔV_{FB})) of the 100 Hz loop. From the discussions above, two potential sources for this behavior can be identified: electron-trapping by gate injection; and the presence of negative mobile ions. For gate injection at 100 Hz, the trapped charge centroid is very close to the polymer/gate interface and therefore hysteresis is too small to be resolved. At the slower sweep of 10 Hz, the centroid moves deeper into the polymer. This movement increases ΔV_{FB} and leads to an observable hysteresis. Similarly, for negative mobile ions, a 100 Hz voltage sweep is too fast for them to follow. At 10 Hz, some degree of following occurs. As the two factors have the

same impact, they cannot be differentiated. The 1 Hz and 0.1 Hz loops not only get larger, but also they no longer stay on the positive side of the 100 Hz curve, suggesting a new factor is now contributing to the negative ΔV_{FB}. This can be explained by the presence of positive mobile ions, meaning that the 1 Hz sweep is slow enough that positive mobile ions start to introduce their voltage shift. This indicates that the positive mobile ions are less mobile than the negative mobile ions. The much larger 0.1 Hz loop suggests that 1 Hz is still somewhat too fast.

The dependence of the extracted hysteresis voltage vs. period of applied sinewave V_{gs} signal is shown in Figure 7.9 with an inset in semi-log scale. The observed rapid increase and then saturation at longer periods is consistent with mobile ions and that they reach the substrate interface. There cannot be any doubt that both negative and positive ions contribute to the hysteresis curves. One cannot, however, conclude the presence or absence of charge trapping by gate injection.

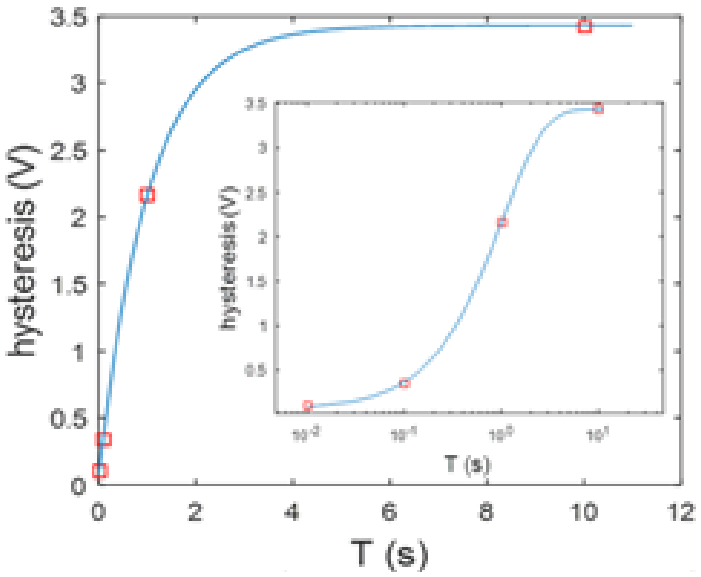

Figure 7.9: Hysteresis width development with signal period

It is seen that compared to the rest of the frequencies, the 0.1 Hz loop exhibits higher current values at the positive extreme and lower current at the negative extreme. (A hint of this behavior can also be obtained from the 1 Hz loop). For slower sweeps, the effect of gate injection and mobile ions continue to increase (till they inevitably saturate). At the positive extreme, positive mobile ions have more time to move close to the semiconductor interface producing more positive effective gate voltage, which eventually leads to higher drain current. At the negative extreme, electron injection from the gate as well as the movement of negative ions close to the channel, results in more negative effective gate voltage, leading to lower drain current. However, mobile ions still dominate the cause of observed hysteresis.

7.2.2 Case #2

In case #1 the analysis was simplified by two factors: the known absence of ferroelectric switching at room temperature (measurements performed well below T_g) and the dominant role of mobile ions. In case #2 these two factors are removed. In this second example, another device is measured, of the same design using the same polar polymer (Figure 7.7). The resulting hysteresis loops of this device are much more narrow than that in the first case, indicating the mobile ion concentration is much lower and no longer complicates the analysis. The difference in the mobile ion concentration, and consequently in the hysteresis loop width, is due to the relatively large sample to sample variations present in the fabrication process. Ferroelectric switching is added to the possible mechanisms via analysis of $I_d - V_g$ hysteresis loops versus temperature (Figure 7.10). All I_d-V_g sweeps are performed while the drain is biased at 1 V and the source is grounded. This device initially exhibits a clockwise hysteresis (CW) loop direction at room temperature. This means that the dominant mechanism can only be the charge–trapping due to charge injection from the semiconductor side. Upon temperature increase, the hysteresis loop becomes smaller and smaller, and eventually reverses to a counter-clockwise orientation when reaching T_g. The decrease in the width of the clockwise hysteresis loop suggests that the trapped charge density is decreasing for both forward and reverse sweeps. The change of the hysteresis loop direction indicates a change in the dominant hysteresis mechanism.

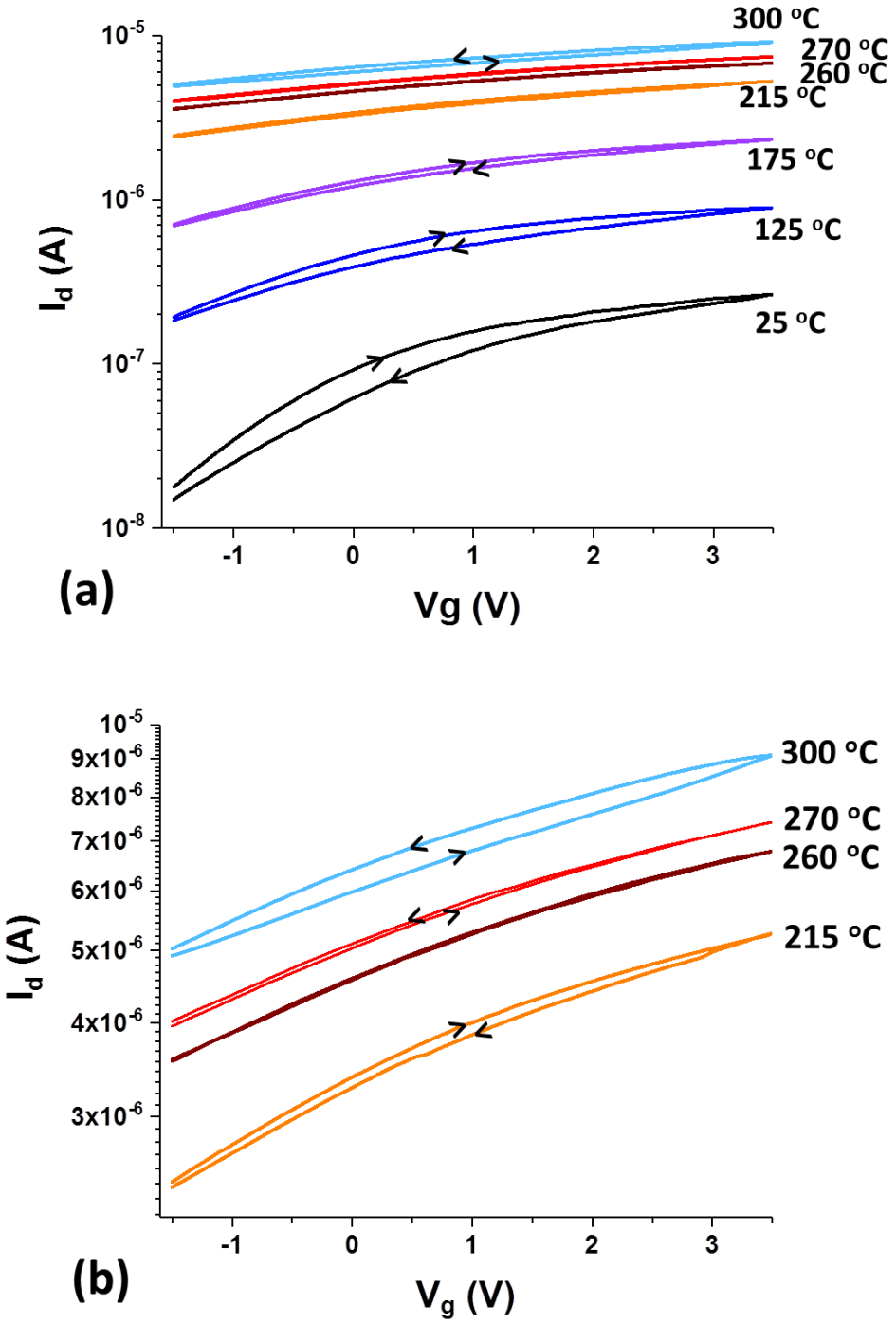

Figure 7.10: I_d - V_g characteristics during a heating cycle

The new dominant mechanism must explain the now counter-clockwise hysteresis loop direction (CCW). Charge injection from the gate side, mobile ions and ferroelectric switching are all possible candidates. If one assumes the defects responsible for charge-trapping at the gate side of the polymeric dielectric are the same as those at the semiconductor side, gate injection can be ruled out because the defects will affect both semiconductor injection and gate injection equally – they would decrease together and therefore charge injection from the gate side cannot explain the change of direction. On the other hand, how can one be sure that a decrease in defect density is responsible for the decrease in the clockwise hysteresis for increasing temperature? An auxiliary measurement of gate leakage current provides the insight as shown in Figure 7.11 where the leakage current and the hysteresis width are plotted as a function of temperature. It is well known that gate leakage, particularly for polymer gate dielectrics, increases with temperature due to the phonon- and trap-assisted tunneling mechanisms. This is also borne out in Figure 7.11. The increase in gate leakage slows at ≈150 ^{o}C, peaks, and then begins to decrease before reaching 250 ^{o}C. This can only be explained by the assumption that the decrease in trap density is larger than the offset increase in phonon-assisted tunneling probability with increasing temperature. As the temperature approaches T_g, defect annealing becomes more efficient. This is seen as a rapid decrease in leakage current beyond 230 ^{o}C. More clues can be revealed through an examination of a second heating run (after cooling) where the lower temperature leakage is three orders of magnitude lower. This suggests that the defects have been annealed. The leakage current at room temperature after the final cooling and that at the beginning of the second heating

cycle are almost the same (first filled diamond point and filled asterisk in Figure 7.11), indicating that the defect annealing has been saturated during the second heating cycle.

The trend in hysteresis width (Figure 7.11) supports the argument that charge-trapping from semiconductor injection is responsible for the clockwise loop at room temperature and that the decrease in loop width is caused by a decrease in defect density. The leakage current analysis suggests that the defect density starts to decrease at <150 C, which roughly coincides with the hysteresis decrease. At higher temperatures, the defect density (as indicated by the leakage current) and hysteresis width have similar dependencies. The link between the CW hysteresis and defect density is thus firmly established.

The remaining two factors, ferroelectric switching and presence of mobile ions, can also be differentiated from Figure 7.11. At the beginning of the second heating cycle, the hysteresis is already counter-clockwise. At this temperature, dipole switching is not possible. The hysteresis must be the result of mobile ions over-compensating charge-trapping from injection from the semiconductor side. As the temperature increases, hysteresis (due to mobile ions) should either increase (more negative) or remain constant (saturated). However, Figure 7.11 shows a mild decrease (less negative). This suggests that the mobile ions are saturated and the mild decrease is due to a mild increase in charge-trapping from semiconductor injection. This is in full agreement with the mild increase in leakage during the second heating cycle. Note that the defect density remains constant during the second heating cycle as evidenced by the small decrease in leakage current after the sample has cooled. The most interesting result in Figure 7.11 is the rapid

increase in hysteresis (more negative) >175 ^{o}C. At this point, the leakage current is still increasing. The only possible explanation for the hysteresis increase is ferroelectric switching. Again, the post second cycle room temperature hysteresis offers further evidence. The hysteresis width is more negative than at the beginning of the second heating cycle, consistent with the additional small decrease of the defect density.

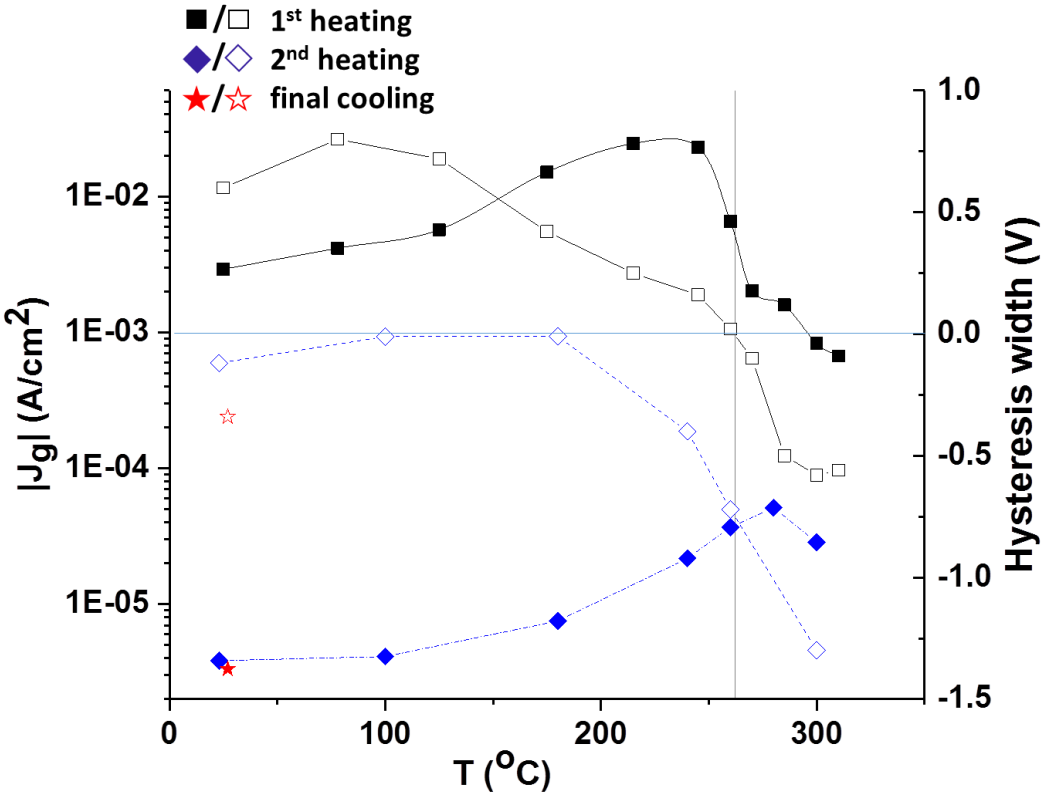

Figure 7.11: Leakage current density (filled symbols - absolute value of current density at V_g = -1.2 V for each temperature) and hysteresis width (open symbols – largest hysteresis width of I_d-V_g loop) development though temperature. Clockwise hysteresis loop is represented with a positive value, while the counter-clockwise one with a negative value, the vertical line indicates the temperature at which the hysteresis loop changes direction during the first heating cycle.

7.3 Conclusion

In this chapter, we demonstrate a systematic and logical methodology to differentiate the ferroelectric effect from other mechanisms present in polar polymer based ferroelectric FETs that can also cause $I_d - V_g$ hysteresis, namely charge injection and trapping and the presence of mobile ions in the polymeric dielectric. It is shown that careful analysis of the hysteresis loop direction, dependence of hysteresis width on gate voltage ramp rate and device temperature, thickness of the polymer insulating layer, and the symmetry of the resulting hysteresis curve can greatly aid in deconvoluting complicated FeFET hysteresis. The method is quite simple for thick polar polymer gate dielectrics. For thin polar polymers, auxiliary measurements of gate leakage may be needed to fully reveal the dominant hysteresis mechanisms. The utility of the methodology is demonstrated in high T_g polar polymer-based FeFETs. In these examples, it is shown that charge trapping and mobiles ions dominate the detected hysteresis at room temperature, while the ferroelectric polarization effect is observed at elevated temperatures. Our methodology can help differentiate the ferroelectric effect induced hysteresis from the other parasitic mechanisms, and unambiguously prove the presence of ferroelectric polarization.

CHAPTER EIGHT GERAM DEMONSTRATION

Ferroelectric random access memory devices (FeRAM) incorporating a polar polymer in the gate dielectric stack of a FeFET have attracted significant research interest in the last decades. [15],[18],[19],[21] While FeRAM is designed to be non-volatile, the reported memory retention time of polymer-based FeRAM is not much longer than a few days.[14],[15],[21],[22],[23] This is significantly shorter than the ten years' time that is needed for mainstream adoption. The main causes that reduce the retention time are depolarization fields, leakage current through the polymeric dielectric,[14] and mobile ions. Mobile ions are a material purity/fabrication issue and therefore not intrinsic. The leakage current may be reduced by inserting additional buffer layers in the gate dielectric stack and/or careful choice of the operation voltage range through device optimization. However, the depolarization field is the result of incomplete charge compensation in the semiconducting substrate that forms the transistor channel and is therefore a universal intrinsic problem.[14]

Common organic FeRAM reports detail the use of polar polymers with sub-room temperature T_g as the gate dielectrics.[19],[22] This sub-room temperature T_g is required to minimize the programming voltage for room temperature operation. Problematically, the same dipoles that are polarized by the electric field during programming are also subject to a depolarization field during operational biasing conditions, which leads to less

desirable retention times. This is commonly overcome by recognizing that the dipole rotation speed is a function of the applied electric field (in other words, the applied voltage across the dielectric film thickness). Thus, very high electric fields are often used during programming to force a fast dipole rotation.[58] During subsequent retention measurements, the gate electrode is grounded which results in a comparatively smaller, yet non-zero, depolarization field to the polar polymer. This field acts to slowly depolarize the state and ultimately limits the non-volatility of this class of memories. This is often observed as a long decay of the memory state.[21],[22]

Even with the above-mentioned challenges, reports present retention to programming time ratios of 7 orders of magnitude.[17][19] Using careful control of programming time under the high programming field, even multi-state memory has been demonstrated.[59],[60] However, since these achievements are accomplished by cleverly taking advantage of electric field-dependent dipole rotation rates, they are not directly applicable to real applications where memory cells are configured in two-dimensional arrays. In such arrays, about half of the voltage applied to program or read a cell will appear across all the cells in the array. This causes the well-known program disturb and read disturb phenomena. In other words, the memory states of all cells in the array will be altered by programming or reading of any of the rest of cells sharing the bit or word lines. Frequent access (reading or writing) of memory cells in the array leads to repeated disturbs that quickly destroy the memory states. While, to our knowledge, no one has addressed the disturb issue for organic ferroelectric memory, the intrinsic weakness of the current organic ferroelectric memory will prevent it from finding real application.

The above-mentioned problem stems from the reliance on leverage of field-dependent dipole rotation rate in all the reported organic ferroelectric memories. The new memory concept presented herein leverages a different dipole rotation control, by taking advantage of the well-known fact that the rate of dipole rotation, for a given electric field, is also a strong function of temperature. Above melting temperature (far exceeding T_g), dipole rotation is extremely rapid even in presence of very weak fields. At temperatures far below T_g, dipole rotation is extremely slow even when high fields are applied (> polymer breakdown field strength). Thus, the proposed organic FeRAM uses polar polymers with T_g well above the operation temperature (room temperature in the current study) and relies on thermal-assisted programming to attain high speed. The operation concept is as follows: To enable fast programming, the polymer is *momentarily* heated to a temperature well above T_g while the programming field is applied. The temperature is held only long enough for the dipoles to respond to the applied programming field. The polymer is then allowed to cool quickly back to near operation temperature while the programming field is held. Once cooled, the polarization state is "locked in". In other words, at room temperature, the dipoles will not rotate even under strong electric fields. Thus, the programmed states cannot be altered by program disturb, read disturb, or the depolarization field. Higher programming temperatures needed for shorter times, which decreases the cool down time. This corresponds to smaller heated volumes and less energy consumption. Thus, this new FeRAM concept is inherently suited for efficient fast operation.

For demonstration, a memory device consisting of a junction-less thin film FeRAM using a thin, high T_g, polar polymer (LaRC-CP1) as the gate dielectric was fabricated. It should be noted that, although prior works report memory devices using high T_g polymers,[61],[62] these efforts were not concerned with ferroelectricity, were often programmed at room temperature, and therefore largely different from the proposed memory technology.

8.1 Device and material Characteristics

Figure 8.1 shows the chemical structure of the high-T_g polar polymer LaRC-CP1[25] used in this study (a), the device cross-section (b), as well as the drain and the gate leakage current (c, d) of the fabricated junction-less FeFET device. While the gate leakage current for a 15-nm polymer film is very low, the ON-OFF ratio of the transistor is poor – reflecting a non-optimized device. Since repeatable gate modulation of the drain current is achieved, it is sufficient for the concept demonstration intended here. Notice that the I_d-V_g hysteresis is almost non-existent in Figure 8.1c, as should be the case for measurement at room temperature when the dipoles of the high-T_g polyimide are locked in their position. This is also an indication that charge-trapping and mobile ions do not play dominating roles in these devices.

The thermally-assisted programming concept only calls for heating during programming. This means that the temperature excursion should be very brief. In this, somewhat rudimentary, demonstration, the temperature is controlled by a miniature (30

mm diameter) wafer chuck. Optimization of the ramp-up/ramp-down times still leaves the device at programming temperatures for close to 1 min.

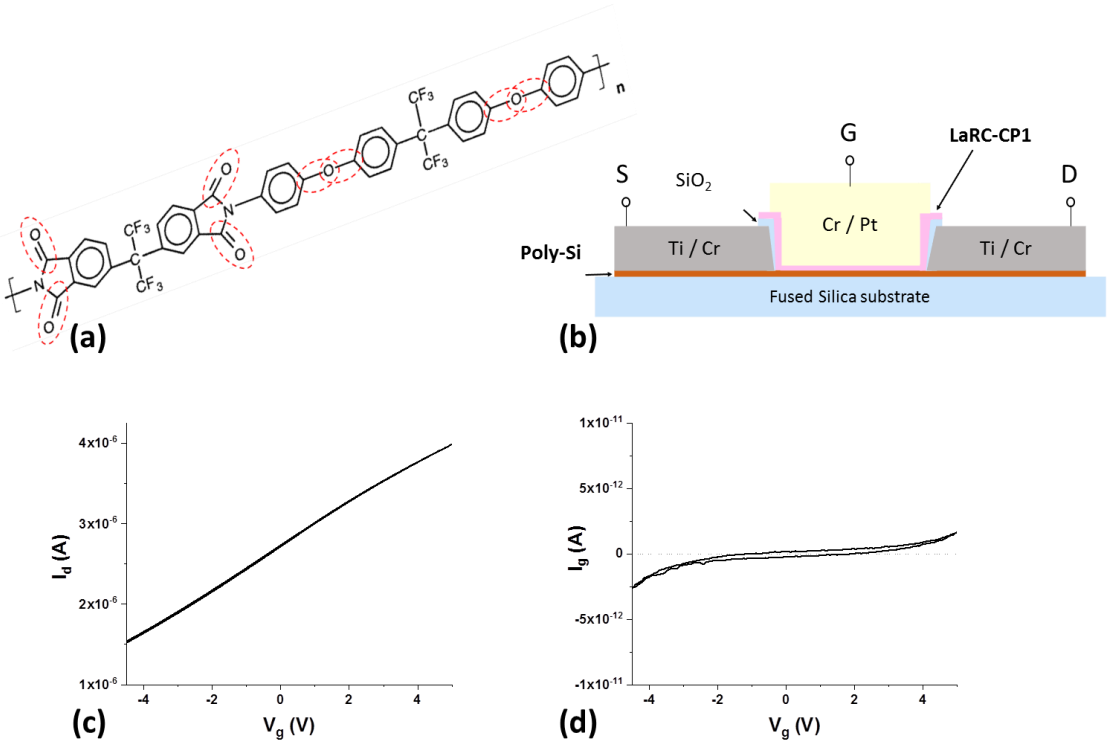

Figure 8.1: a) Chemical Structure of CP1 Polyimide molecule. Dashed ovals designate the dipoles believed to contribute to the ferroelectric effect. b) Schematic cross-section of the device structure. c) I_d-V_g, and d) I_g–V_g characteristics for a device with channel L = 2.5 μm and W = 2.5 μm.

Figure 8.2 shows dielectric spectroscopy measurements detailing the frequency response of LaRC-CP1 (from a fabricated metal-polymer-metal capacitor, details discussed in section 4.2) as a function of temperature. Figure 8.2 also shows the responses of three other polar polymers taken from literature reports.[63],[64],[65] Each set of data is plotted in log-log scale and fitted to a straight line spanning 10 orders of magnitude to demonstrate that dipole rotation rates are indeed strongly dependent on

temperature. The slope of the line, as expected, is polymer specific. One might question the validity of such an extended extrapolation. However, we note that the reported viscosity of chalcogenide glasses vary smoothly as a function of temperature over 17 orders of magnitude. The reported viscosity/temperature dependence was not quite exponential (viscosity decreases somewhat faster than exponential for decreasing temperature). [28] Using this reported behavior as a reference, the exponential extrapolation presented in Figure 8.2 is both justified and possibly even overly pessimistic. It is also clear from Figure 8.2 that CP2 is somewhat better than CP1 because it requires a much smaller temperature change to span the same frequency range. However, CP1 was chosen as the subject of this work due to the commercial unavailability of CP2.

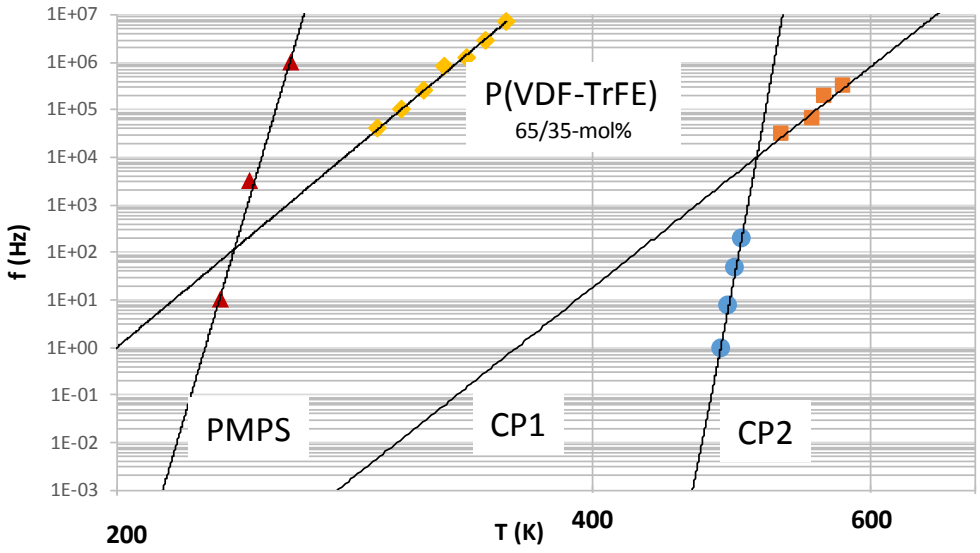

Figure 8.2: Frequency response versus temperature (corner frequencies corresponding at various temperatures).

8.2 Polarization of the ferroelectric device, and proof of ferroelectric effect

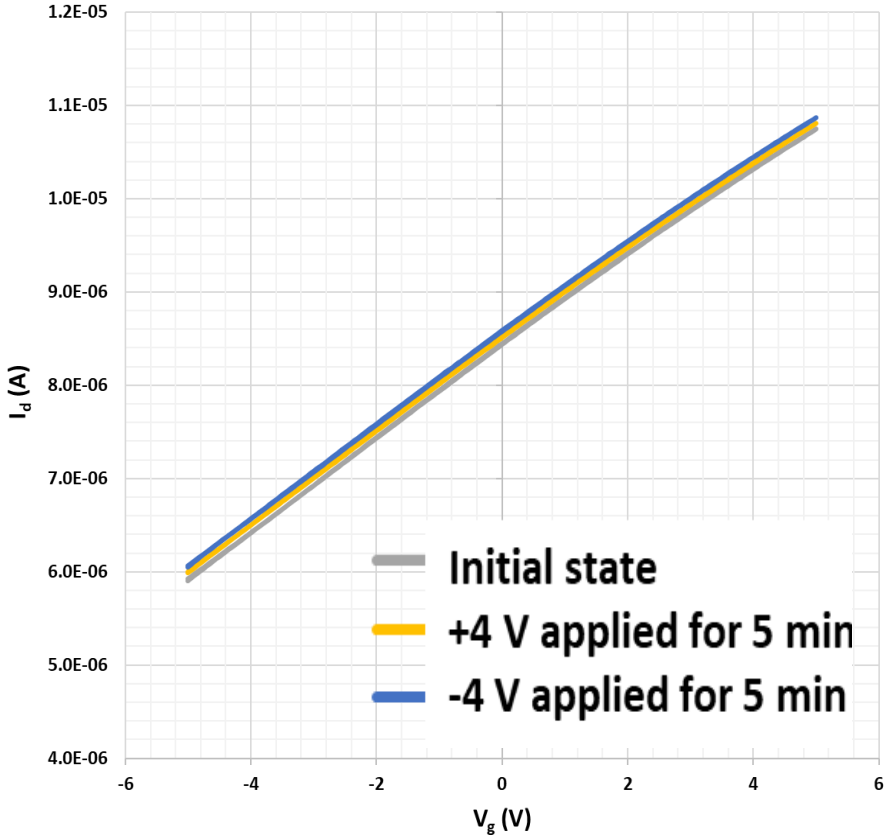

Figure 8.3: Attempt to program the device at room temperature

At room temperature, attempts to program the device resulted in negligible change to the polarization state of the device as shown in Figure 8.3. However programming at 275 ^{o}C (≈ 15 ^{o}C above T_g), resulted in an polarity-dependent flat-band voltage shift confirming state changes (shown in Figure 8.4). At this elevated temperature, LaRC-CP1 supports dipole rotation frequency up to 300 kHz (according to data of Figure 8.2). Compared to the ~ 1-min programming time, there is clearly

sufficient time for dipole rotation to satisfy the electrostatic field established by the applied voltage. Before one concludes that this is the result of dipole rotation, other possible causes such as charge-trapping and mobile ions must first be discounted.

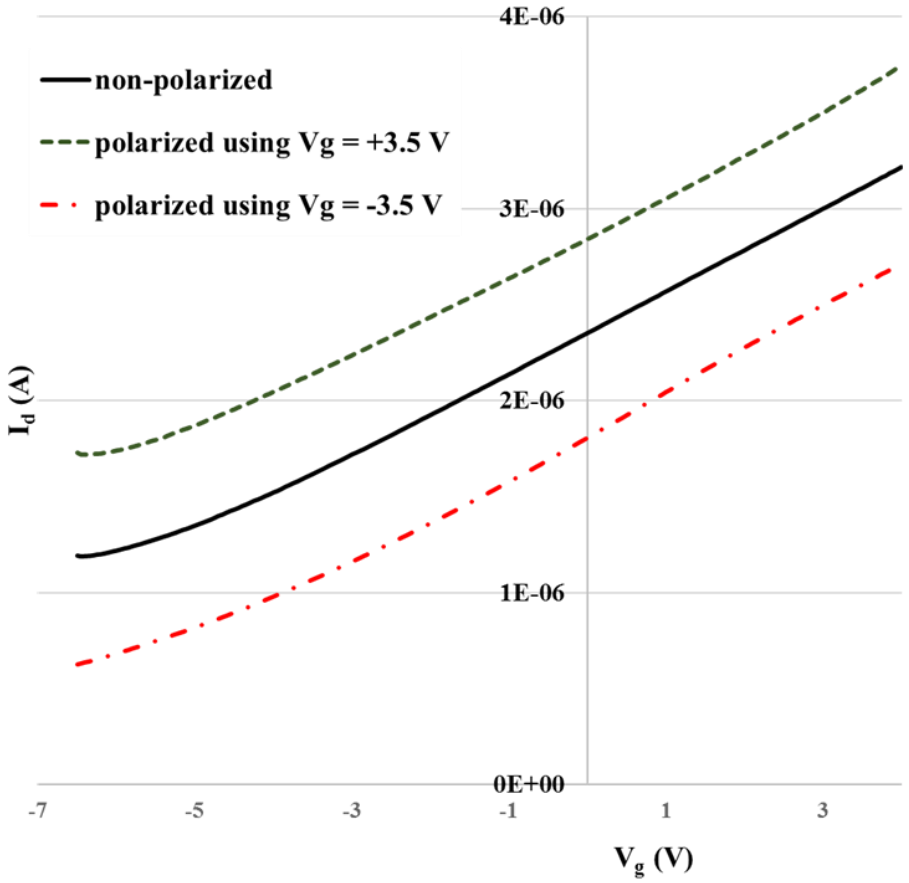

Figure 8.4: $I_d - V_g$ characteristics of a 2.5 x 2.5 μm^2 device in the unpolarized state (solid line), positively polarized using a positive bias of 3.5 V (dashed line), and negatively polarized using a negative bias of 3.5 V (dashed dot line).

To clearly show how charge-trapping and mobile ions affect the device, we choose another device (on the same wafer) that showed hysteresis in the room temperature I_d-V_g characteristic. The approach is to analyze the gate leakage current and

the hysteresis as a function of temperature during anneal cycles. Figure 8.5a shows the hysteresis and I_d - V_g behavior as a function of temperature during the temperature ramp up. Figure 8.5b replots the high temperature range to make the change of hysteresis loop direction clearer. This device initially exhibits a clockwise hysteresis loop at room temperature indicating that the dominant mechanism can only be the charge–trapping due to charge injection from the semiconductor (mobile ion and dipole rotation lead to counter-clockwise hysteresis). As temperature rises, the hysteresis loop decreases in size, and eventually switches to a counter-clockwise direction when reaching T_g. Figure 8.6 summarizes this hysteresis behavior as well as the corresponding gate leakage current as a function of temperature for two complete anneal cycles. All I_d - V_g sweeps are performed while the drain is biased at 1 V and the source is grounded.

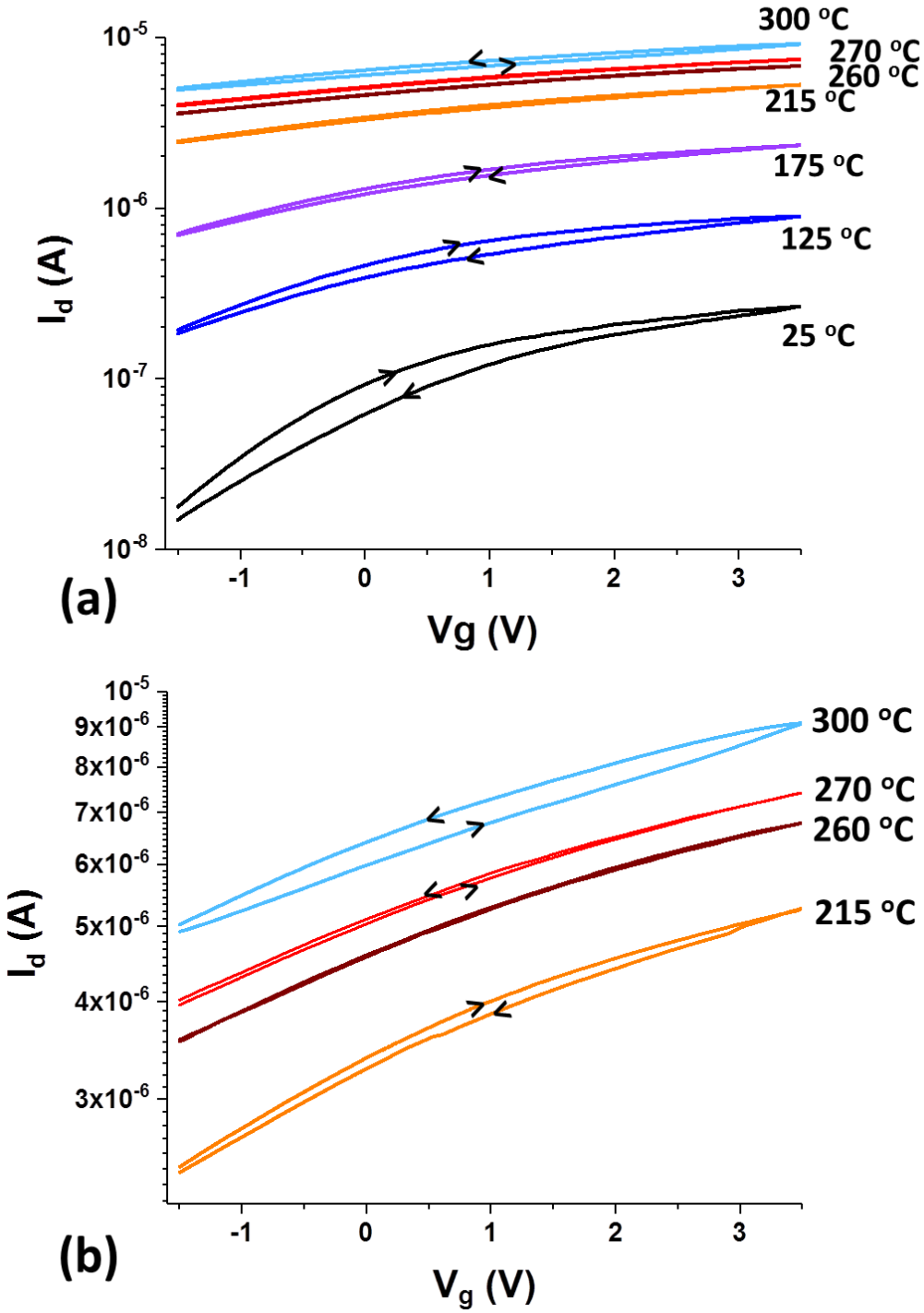

Figure 8.5: (a) I_d - V_g characteristics during the first heating cycle, (b) close-up of the high temperature range.

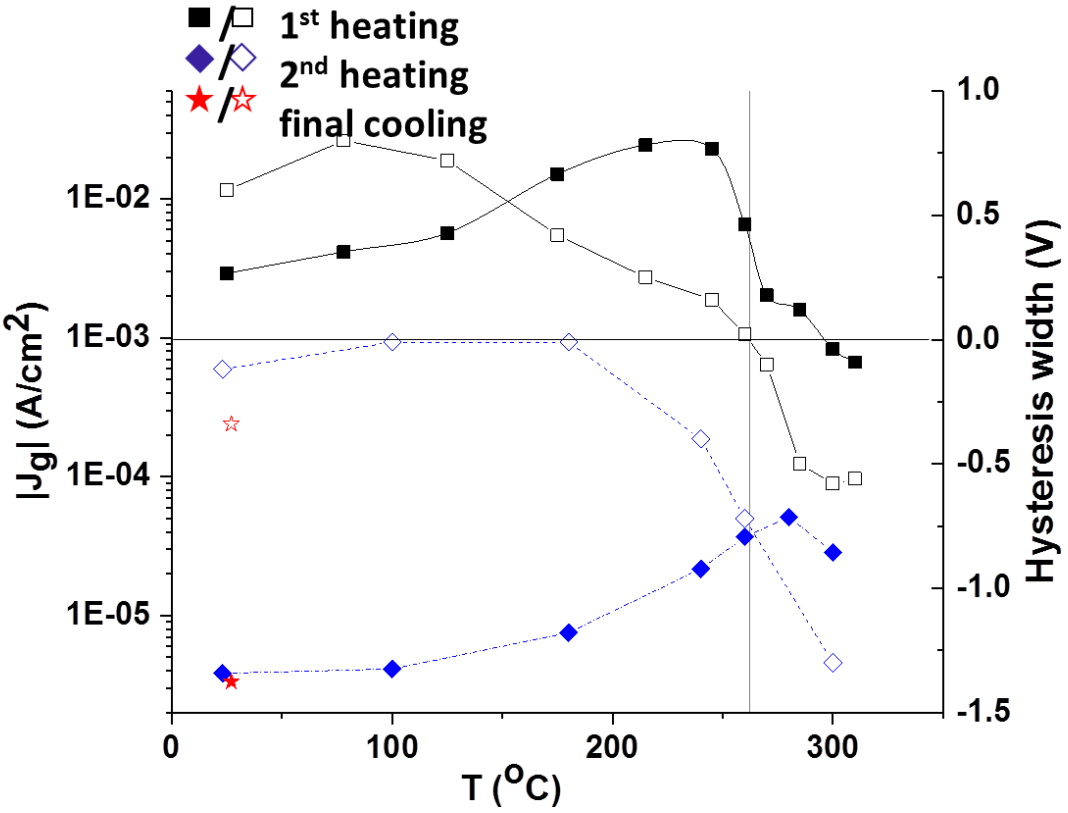

Figure 8.6: leakage current density (filled symbols - absolute value of current density at V_g = -1.2 V for each temperature) and hysteresis width (open symbols – largest hysteresis width of I_d - V_g loop) evolution with temperature. Clockwise hysteresis loops are represented with positive values, while counter-clockwise loops are represented with negative values, the vertical line indicates the temperature at which the hysteresis loop changes direction during the first heating cycle.

Gate leakage current is an indication of charge-trapping which is proportional to defect density. It is well-known that polymer conduction increases exponentially with temperature. This behavior is reflected in the gate leakage curve in Figure 8.6 which indeed increases with temperature over the lower temperature ranges. However, this trend diverges at ≈150 ^{o}C and actually trends downward rapidly at T_g. This behavior indicates

that defect annealing is decreasing the gate leakage current faster than temperature-induced increases. The hysteresis data is also consistent with this defect annealing interpretation as there is a transition from clockwise to counter-clockwise at T_g. This is an indication that the combined effect of mobile ions and dipole rotation is stronger than charge-trapping at this high temperature. This interpretation is reinforced in the examination of the second heating cycle. The leakage current at the beginning of the second heating cycle is several orders of magnitude less than that measured at the beginning of the first heating cycle. Furthermore, the leakage increase with temperature during the second cycle does not turn around until temperatures exceeding T_g. Clearly, the defect density is much lower. The hysteresis loop is also protracted but still counter-clockwise. This hysteresis persists until the temperature reaches 200 ^{o}C. At higher temperatures, the hysteresis increases with temperature but remains counter-clockwise. Upon completion of the second heating cycle, the sample is cooled to room temperature. At room temperature, the leakage current is found to be slightly lower than at the beginning of the second heating cycle, indicating minimal further defect annealing during the second heating cycle. The room temperature hysteresis increases somewhat and remains counter-clockwise. This is likely a contribution from mobile ions because charge-trapping is negligible and dipole rotation is largely forbidden. Since mobile ions are already mobile at room temperature, the hysteresis observed during the second heating cycle is due to dipole rotation, plus a small contribution due to the further reduction of charge-trapping.

The device used to generate Figure 8.4 has negligible hysteresis at room temperature and very low leakage current. Based on the above discussion, we can conclude that the dominating factor that produced the flat-band shift is dipole rotation under the applied field at high temperature (programming). The magnitude of V_{FB} shift and the device capacitance (~1.3 $\mu F/cm^2$) indicates that the dipole density is at least $10^{12}/cm^2$. Note that not all dipoles are aligned to the applied field since the net dipole moment must satisfy the applied field.

8.3 Multi-state Programming

As mentioned above, when programming a device, not all dipoles in the polymeric film are aligned to the applied field, but only the appropriate number of dipoles that are needed to satisfy the externally applied field. It is this property that also facilitates temperature-assisted multi-state programming by simply tuning the applied programming voltage at higher temperatures. At these higher temperatures, the dipoles are almost freely rotating. In this situation, arbitrarily low program voltages can be used (limited only by thermal noise). Figure 8.7 demonstrates this multi-state programming capability.

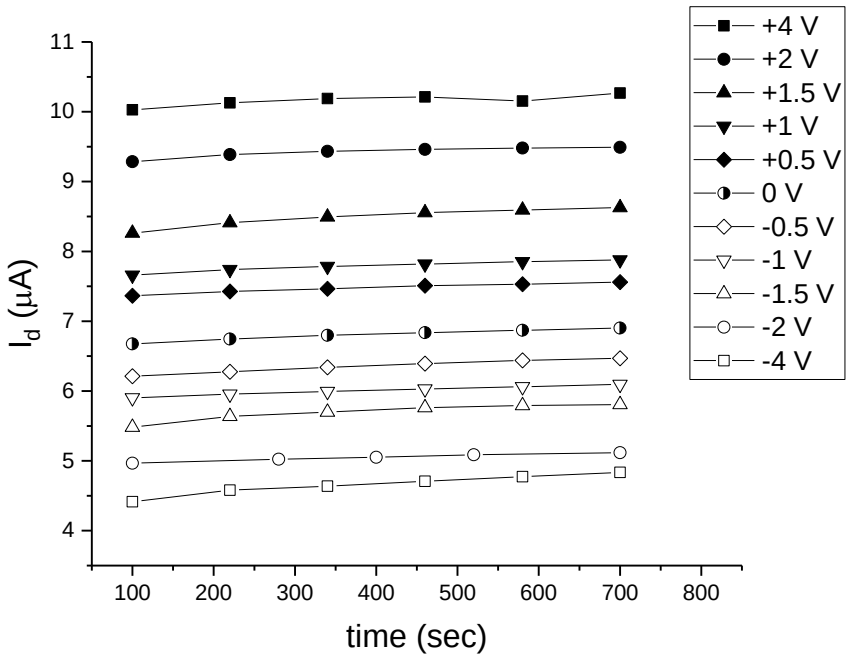

Figure 8.7: Multi-state memory effect for a device with channel L = 2 μm, and W = 6.5 μm.

The data shown in Figure 8.7 were sequentially collected by programming and returning the device to an initial state by heating up the polymer without bias between programming states. With sufficient time, thermal agitation will randomize dipole orientations, equalize the mobile ion distribution, and minimize the trapped charge through thermally stimulated emission. The unequal spacing of the initial program-state shown in Figure 8.7 reflects the somewhat incomplete initialization between each measurement and should not be interpreted as a lower threshold for state granularity. As mentioned above, at 275 ^{o}C the dipoles freely rotate up to 300 kHz. Thus, the incomplete initialization cannot be attributed to incomplete dipole randomization. Incomplete initialization reflects that we have the usual charge injection and mobile ion problems which are typically associated with research grade devices.

Multi-state programming has been demonstrated in earlier reports[59],[60] with low T_g films. Without the benefit of the thermally-assisted method, multi-state programming relies on the delicate balance between applied field and programming time. This approach presents a fundamental conflict between fast programming and detailed state control. In actual applications, device-to-device variation will render this an impractical method to achieve reliable multi-state programming. In addition, read/program disturb immunity of this approach is expected to be extremely poor. On the contrary, the new organic FeRAM proposed here does not rely on the delicate balance to achieve multi-state programming. The memory state is entirely determined by the program voltage, which can be any value below saturation. Once programmed, the states are completely immune to disturb (see Figure 8.3).

8.4 Memory Retention

Figure 8.8 presents the retention time study of a typical device. The device was consecutively programmed at +4 V, 0 V and -4 V. A clear initial decay is observed for the +4V program state for this device. The only explanation that is consistent with the observed significant positive program state change and muted negative program state change is the presence of positively charged mobile ions. During positive programming, positive mobile ions accumulate at the polymer/semiconductor interface where they have the biggest effect on V_{FB}. During the retention study, these ions driven by the depolarization field diffuse away from that interface leading to a positive flat band shift and a decrease in drain current. During negative programming, positive ions are attracted

to the polymer/gate interface where the effect on flat band voltage is minimal. Throughout the subsequent negative state retention study, mobile ions slowly diffuse away from the gate and slowly decrease the drain current.

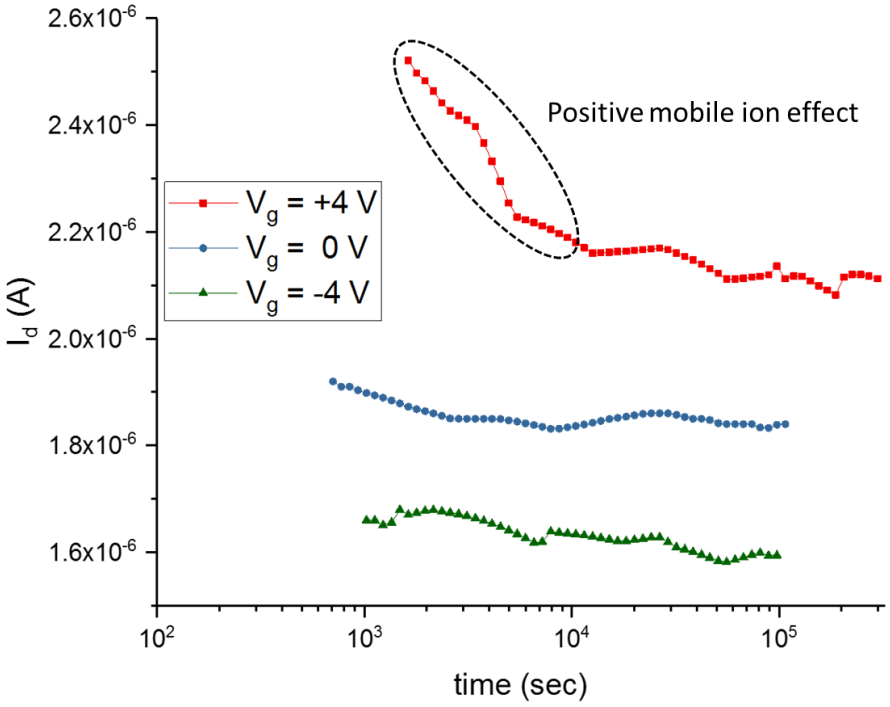

Figure 8.8: Memory retention measurements versus time.

If charge injection dominated, positive programming means electrons are injected from the semiconductor. The emission of these trapped electrons would increase the drain current, which is inconsistent with the data. Depolarization can also be discounted because positive gate voltage accumulates the semiconductor and negative gate voltage depletes the semiconductor. Band-bending, and therefore the depolarization field, is

stronger in depletion than in accumulation which again counters the observations in Figure 8.8.

The above discussion allows one to conclude that Figure 8.8 shows no sign of retention loss due to depolarization after 10^5 seconds. While this does not outperform recent literature reports,[15][21][23] it clearly demonstrate the short programming time at high temperature and long retention time at room temperature. From Figure 8.2 one expects the retention may not be 10 years. However, it should be better than PVDF by ≈7 orders of magnitude.

8.5 Projection of Programming Time and Endurance

It is reasonable to question the practicality of the thermal-assisted programming concept. However, integrating micro heater integration is becoming commonplace.[66] Micro-heater integration does make device fabrication somewhat more complex however this approach has been enabled by the mass-production of phase-change memories.[67],[68] For future technology nodes the sense transistor itself can self-heat[69] the polymer to the needed temperature during programming. While self-heating effect (SHE) is a growing problem for nanometer-scale CMOS and beyond and much research is on-going to mitigate it, this proposed new memory concept takes advantage of it instead – turning a problem into a solution. Figure 8.9 shows the simulated temperature rise if the transistor is running at 1 mA/μm, which is very conservative for such highly scaled device. It is clear that the needed thermal assist can be achieved in as little as 100

ps. Whether using transistor self-heating or an integrated local micro heater, the thermal-assisted programming concept is practical.

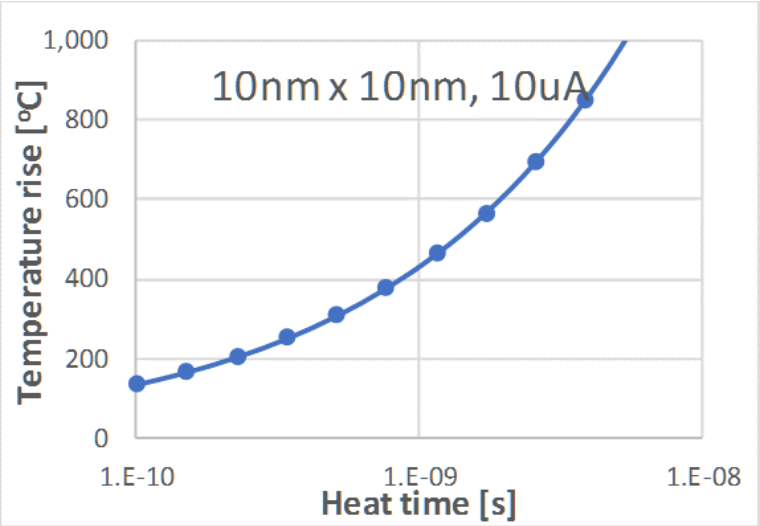

Figure 8.9: Simulated temperature rise of a 10 nm x 10nm transistor channel when 10 μA current flows through.

Apart from fast programming, a promising memory technology requires the prospective of high endurance. For the proposed technology, if we assume that at each programming operation, the polymer is heated up to near melting temperature (well above T_g) to achieve high program speed, it is practical to question how many times the cell can be programmed. Naturally, it depends on the specific polymer. Many polymers remain stable in molten state for days or even much longer in the absence of oxygen (or another oxidizing agent). However, it is expected that the proposed GeRAM cell should be fully encapsulated and therefore no oxidizing agent will be present. For 100 ps programming, one day will be the equivalent of ≈1015 cycles.

Moreover, by nearly melting the polymer film in each programming cycle, the polymer chain gets fully relaxed every single time, returning to an initial state. Thus, GeRAM should not suffer from the problem of imprint (preferential polarization state from previous writes to present state) that plagues current FeRAM technology.[70]

8.6 Conclusion

The literature reports on ferroelectric memory focus on prolonging the retention time and multi-state programing of a single device. However, the reported retentions are far from adequate for most intended applications. Moreover, multi-state programming reports generally rely on a very delicate (impractical) balance between applied electric field and the programming time. Most importantly, in the actual applications, memory cells are always used in 2-dimensional array and therefore subject to program and read disturbs. All the reported retention or multi-states performances are meaningless in the presence of these disturbs. In this chapter we demonstrate a method of manipulating the polymer properties while using thermally-assisted programming to achieve long retention time, multi-states capability and, most importantly, immunity to disturbs.

CHAPTER NINE CONCLUSIONS AND FUTURE WORK

9.1 Concluding Remarks for the Dissertation

This dissertation is focused on a novel class of non-volatile ferroelectric memory based on high T_g polar polymers. First, the characteristics as well as the advantages and the drawbacks of the state of the art Ferroelectric memory technology are discussed. Then, the concept of the proposed memory technology is introduced, and ferroelectric FETs are fabricated and characterized. Moreover, the effect of a short and mild annealing process on the fabricated FeFETs is presented. At last, the ferroelectric effect of the devices is demonstrated and it is shown how the concept of thermally assisted programming of an organic memory device incorporating high-T_g polar polymers can overcome many of the problems associated with FeRAM, leading to the realization of arbitrary programming states and long retention times.

The major findings of this dissertation are summarized in the following:

1. The proof of the ferroelectric effect in FeFETs is controversial due to the similar effects of parasitic mechanisms such as charge injection and trapping in the polymeric dielectric and the presence of mobile ions. However, we have shown that the observed shape, position and direction of the hysteresis loop contain very specific information to remove various potential factors that cofound the confirmation of ferroelectric switching.

2. Defects in the polar polymer of the fabricated FeFET that were created by small atomic displacement, such as elastic stress arising from metal contact deposition can be annealed at temperature well below T_m. We observed surprisingly efficient annealing of polymer defects at and below the glass transition temperature. A drastic reduction of leakage current density in such short "low" temperature anneals is shown. The reduction of defect density was confirmed by the joint behavior of leakage current density and $I_d - V_g$ hysteresis.
3. Ferroelectric effect in fabricated FeFETs incorporating a high-T_g polar polymer in the gate dielectric stack is confirmed. It is shown that thermal-assisted programming leads to long retention times, while the device is immune to depolarization fields (intrinsic and externally applied) at operation temperatures.
4. The thermally-assisted programming allows multi-states programming by arbitrarily low program voltages (limited only by thermal noise), while the states are independent of the programming times.
5. It is shown through simulations that the temperature required for thermally-assisted programming can be achieved for nano-size devices in as little as 100 ps, allowing fast programming.

9.2 Prospects for Future Work

There are a number of improvements and further investigations in this work that can be performed. First, other polar polymers with high T_g, such as LaRC-CP2, that have a steeper characteristic frequency versus temperature response should be used as the gate dielectric. The steeper this slope is, the smaller temperature change is required to program the memory cell, and consequently less power is consumed. Second, the interface between the polar polymer and the semiconductor channel has to be investigated and optimized in order to minimize charge trapping and maximize drain current modulation. Using another polymer, replacing the poly-Si with single-crystal Si substrate, or introducing a thin grown good quality silicon dioxide might result in a better interface. Finally, smaller device size should be fabricated in order to show a faster programming process, at least at the order of μs.

REFERENCES

[1] G. E. Moore, “Progress in Dıgital Integrated,” *Electron Devices Meet. 1975 Int.*, vol. 21, pp. 11–13, 1975.

[2] S. I. Assoc., “International Technology Roadmap for Semiconductors 2.0,” 2015.

[3] R. H. Dennard, “FIELD-EFFECT TRANSISTOR MEMORY,” 1968.

[4] K. Kim, “From the future si technology perspective,” in *Electron Devices Meeting (IEDM)*, 2010.

[5] A. . Alvandpour and S. Natarajan, “Emerging memory technologies,” in *IEEE VLSI-TSA International Symposium*, 2005.

[6] G. W. Burr, B. N. Kurdi, J. C. Scott, C. H. Lam, K. Gopalakrishnan, and R. S. Shenoy, “Overview of candidate device technologies for storage,” *IBM J. Res. Dev.*, vol. 52, no. 4.5, pp. 449–464, 2008.

[7] K. Galatsis *et al.*, “Emerging memory devices,” *IEEE Circuits and Devices Magazine*, pp. 12–21, 2006.

[8] S. Yu, “Overview of resistive switching memory (RRAM) switching mechanism and device modeling,” in *Proceedings - IEEE International Symposium on Circuits and Systems*, 2014, pp. 2017–2020.

[9] M. Hosomi *et al.*, “A novel nonvolatile memory with spin torque transfer magnetization switching: spin-ram,” *IEEE Int. Devices Meet. 2005. IEDM Tech. Dig.*, vol. 0, no. c, pp. 459–462, 2005.

[10] S. Raoux *et al.*, “Phase-change random access memory: A scalable technology,” *IBM J. Res. Dev.*, vol. 52, no. 4.5, pp. 465–479, 2008.

[11] G. R. Fox, R. Bailey, W. B. Kraus, F. Chu, S. Sun, and T. Davenport, “The Current Status of FeRAM,” in *Ferroelectric Random Access Memories*, Springer, Berlin, Heidelberg, 2004, pp. 139–148.

[12] D. A. Buck, “Ferroelectrics for Digital Information Storage and Switching.”

[13] J. R. Macdonald, “Impedance Measurement Techniques,” in *Impedance Spectroscopy Emphasizing Solid Materials and Systems*, 1987, pp. 134–159.

[14] T. P. Ma and J. P. Han, “Why is nonvolatile ferroelectric memory field-effect transistor still elusive?,” *IEEE Electron Device Lett.*, vol. 23, no. 7, pp. 386–388, 2002.

[15] R. C. G. Naber *et al.*, “High-performance solution-processed polymer ferroelectric field-effect transistors,” *Nat. Mater.*, vol. 4, no. 3, pp. 243–248, 2005.

[16] K. Asadi, D. M. de Leeuw, B. de Boer, and P. W. M. Blom, “Organic non-volatile memories from ferroelectric phase-separated blends.,” *Nat. Mater.*, vol. 7, no. 7, pp. 547–550, 2008.

[17] S. Fujisaki, H. Ishiwara, and Y. Fujisaki, “Organic ferroelectric diodes with long

retention characteristics suitable for non-volatile memory applications," *Appl. Phys. Express*, vol. 1, no. 8, pp. 0818011–0818013, 2008.
[18] S.-W. Jung *et al.*, "Non-volatile organic ferroelectric memory transistors fabricated using rigid polyimide islands on an elastomer substrate," *J. Mater. Chem. C*, vol. 4, no. 20, pp. 4485–4490, 2016.
[19] R. Sugano *et al.*, "Ultrathin flexible memory devices based on organic ferroelectric transistors," *Jpn. J. Appl. Phys.*, vol. 55, no. 10, 2016.
[20] V. Khikhlovskyi, A. J. J. M. Van Breemen, R. A. J. Janssen, G. H. Gelinck, and M. Kemerink, "Data retention in organic ferroelectric resistive switches," *Org. Electron. physics, Mater. Appl.*, vol. 31, pp. 56–62, 2016.
[21] S. Das and J. Appenzeller, "FETRAM. An organic ferroelectric material based novel random access memory cell," *Nano Lett.*, vol. 11, no. 9, pp. 4003–4007, 2011.
[22] R. Schroeder, L. A. Majewski, and M. Grell, "All-Organic Permanent Memory Transistor Using an Amorphous, Spin-Cast Ferroelectric-like Gate Insulator," *Adv. Mater.*, vol. 16, no. 7, pp. 633–636, 2004.
[23] M. A. Khan, U. S. Bhansali, and H. N. Alshareef, "High-performance non-volatile organic ferroelectric memory on banknotes," *Adv. Mater.*, vol. 24, no. 16, pp. 2165–2170, 2012.
[24] C. Park, Z. Ounaies, J. Su, and J. Harrison, "Polarization stability of amorphous piezoelectric polyimides," no. February 2000, pp. 1–7, 1999.
[25] G. A. Miner *et al.*, "The Wettability of LaRC Colorless Polyimide Resins on Casting Surfaces," in *1997 American Chemical Society National Meeting*, 1997.
[26] D. S. Fryer *et al.*, "Dependence of the glass transition temperature of polymer films on interfacial energy and thickness," *Macromolecules*, vol. 34, no. 16, pp. 5627–5634, 2001.
[27] J. H. Kim, J. Jang, and W.-C. Zin, "Thickness Dependence of the Glass Transition Temperature in Thin Polymer Films," *Langmuir*, vol. 17, no. 9, pp. 2703–2710, 2001.
[28] J. D. Musgraves, S. Danto, and K. Richardson, "4 - Thermal properties of chalcogenide glasses BT - Chalcogenide Glasses," in *Chalcogenide Glasses: Preparation, Properties and Application*, J.-L. A. X. Zhang, Ed. Woodhead Publishing, 2014, pp. 82–112.
[29] W. C. Stewart, "Infrared and X-Ray Photoelectron Spectroscopy Sudies of the Polyimide/Metal Interface," University of Minnesota, 1989.
[30] R. J. Jensen, J. P. Cummings, and H. Vora, "Copper/Polyimide Materials System for High Performance Packaging," *IEEE Trans. Components, Hybrids, Manuf. Technol.*, vol. 7, no. 4, pp. 384–393, 1984.
[31] K. Kelley, Y. Ishino, and H. Ishida, "Fourier Transform IR Reflection Techniques for Characterization of Polyimide Films on Copper Substrates," *Thin Solid Films*, vol. 154, pp. 271–279, 1987.
[32] K. Müller, K. Henkel, I. Paloumpa, and D. Schmeißer, "Organic field effect transistors with ferroelectric hysteresis," *Thin Solid Films*, vol. 515, no. 19 SPEC. ISS., pp. 7683–7687, 2007.

[33] T. J. Lewis, “Charge transport, charge injection and breakdown in polymeric insulators,” *J. Phys. D. Appl. Phys.*, vol. 23, no. 12, pp. 1469–1478, 2000.
[34] A. A. Aly, “Heat Treatment of Polymers: A Review,” *Int. J. Mater. Chem. Phys.*, vol. 1, no. 2, pp. 132–140, 2015.
[35] L. I. Samoilova, P. Y. Apel, and I. E. Larionova, “TEMPERATURE EFFECTS IN POLYIMIDES IRRADIATED BY HEAVY IONS,” in *Proc. Third Int. Conf. Particle Track membranes ans their Applications*, 1993, pp. 85–88.
[36] J. H. Park, N. Kurra, M. N. AlMadhoun, I. N. Odeh, and H. N. Alshareef, “A two-step annealing process for enhancing the ferroelectric properties of poly(vinylidene fluoride) (PVDF) devices,” *J. Mater. Chem. C*, vol. 3, no. 10, pp. 2366–2370, 2015.
[37] V. Georgiou, D. Veksler, D. E. Ioannou, and K. P. Cheung, “A simple method to prove ferroelectric switching for polymer ferroelectric memory,” in *International Semiconductor Device Research Symposium*, 2016.
[38] M. Egginger, S. Bauer, R. Schwödiauer, H. Neugebauer, and N. S. Sariciftci, “Current versus gate voltage hysteresis in organic field effect transistors,” *Monatshefte fur Chemie*, vol. 140, no. 7, pp. 735–750, 2009.
[39] S. A. Kaffafi, “THE IONIZATION POTENTIAL, ELECTRON AFFINITY AND ENERGY GAP OF POLYIMIDE,” *Chem. Phys. Lett.*, vol. 169, no. 6, pp. 561–563, 1990.
[40] M. Y. Ruan, H. Moaddel, a. M. Jamieson, R. Simha, and J. D. McGervey, “Positron annihilation lifetime studies of free volume changes in polycarbonate under static tensile deformation,” *Macromolecules*, vol. 25, no. 9, pp. 2407–2411, 1992.
[41] C. L. Wang, B. Wang, S. Q. Li, and S. J. Wang, “Effects of deformation on the microstructure of PTFE polymer studied by positron annihilation,” *J. Phys. Condens. Matter*, vol. 5, pp. 7515–7520, 1993.
[42] T. C. Sandreczki, X. Hong, and Y. C. Jean, “Sub-Glass-Transition-Temperature Annealing of Polycarbonate Studied by Positron Annihilation Spectroscopy,” *Macromolecules*, vol. 29, no. 11, pp. 4015–4018, 1996.
[43] B. Stadlober, M. Zirkl, M. Beutl, G. Leising, S. Bauer-Gogonea, and S. Bauer, “High-mobility pentacene organic field-effect transistors with a high-dielectric-constant fluorinated polymer film gate dielectric,” *Appl. Phys. Lett.*, vol. 86, no. 24, pp. 1–3, 2005.
[44] C. A. Lee, D. W. Park, S. H. Jin, H. Park, J. D. Lee, and B. G. Park, “Hysteresis mechanism and reduction method in the bottom-contact pentacene thin-film transistors with cross-linked poly(vinyl alcohol) gate insulator 252102,” *Appl. Phys. Lett.*, vol. 88, no. 25, 2006.
[45] M. Egginger *et al.*, “Mobile ionic impurities in poly (vinyl alcohol) gate dielectric: Possible source of the hysteresis in organic field-effect transistors,” *Adv. Mater.*, vol. 20, no. 5, pp. 1018–1022, 2008.
[46] T. Da Tsai, J. W. Chang, T. C. Wen, and T. F. Guo, “Manipulating the hysteresis in poly(vinyl alcohol)-dielectric organic field-effect transistors toward memory elements,” *Adv. Funct. Mater.*, vol. 23, no. 34, pp. 4206–4214, 2013.

[47] J. H. Kim, J. Jang, and W. C. Zin, “Thickness dependence of the glass transition temperature in thin polymer films,” *Langmuir*, vol. 17, no. 17, pp. 2703–2710, 2001.
[48] D. Mandal, K. Henkel, K. Muller, and D. Schmeiber, “Bandgap determination of P(VDF-TrFE) copolymer film by electron energy loss spectroscopy,” *Bull. Mater. Sci.*, vol. 33, no. 4, pp. 457–461, 2010.
[49] C. Duan, W. N. Mei, J. R. Hardy, S. Ducharme, J. Choi, and P. A. Dowben, “Comparison of the theoretical and experimental band structure of poly (vinylidene fluoride) crystal,” *Europhys. Lett.*, vol. 61, no. 1, pp. 81–87, 2003.
[50] D. R. Wolters and J. J. Van Der Schoot, “Kinetics of charge trapping in dielectrics,” *J. Appl. Phys.*, vol. 58, no. 2, pp. 831–837, 1985.
[51] Y. Taur and T. H. Ning, “MOS Capacitors,” in *Fundamentals of Modern VLSI Devices*, 2009, pp. 73–107.
[52] F. P. Heiman and G. Warfield, “The effects of oxide traps on the MOS capacitance,” *IEEE Trans. Electron Devices*, vol. 12, no. 4, pp. 167–178, 1965.
[53] Y. Wang, V. Lee, and K. P. Cheung, “Frequency dependent charge-pumping, how deep does it probe?,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 6–9, 2006.
[54] A. Hadjadj, O. Simonetti, T. Maurel, G. Salace, and C. Petit, “Si-SiO2 barrier height and its temperature dependence in metal-oxide-semiconductor structures with ultrathin gate oxide,” *Appl. Phys. Lett.*, vol. 80, no. 18, pp. 3334–3336, 2002.
[55] W. J. Zhu, T. P. Ma, T. Tamagawa, J. Kim, and Y. Di, “Current transport in metal/hafnium oxide/silicon structure,” *IEEE Electron Device Lett.*, vol. 23, no. 2, pp. 97–99, 2002.
[56] a. Mallikarjunan, S. P. Murarka, and T.-M. Lu, “Mobile Ion Detection in Organosiloxane Polymer Using Triangular Voltage Sweep,” *J. Electrochem. Soc.*, vol. 149, p. F155, 2002.
[57] J. Beilsten-Edmands, G. E. Eperon, R. D. Johnson, H. J. Snaith, and P. G. Radaelli, “Non-ferroelectric nature of the conductance hysteresis in CH<inf>3</inf>NH<inf>3</inf>PbI<inf>3</inf> perovskite-based photovoltaic devices,” *Appl. Phys. Lett.*, vol. 106, no. 17, pp. 2–7, 2015.
[58] T. Furukawa, H. Matsuzaki, M. Shina, and Y. Tajitsu, “Nanosecond Switching in Thin Fims of Vinylidene Fluoride_Trilluoroethylene Copolymers,” *Jpn. J. Appl. Phys.*, vol. 24, pp. L661–L662, 1985.
[59] S. K. Hwang, I. Bae, S. M. Cho, R. H. Kim, H. J. Jung, and C. Park, “High performance multi-level non-volatile polymer memory with solution-blended ferroelectric polymer/high-k insulators for low voltage operation,” *Adv. Funct. Mater.*, vol. 23, no. 44, pp. 5484–5493, 2013.
[60] D. Zhao, I. Katsouras, K. Asadi, W. A. Groen, P. W. M. Blom, and D. M. De Leeuw, “Retention of intermediate polarization states in ferroelectric materials enabling memories for multi-bit data storage,” *Appl. Phys. Lett.*, vol. 108, no. 23, 2016.
[61] Y.-H. Chou, H.-J. Yen, C.-L. Tsai, W.-Y. Lee, G.-S. Liou, and W.-C. Chen, “Nonvolatile transistor memory devices using high dielectric constant polyimide

electrets," *J. Mater. Chem. C*, vol. 1, no. 19, p. 3235, 2013.
[62] S. Park, K. Kim, D. M. Kim, W. Kwon, J. Choi, and M. Ree, "High temperature polyimide containing anthracene moiety and its structure, interface, and nonvolatile memory behavior," *ACS Appl. Mater. Interfaces*, vol. 3, no. 3, pp. 765–773, 2011.
[63] V. Bharti and Q. Zhang, "Dielectric study of the relaxor ferroelectric poly(vinylidene fluoride-trifluoroethylene) copolymer system," *Phys. Rev. B*, vol. 63, no. 18, pp. 1–6, 2001.
[64] K. L. Ngai, "Mobility in thin polymer films ranging from local segmental motion, Rouse modes to whole chain motion: A coupling model consideration," *Eur. Phys. J. E*, pp. 225–235, 2002.
[65] J. D. Jacobs *et al.*, "Dielectric characteristics of polyimide CP2," *Polymer (Guildf).*, vol. 51, no. 14, pp. 3139–3146, 2010.
[66] Z. Jiang *et al.*, "Microsecond Transient Thermal Behavior of HfOx-based Resistive Random Access Memory Using a Micro Thermal Stage (MTS)," in *Int. Electron dev. Meeting (IEDM)*, 2016, pp. 560–563.
[67] H.-S. P. Wong *et al.*, "Phase Change Memory," *Proc. IEEE*, vol. 98, no. 12, pp. 2201–2227, 2010.
[68] J. H. Park *et al.*, "Improvement of reliability and speed of phase change memory devices with Improvement of reliability and speed of phase change," vol. 9, no. 2015, pp. 0–12, 2015.
[69] O. Semenov, A. Vassighi, and M. Sachdev, "Impact of self-heating effect on long-term reliability and performance degradation in CMOS circuits," *IEEE Trans. Device Mater. Reliab.*, vol. 6, no. 1, pp. 17–27, 2006.
[70] N. Inoue and Y. Hayashi, "Effect of imprint on operation and reliability of ferroelectric random access memory (FeRAM)," *IEEE Trans. Electron Devices*, vol. 48, no. 10, pp. 2266–2272, 2001.

BIOGRAPHY

Vasileia Georgiou received her Diploma on Electrical and Computer Engineering from National Technical University of Athens in 2009. She received her Master of Science in Electrical and Computer Engineering from George Mason University in 2012. She has been a Guest Researcher in the Semiconductor and Dimensional Metrology Division at the National Institute of Standards and Technology (NIST), Gaithersburg, MD, since 2011. Ms Vasileia Georgiou has recently joined Roche Molecular Sequencing as a Process Engineer. Her research interests include organic ferroelectric materials, organic memories, solid state nanofabrication, and solid state devices for DNA sequencing.

PUBLICATIONS RELATED TO THIS WORK

Reviewed Journal Articles:

- **V. Georgiou**, D. Veksler, J.T. Ryan, J.P. Campbell, P.R. Shrestha, D.E. Ioannou, and K.P. Cheung, "Highly Efficient Rapid Annealing of Thin Polar Polymer Film Ferroelectric Devices at Sub-Glass Transition Temperature", Advanced Functional Materials (accepted for publication, DOI 10.1002/adfm.201704165).
- **V. Georgiou**, D. Veksler, J.P. Campbell, J.T. Ryan, P.R. Shrestha, D.E. Ioannou, and K.P. Cheung, "Ferroelectricity in Polar Polymer-based FETs: A Hysteresis Analysis", Advanced Functional Materials (under review / revision submitted).
- **V. Georgiou**, D. Veksler, J.P. Campbell, J.T. Ryan, P.R. Shrestha, D.E. Ioannou, and K.P. Cheung, "Depolarization-Free Polymer-Based Ferroelectric Memory with Arbitrary Polarization States" (under review).

International Conferences:

- **V. Georgiou**, Jason P. Campbell, Pragya R. Shrestha, Dimitris E. Ioannou, and Kin P. Cheung, “Glassy-Electret Random Access Memory – A naturally Nanoscale Memory Concept”, International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), Hsinchu, Taiwan, April 2018 (submitted).

- **V. Georgiou**, D. Veksler, J.P. Campbell, P.R. Shrestha, J.T. Ryan, D.E. Ioannou, and K.P. Cheung, "Novel Approach to Mitigate the Trade-Offs Between Fast Programming and Long Retention Times in Polymer Ferroelectric Memory", International Meeting on Ferroelectricity (IMF), San Antonio, TX, September 2017.
- **V. Georgiou**, D. Veksler, J.P. Campbell, P.R. Shrestha, J.T. Ryan, D.E. Ioannou, and K.P. Cheung, "Anomalous behaviors of FeFETs based on polar polymers with high glass temperature", SPIE Organic Photonics + Electronics, San Diego, CA, August 2017.
- **V. Georgiou**, D. Veksler, D.E. Ioannou, and K.P. Cheung, "Retention Study of Novel Class of Organic Ferroelectric Memories", 14th International Conference on Nanosciences and Nanotechnologies (NN17), Thessaloniki, Greece, July 2017 (invited).
- **V. Georgiou**, D. Veksler, J.P. Campbell, J.T. Ryan, D.E. Ioannou, and K.P. Cheung, "Engineering Ferroelectric Polymer Memories: Confounding Factors Which Obscure Polarization", International Conference on Frontiers of Characterization and Metrology for Nanoelectronics (FCMN), Monterey, CA, March 2017.
- **V. Georgiou**, D. Veksler, D.E. Ioannou, and K.P. Cheung, "A simple method to prove ferroelectric switching for polymer ferroelectric memory", International Semiconductor Device Research Symposium (ISDRS), Bethesda, MD, December 2016.