SPATIAL AND TEMPORAL SCHEDULING OF CLOCK ARRIVAL TIMES FOR IR HOT-SPOT MITIGATION, REFORMULATION OF PEAK CURRENT REDUCTION & PHYSICAL DESIGN AUTOMATION TOOL

by

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by

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DEDICATION

I dedicate this thesis to my parents Sulochana and GSN Reddy, my wife Lavanya and my son Karthik.

ACKNOWLEDGEMENTS

I would like to express my heartfelt gratitude to my advisor Dr. Avesta Sasan for introducing me to several aspects of ASIC physical Design, and for continuously motivating and guiding me throughout the research. This thesis would not have been possible if not for him. I would also like to take this opportunity to thank Lakshmi B for her support in getting the work done.

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LIST OF ABBREVIATIONS AND SYMBOLS

Voltage Drop ..... IR Drop
Power Delivery Network ..... PDN
Clock Tree Synthesis ..... CTS
Clock Arrival Time ..... CAT
Nominal Threshold Voltage ..... NTV
Super Threshold Voltage ..... STV
Threshold Voltage ..... VT
Toggle Rate ..... TR
Metal 1- Metal 7 ..... M1-7
Effective Series Resistance ..... ESR
Decoupling Capacitors ..... DECAPS
Circuit Under Design ..... CUD
Re-distribution Layer ..... RDL
Minimum Resistance Path ..... MRP
Supply Voltage ..... VDD
Ground Voltage ..... VSS
Micro meter squared ..... μm^2

ABSTRACT

SPATIAL AND TEMPORAL SCHEDULING OF CLOCK ARRIVAL TIMES FOR IR HOT-SPOT MITIGATION, REFORMULATION OF PEAK CURRENT REDUCTION & PHYSICAL DESIGN AUTOMATION TOOL

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George Mason University, 2017

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One of the major reason for chip failures is on chip variability. In order to prevent failures due to on chip variability, the variability need to be margined in physical design by providing voltage guard band. One of the major reasons of variability is dynamic IR drop. To prevent the timing failures due to large IR drop, big margin is provided as voltage gaur band. So by reducing IR drop the timing failures can be avoided and this gives option for reducing the voltage gaur band margin. In this thesis we propose a technique to reduce the IR drop by temporal scheduling of clock arrival times for IR Hot-Spot mitigation. In this technique we utilize the available slack and scheduling useful skew we distribute the switching of cells within the timing window. Previous work done for reducing the IR-drop was focused on reducing the overall peak current but we breakdown the problem into many smaller problems of local IR-hotspots. And based on location of the cells we group them based on minimum resistive region and change the

clock arrival time of the flip flops for reducing the intensity of individual hot spots. Application of the proposed solution to a selected number of IWLS benchmarks reduces the peak IR-drop by ~35%, and peak current by ~37%. We have published papers on this work in conference ISLPED [1]and ISVLSI [2].

Complete Physical design process involves various tools like Design compiler, Primetime, ICC and needs many scripts to be implemented and executed. And complete Physical design process is time consuming and based on the size of the design. To automate the physical design process across all tools used a tool was implemented based using GNU make. Using this Physical design automation tool all the physical design steps like Synthesis, Floor-planning, Placement, Clock Tree Synthesis, Routing and STA analysis was automated.

1 INTRODUCTION

In a synchronous design, at each clock cycle, the triggering edge of input clock enables the registers to launch their state value into the next pipeline stage, causing a surge of switching activity. The switching activity quickly reduces as signals propagate down the combinatorial logic [1]. Hence, the peak current demand lines up with the triggering edge of the clock. Therefore, during the Clock Tree Synthesis (CTS), optimization for zero clock skew significantly increases the intensity of peak current demand [2]. Demanded current, in the result of this clock orchestrated simultaneous switching, depletes the nearby decoupling capacitances and results in large demanded battery current in a short interval. Hence, the resistive PDN experience resistive voltage drop, and the inductive package respond to this current spike by inductive voltage drop and RLC oscillation afterward, a scenario that is repeated at every clock cycle.

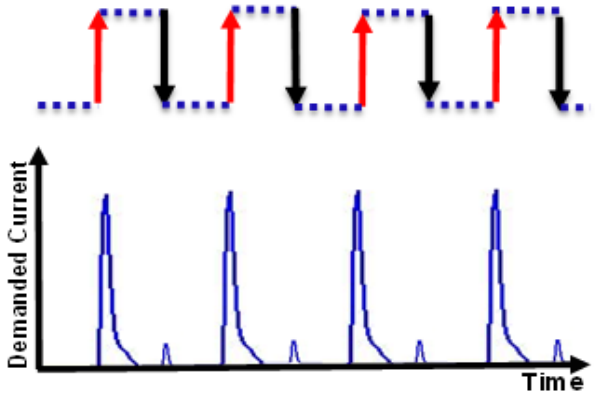

Figure 1. Peak current demand

Total IR drop is addition of resistive IR drop and an inductive IR drop. The resistive IR drop is IR and this could be reduced by decreasing the resistance of Power Delivery Network (PDN) or reducing the peak current passing through the elements of PDN. The inductive IR drop *Ldi/dt* could be reduced by reducing the inductance (L) of board and package, or by reducing the rate of change in the current passing through them. Following these guidelines, several techniques for reducing the peak current demand have been proposed. Work in [3] reduces the current demand for clock distribution network by operating half of clock buffers in the rising and the other half in the falling edge of the clock. The work in [4] reduces the peak current by either state replication or state re-encoding to minimize the peak switching value of the FSM. Works [1] [2] [5] [6] [7] explore the idea of widening the distribution of the Clock Arrival Times (CAT) to reduce the simultaneous switching of cells and peak current. These methods reduce the overall peak current, however for being ignorant to cell placement, they have limited ability to address the formation of local IR hot-spots.

Our proposed technique reformulates the peak current reduction into many smaller problems of reducing the peak current demanded through each lower level via-stack that connects Metal-1 rails in IR hot-spots to upper PDN metal straps. The proposed technique allows us to reduce the peak current by considering both temporal and spatial arrival time of the clocks, and proves to be very effective in removing IR hot-spots.

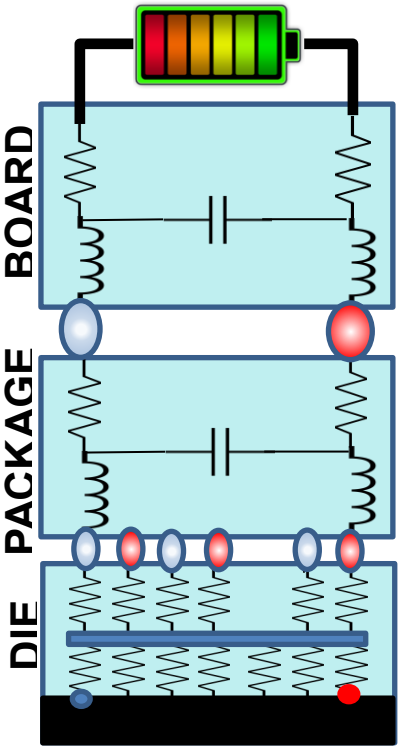

Figure 2. IR drop due to PDN, Package and Board

2 BACKGROUND

To prevent setup and hold timing violation, during the functioning of a chip, on chip variability should be modeled and margined by providing voltage gaurdband. One of the main source of on-chip variations is dynamic IR drop and cycle-cycle voltage variation. The large IR drop or large cycle-cycle voltage variation can cause timing failure. As hold or setup failure of one timing path can make the chip nonfunctional, the margins for IR drop and voltage noise, are determined based on worst case and this is a pessimistic approach. To guard the design against timing failures, during physical design and timing closure, large design margins for IR-drop and endpoint uncertainty are adopted, paying the price in terms of performance, power and area penalties.

With focus on reducing the power demand of the devices like mobile phones and Internet of Things (IoT), designers are doing the design and operation these circuits at Near Threshold voltage (NTV). The impact of IR drop and voltage variation worsens at scaled voltages. With 5% voltage noise in a design that is operated at Super Threshold Voltage (STV), 10-20% performance variation is observed [8].However, the situation becomes far worse when the circuit is operated at Near Threshold Voltage (NTV), where 5% of voltage noise causes more than ~200% performance variation [8]. To prevent on chip variation from causing timing failures, during physical design, appropriately large design margins for IR-drop and endpoint uncertainty (to account for jitter in the result of voltage variation) are adopted. However, the price will be paid in terms of Power, Performance and Area (PPA) penalties, which increase super-linearly at the scaled

voltages to a point that for designs operating at NTV, margin requirements for IR-drop and voltage noise could even eliminate the feasibility of such solutions.

2.1 Improving PPA & peak current by building clock skews

In a pipelined design, the longest stage of the pipelined circuit dictates the overall clock period. Hence the conventional CTS flows that build a clock tree with minimized or zero clock skew will result in little or no timing slack in longer pipeline stages, while building larger unused slacks in shorter stages of the pipeline. A novel idea, to mitigate this problem and to improve the PPA was the introduction of time borrowing technique. In this technique, which is widely adopted by commercial EDAs [9] [10],the unused slack in a shorter pipeline stage is borrowed and is pushed to the subsequent or preceding longer pipeline stage by building useful skews [11], The source and destination registers, for the transfer of timing slack, need not be form successive stages of pipeline; the timing slacks could be moved across multiple stages of pipeline until delivered to the required stage.

In addition to timing closure, the useful skew is also leveraged for reduction of peak current. Each triggering edge of clock initiates a surge of toggle activities on die. However, as signals propagate forward in the combinatorial logic, their toggle activity is quickly suppressed, and thus, their current demand is quickly reduced. Therefore, widening the distribution of CAT, as claimed in [1] [2] [5] [6] [7], reduces the simultaneous switching activities, resulting in reduction in the peak current. These

techniques reduce the overall peak current, but they cannot mitigate the occurrence of IR hot-spots. This is because by distribution of clock's arrival time, there is no guaranty that a subset of registers, that simultaneously switch, are not placed near one another.

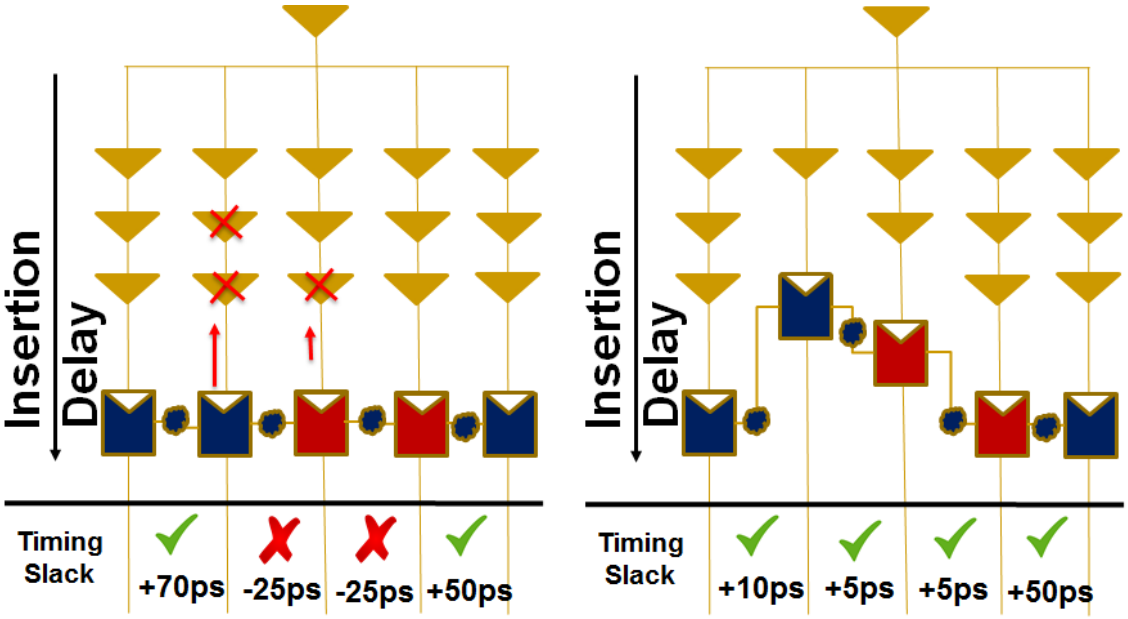

Figure 3. Useful Skew

To reduce IR hot spots along with changing the arrival time of the clock, the information regarding the placement of the cells should be taken into account. This reduces the simultaneous switching of cells that are placed spatially close to one another and this in turn reduces the peak current drawn through its via.

3 BACKGROUND ON POWER DELIVERY NETWORK

In this section, we describe the Construction of a typical PDN in advanced geometry nodes where 9 or more metal layers exist. Physical design process illustrated in Fig. 1, this starts with creating Metal 1 (M1) rails. To this M1 rails the power and ground pins of standard cells are connected. M1 rails are altered between Power (P) and Ground (G), and is implemented by placing filler cells after creating floorplan in the design, followed by pre-routing the power and ground pins and then later these filler cells are removed. This leaves the M1 rails behind. With this process these M1 rails are created such that these are separated by the height of standard cells. With the increase in the current and power density in the scaled geometries like 28nm technology, the M1 rails alone are not capable to meet IR drop requirements. Therefore, M2 rail could be optionally routed in parallel to M1 rails. A batch of higher-level metal straps (usually M7) which are routed orthogonal to M1 rails is then drawn to distribute the current more evenly. These straps are connected to M1 rails at each of their cross-layer intersections by using a via-stack. Choosing the size of via-stack is a physical design tradeoff; larger via-stacks reduce the resistive IR drop, however consume more routing resource.

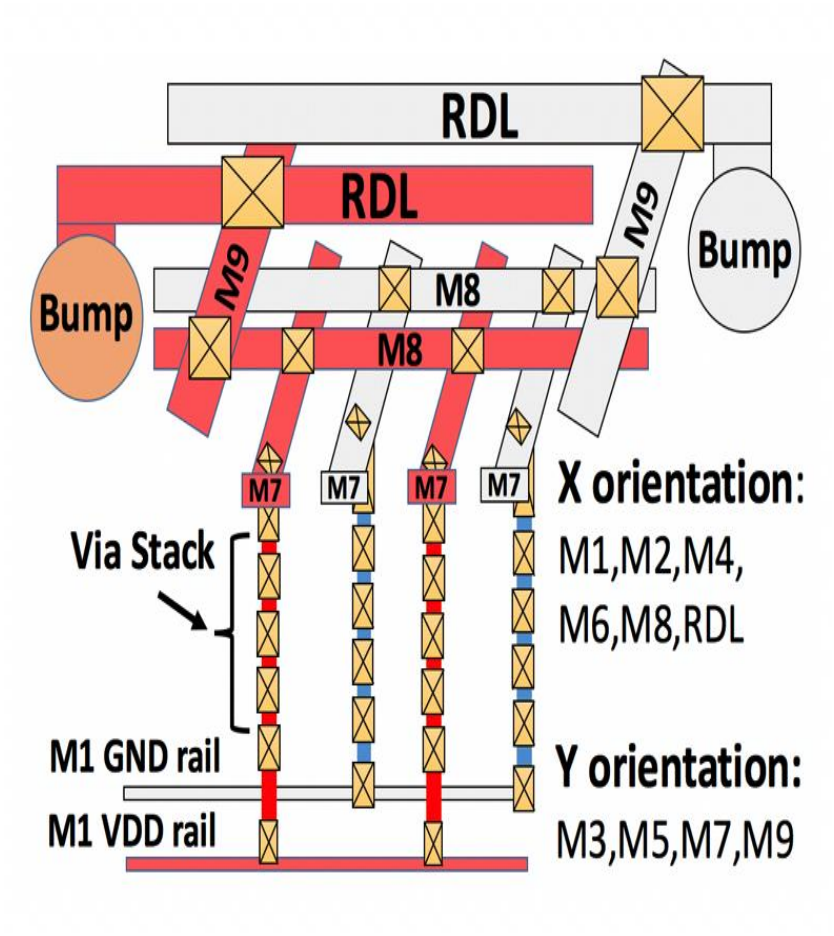

Figure 4: Power Delivery Network

Upper PDN metal layers (M8 & M9) are progressively made wider and will be connected to lower level PDN to evenly distribute the current across the chip. PDN is then extended to the Re-Distribution Layer (RDL) to further distribute the current and to connect the PDN to bumps that interface the on chip and the package PDN. Package is responsible for inductive IR drop.

In Static Timing Analysis (STA) delays are calculated based on a fixed voltage, however, in reality each cell experiences a unique voltage waveform; this voltage waveform is a function of the switching activity of nearby cells and parasitic signature of on-chip PDN, package and board. The effect of the supply voltages of two cells reduces, as cells are placed apart by sharing a smaller portion of PDN.

Considering the structure of a typical PDN, the simultaneous switching of cells, may lead to formation of local IR-hot spots when placement of the cells ties their power and ground pins to the most resistive section of PDN. In this case the demanded current for simultaneous cell switching integrates over the M1 rail and lower level via stacks. M1 rail and lower level via stacks are highly resistive, which lead to large instantaneous IR drop. In this work, to mitigate the intensity of IR hot-spots we consider the relative placement of cells and their connectivity to the PDN while scheduling the clock arrival times to address the peak current reduction and IR hot-spot mitigation at the same time.

4 BACKGROUND ON TIMING

We proposed that depending on the placement and location of high IR drop cells and their timing window, and the available slack in their timing paths, we can fix the IR hot spot problem with clock skew adjustment.

Timing delay of a cell depends on the supply voltage of the cell when the input signal reaches the cell. Due to IR drop in PDN, different cells in the design will see different voltage even though supply voltage is constant. As shown in below diagram.

Vias are considered as source of current at M1 layer for all the cells. When there is simultaneous switching of cells and if these cells are sharing same via stack for drawing current then this leads to additional current demand through the via-stack and M1 rails and this leads to a larger IR drop. Figure 5 shows the example layout of cells after cell placement. If the cells colored in yellow share a portion of their switching window, and they could toggle at the same time. As they are sharing same MRP the current demand through shared via in MRP, for the duration of activation of both cells is high. This instantaneous high current surge causes larger resistive and inductive drop.

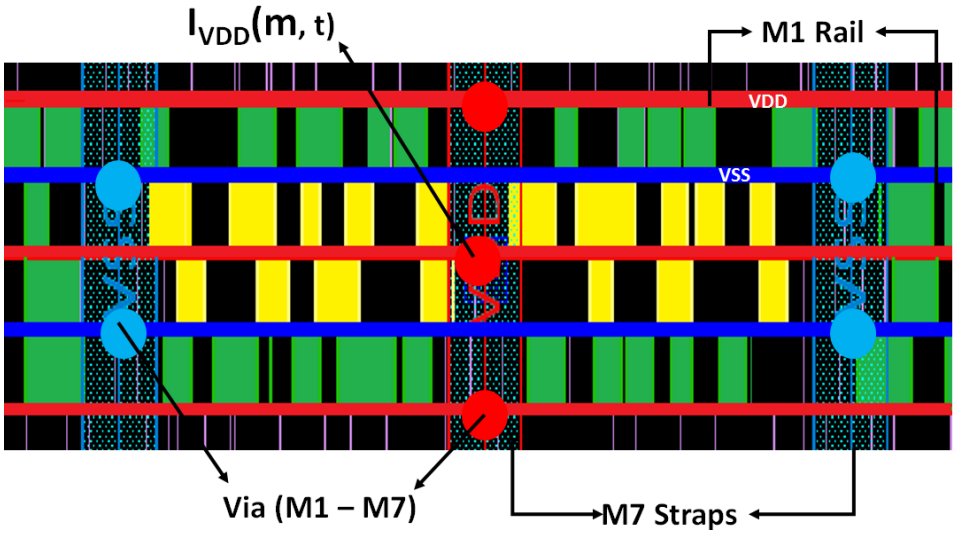

Figure 4. Simultaneous Switching of cells in MRR

MRP is the minimum resistive path from a cell to a bump or a pad. For the type of PDN that we have described earlier will have a distinct MRP for each of the PG pins of each cell. For example, in case of any cell, the minimum resistive path)MRP) for VDD pin or VSS pin is path from M1 rail, towards the right or left leading to the closest via stack, going up the via-stack, then to closest Via7 and going through the shortest resistance path in upper metal layer till the closest bump or wire bond is reached. The MRP carries the largest current to the cell.

Consider that cells colored yellow are sharing the same MRP and the simultaneous activation of these cells will have an additive effect on current in the shared MRP. The Cells of they do not share large part of MRP, then there will be little impact when switched at the same time as cell A.

From this background provided it is shown that by changing the activation timing window of closely located cells with overlapping switching window (timing window) can reduce the instantaneous peak current through the via and thus reduce the IR drop in lower layers of PDN. In addition, as explained, the switching activity is highest at the beginning of a clock cycle and is reduces very quickly as signal propagates through the timing path. By distributing the arrival time of the clocks in a MRR region can reduce simultaneous switching and instantaneous peak current demand leading to reducing the IR hot spots.

5 METHODOLOGY AND ALGORITHM

To simultaneously reduce the peak current and the intensity of IR hot-spots, as illustrated in Fig. 3, we break the problem of overall peak current reduction into many smaller problems of via stack peak current minimization; The most resistive section of the PDN is the M1-rail and the via stack that connects the M1 to the wider upper layer (M7) metal straps. Considering that the M1-rails and lower level via-stacks are highly resistive, they are the most contributing elements to the formation of high-IR regions. Therefore, if the integral of the current, which is demanded through each lower level via stack could be lowered, the intensity of IR hot-spots could be greatly mitigated.

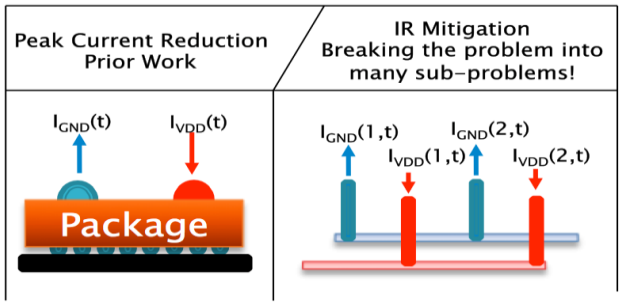

Figure 5. Breaking the overall peak current reduction problem into many smaller via-peak-current minimization problems.

A PDN, which is constructed as explained in section II.B, has a regular mesh structure. Therefore, for a given standard cell, via stacks closest to the power and ground

pins of that cell are parts of its (Ground and Power) MRP. Most of the current delivered or returned to/from a cell, runs through its MRP. Table I. defines a few other terms that are used in our formulation.

TABLE 1. ABBREVIATIONS AND DEFINITIONS

Term	Definition
D	Distance between neighboring via stacks
H	Height of standard cells
V[i]	i-th via-stack in MRP region
MRR(via[i])	The region bounded by equations (1) and (2). The min resistive path for all cells in this region goes through via[i]
X(FF[i]), X(V[i])	Cartesian X location of FF[i] or V[i]
Y(FF[i]), Y(V[i])	Cartesian Y location of FF[i] or V[i]

Problem formulation: For each via V[i], and all flip-flops FF[j] that satisfy the two conditions below, schedule the clock arrival time such that the peak current demand through V[i] is minimized.

$$X[V[i]] - \frac{D}{2} < X[FF[j]] < X[V[i]] + \frac{D}{2} \qquad (1)$$

$$Y[V[i]] - H < Y[FF[j]] < Y[V[i]] + H \qquad (2)$$

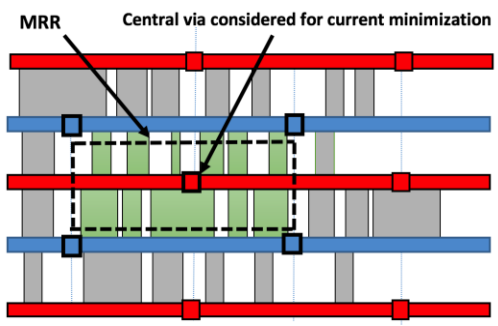

Figure 6. Minimum Resistive Region (MRR) of the central via

In other words, considering each via stack as a source or sink for the current, we are aiming to schedule the arrival time of the triggering edge of the clock to the clock pin of each FF in MRR such that the expected simultaneous switching of FFs and the expected current demand through via is minimized. Note that satisfying conditions (1) and (2), as illustrated in the example given in Fig. 4 ensures that FFs are in the MRR of the via-stack considered for peak current reduction.

The simultaneous switching of FFs in the same MRR has an additive effect on the demanded current in the shared MRP. When scheduling the arrival time of FFs, their size and output load should also be considered. To account for cell strength and output load variation, we built a simple yet effective model: The current that each FF draws during the switching will be will be directly proportional to its output load $\boldsymbol{C_L}$, and inversely

proportional to its propagation delay $\boldsymbol{T_p}$. Let's define Expected Current Demand (ECD) of a FF as:

$$ECD = C_L . T_p \quad (3)$$

The capacitive load of the FF ($\boldsymbol{C_L}$) is obtained by adding FF's internal capacitance, output wire capacitance and fan-out gate capacitances, and the propagation delay through the FF ($\boldsymbol{T_p}$) is obtained from graph based timing analysis.

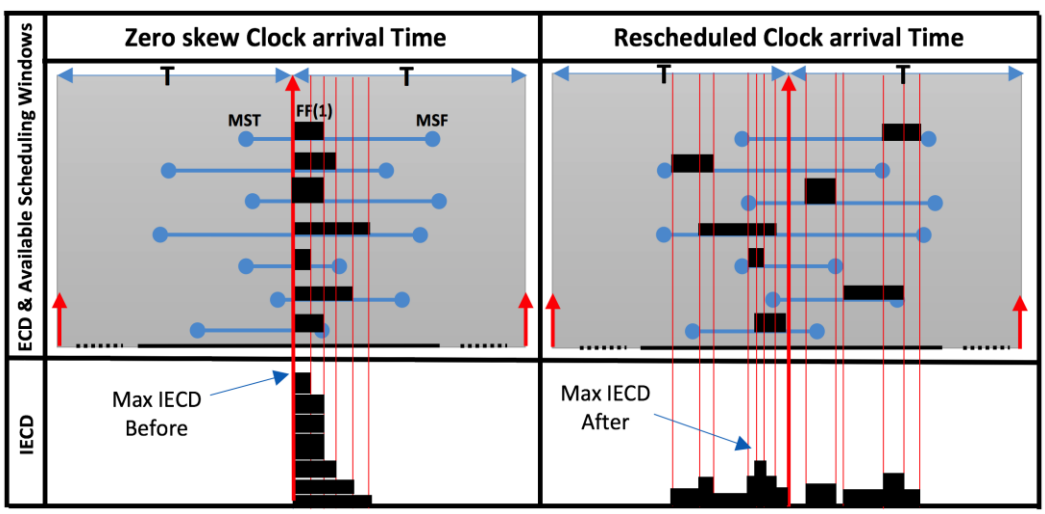

Figure 7. Deriving the IECD from ECD of all FFs in MRR.

To schedule the clock arrival times, first, the ECD of each FF in the MRR of interest is computed. This is illustrated in Fig. 5 (left). Each black rectangle represents a FF. The height of the rectangle is the ECD of that FF, and the width of the rectangle is

the propagation delay of that FF. The blue line, associated with each FF, shows the range in which that FF could be scheduled. This range is defined as the scheduling window of each register. Scheduling windows are computed by analyzing the available slack "**to**" and "**from**" each FF. Fig. 9. Illustrates an example on how the scheduling window of register FF is obtained. In this example, the minimum available timing slack from start-points S1, S2 and S3 to flip-flop FF is that of S2→FF with 1.0ns of slack. The smallest slack from FF, as a start point, is that of FF→ E1 with 0.5ns. Therefore, without causing timing violation, the arrival time of the clock to the clock pin of FF could be skewed within this scheduling window, spanning a scheduling window of width 1.5ns. Note that scheduling window could be easily extended by considering multiple pipeline stages. For example, if there exists available slack for all timing paths starting from E1, the arrival time of clock to E1 could be skewed and pushed out by 0.5ns, making it possible for FF to be skewed late by 1ns, instead of 0.5ns.

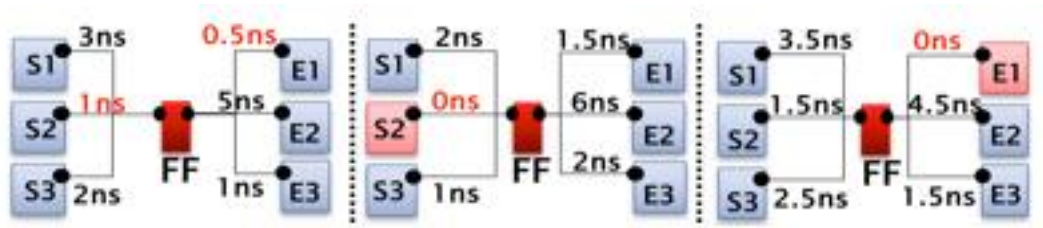

Figure 8. Timing slack transfer using CAT scheduling

To roughly obtain the demanded current signature over time, the ECDs of all FFs are integrated over two consecutive clock cycles. The Integrated ECD (IECD) graph is divided into multiple ECD-Slices (ECDS). The boundary of each slice is defined by the start and end-point of the timing windows of individual FFs. As illustrated in Fig. 5. (left), the maximum IECD, for a zero-skewed clock tree, happens in the first ECDS slice. Our proposed IR-mitigation technique skews the clock arrival time of FFs in a MRR region, within their available scheduling window, to minimize or considerably reduce the peak value of IECD in any ECDS slice.

5.1 Explanation of the Algorithm:

The pseudocode in Fig. 7 provides a detail description of the algorithm used to implement the proposed solution. The flow consists of 3 steps: (1) performing IR analysis, (2) identifying IR-hot spots, and preparing a clock skew plan, (3) implementing the clock skew by running incremental CTS.

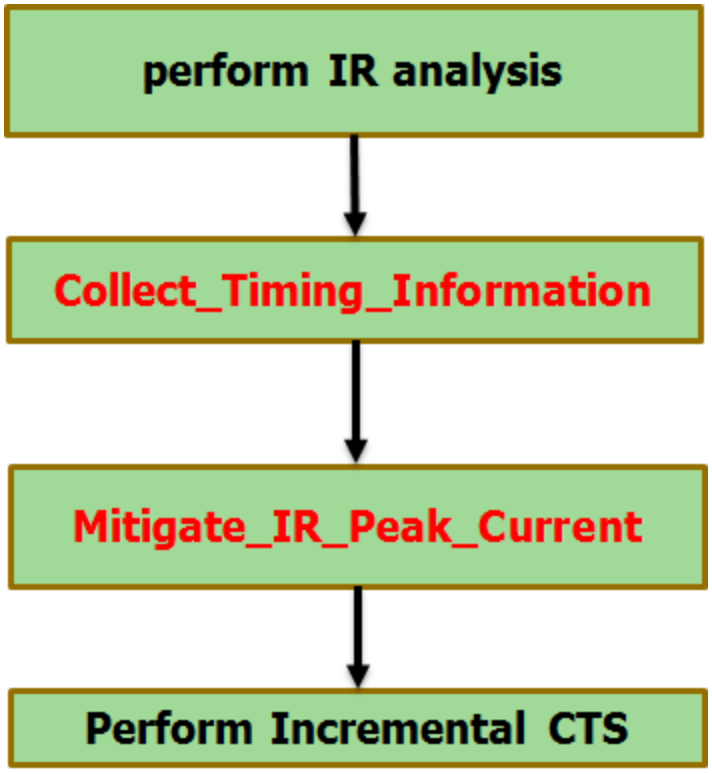

Figure 9. IR Mitigation Flow

The second step is the heart of our work. In this step, we first find the available scheduling window of each FF in the MRR using the function **Collect_Timing_Information**.

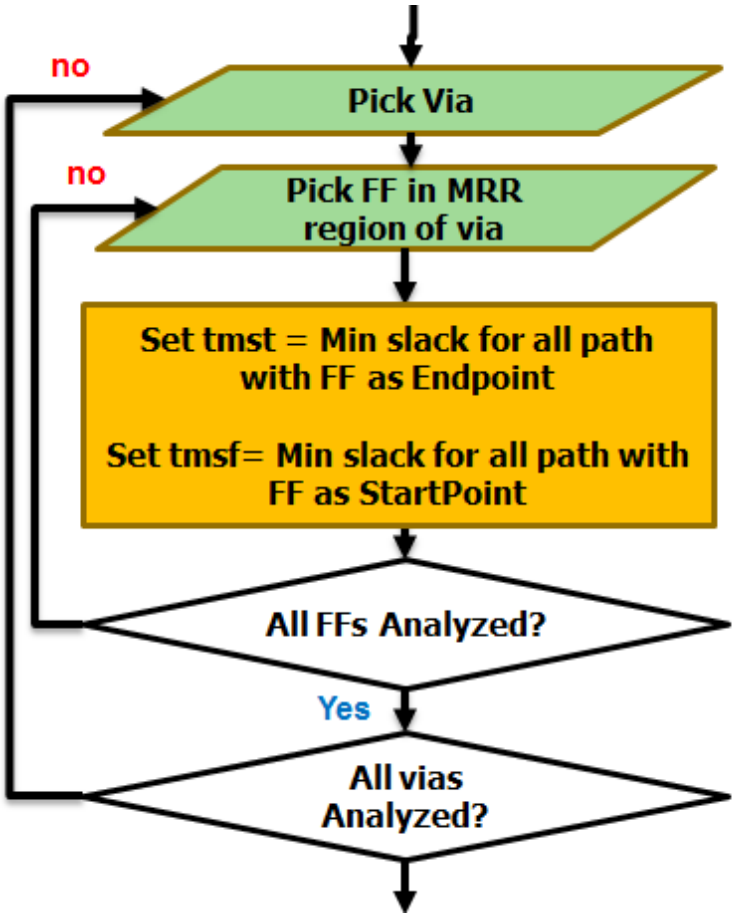

Figure 10. Collect Timing Information

Then the arrival time of each FF is scheduled to have the maximum time difference with the arrival time of zero-skewed clock by pushing it as early or as late as possible. This step alone, reduced both peak current, and IR-hot spot intensity, but doesn't eliminate the chances of FF simultaneous switching. In order to further reduce the intensity of IR-hot spots, multiple rounds of analysis and optimization is applied. In each round, the IECD of the newly scheduled clock distribution is computed, and the ECDS

slices with maximum/largest expected demand current (due to simultaneous switching) are identified.

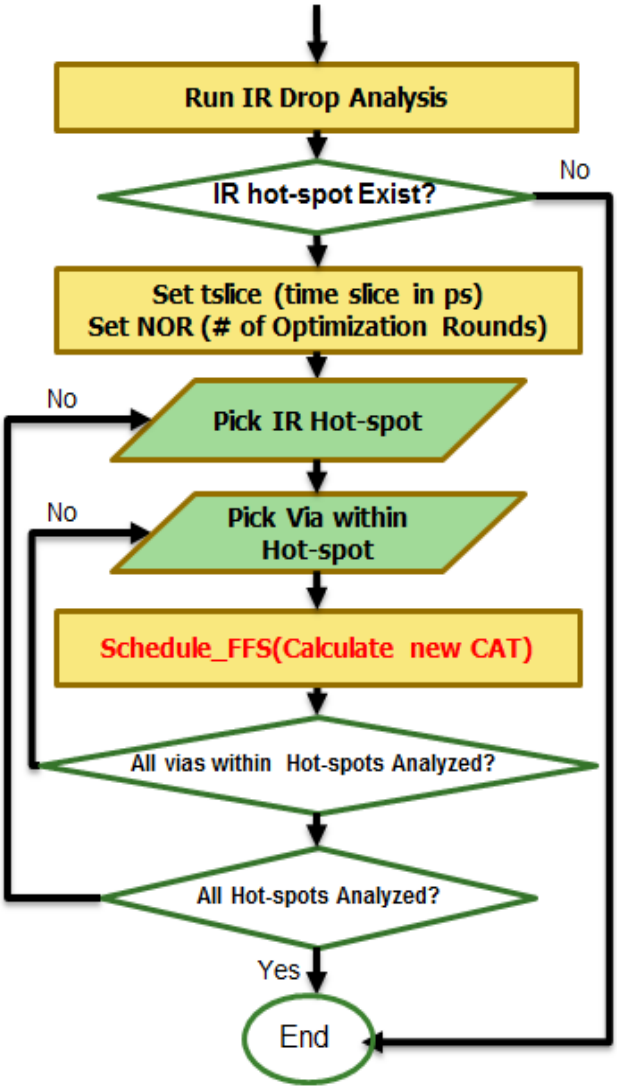

Figure 11. Mitigate_IR_Peak_Current

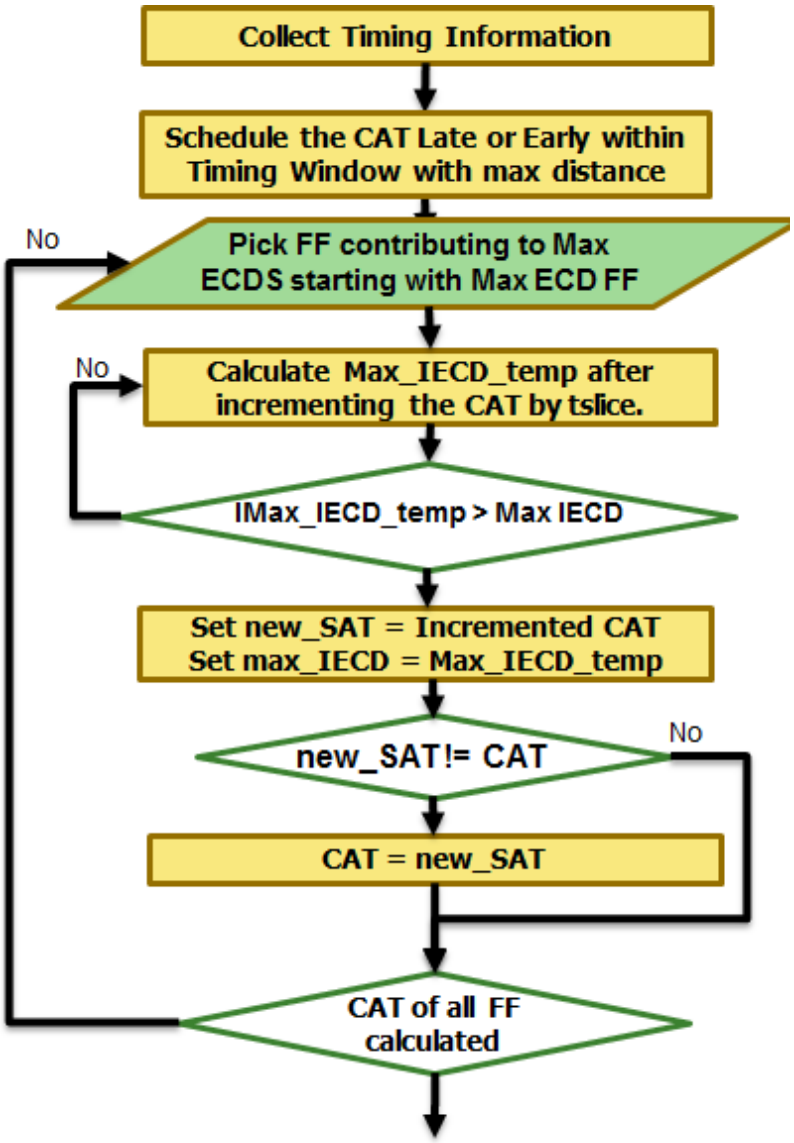

Figure 12. Schedule _FFS

The maximum expected current value of all ECDS slices in an IECD curve is computed using **max_IECD** function. The FFs contributing to the max_IECD, which are

a small subset of the original FFs, are flagged. Then the arrival time of each flagged FF is swept, using small timing steps. At each step a new IECD (IECD_temp) is computed. If the IECD_temp has a lower max_IECD value, the new arrival time of the clock for that FF is recorded, and the IECD_temp replaces the existing IECD. When all FFs contributing to the maximum current ECDS slice are re-scheduled, one optimization round is concluded. **NoR,** in this pseudocode, is the number of times that the above Peak ECDS current reduction flow would run. NoR should be experimentally obtained. Setting up the NoR to a small number, may lead to existence of some simultaneous switching in spatially close registers, when the situation could have been fully avoided. Setting the NoR to a very large number and resolving all or most timing-window overlaps, may lead to scheduling the clock arrival times closer and closer to the zero skew clock. This reduces the local resistive IR drop, however may increase the overall peak current, contributing to larger inductive IR drop.

```
Mitigate_IR_and_Peak_Current () {
|  Run IR drop analysis
|  If high intensity IR regions exist
|  |   Set tslice = small time slice (e.g. 5ps)
|  |   Set NoR = 5; // Number of optimization Rounds
|  |   For each IR-hot spot {
|  |  |  For each via(i) {
|  |  |  |  Schedule_FFS (NoR, tslice, Via[i])
|  |  |  }
|  |  }
|  Run CTS to implement the scheduled clock arrival times
}
```

```
Schedule_FFS (int NoR, int tslice, struct via) {
|  Collect_Timing_information(MRR[via[i])
|  Schedule the arrival time of all FFs to be at
|        max distance from early edge of the arriving clock
|        by pushing them as early or as late as possible.
|  Compute the IECD
|  For (i=1; i<NoR; i++) {  // rounds of optimization
|  |  For each FF[i] contributing to max ECDS,
|  |                 in the descending order of ECD per FF {
|  |  |  For tt = tmst[i]; tt<tmsf[i]; tt+=tslice {
|  |  |  |  Set arrival time of FF[i] to be tt.
|  |  |  |  Compute the new IECD → IECD_temp
|  |  |  |  if max_IECD (IECD_temp) > max_IECD(IECD) {
|  |  |  |  |  set new_SAT = tt;
|  |  |  |  |  set IECD = IECD_temp;
|  |  |  |  }
|  |  |  }
|  |  |  if new_SAT != current arrival time {
|  |  |  |  Schedule the clock arrival time of FF[i] to be "new_SAT"
|  |  |  |  Annotate the FF with required book keeping information.
|  |  |  }
|  |  }
|  }
}
```

```
Collect_Timing_Information (MRR) {
|  For each FF[i] in the MRR[via[i]] {
|  |  Set tmst[i] = The min slack for all paths ending at FF[i]
|  |  Set tmsf[i] = The min slack in all timing paths starting from FF[i]
|  }
}
```

Figure 13. Algorithm to reduce IR hot spot

We acknowledge that there is room for improving this algorithm. Rescheduling the clock arrival time of a FF will shift the timing window of all cells in its proceeding timing paths, which may result in formation of an IR hot-spot elsewhere. Although a

valid concern, in actual this is not a issue because the toggle rates reduce very quickly; therefore, although timing overlap may happen, because of the reduced probability of switching, the actual re-occurrence of simultaneous switching is less probable. The algorithm can be executed multiple times to mitigate the occurrence of new IR hot spots. In addition, this algorithm doesn't consider the switching activity of other cells (non-sequential cells) in the region. Although the switching activity depresses very quickly in the first few stages of combinatorial logic, considerations for expected current demand of the first few cells in each timing path, which experience higher switching activity, could improve our proposed clock arrival time scheduling algorithm and may lower the peak current and max IR drop. These issues are being addressed in our future work.

Impact on timing: Our proposed technique for IR hot-spot mitigation reduces the intensity of IR hot spots and improves the circuit timing by (1)removing the local hot spots, the mean supply voltage seen by standard cells is higher, and therefore they are faster. (2) By distributing the clock arrival time, the frequency of voltage variation reduces; therefore, uncertainty margin during the STA analysis can be reduced. (3) The accumulative impact of distributing the arrival time of FFs, reduces the overall peak current (battery demanded current), reducing the cycle to cycle voltage noise, which could be modeled by reducing the margin during the timing closure.

6 EXPERIMENTAL RESULTS

Our proposed peak current and IR hot-spot mitigation technique was tested on selected number of larger IWLS [12]benchmarks. Synopsys's Design Compiler Topographical (DC-Topo) [13]was used to synthesize each benchmark, and the Synopsys IC Compiler (ICC) [10]was utilized for floorplaning, PDN construction, cell placement, clock tree synthesis, and wire routing. The proposed flow is written in TCL, which is the native scripting language in ICC's shell. The runtime overhead of the scheduling algorithm is negligible (~1%) when compared to the run time of incremental CTS needed for implementation of scheduled clock arrival times. The overhead of incremental CTS, to implement the scheduled clock arrival times, varies between 5% to 40% of the run time of the original CTS. For the results reported in this section, all designs are subjected to a single round of analysis and mitigation.

The IR drop is calculated using Apache RedHawk [14]. For the purpose of this simulation, a lumped package inductance of 150pH and a lumped package resistance of 2.0mOhm is considered.

6.1 IR drop improvement

Fig. 8 illustrates the effectiveness of our proposed algorithm in mitigating IR hot spots. In this figure the IR map of a DES Crypto Engine before and after the application of the proposed algorithm is illustrated. As demonstrated, the IR hot-spots are completely mitigated.

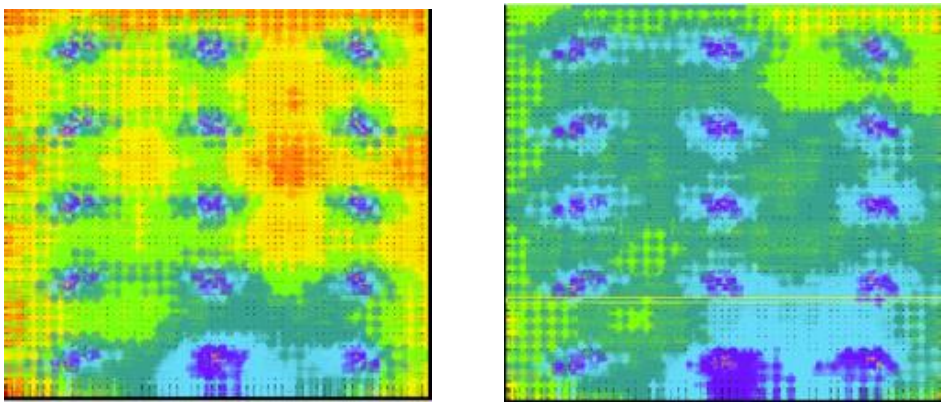

Figure 14. IR hotspot regions before (left) and after (right) the application of IR-mitigation technique.

Fig. 9 illustrates the distribution of IR-drops for all cells in the design. Application of the proposed algorithm reduces the intensity of IR drop and pulls in the tail of IR-drop distribution. In this benchmark, the worst IR-drop is improved by ~29%. For having a tighter distribution of voltages, the mean IR-drop of the entire design has also improved by ~9%.

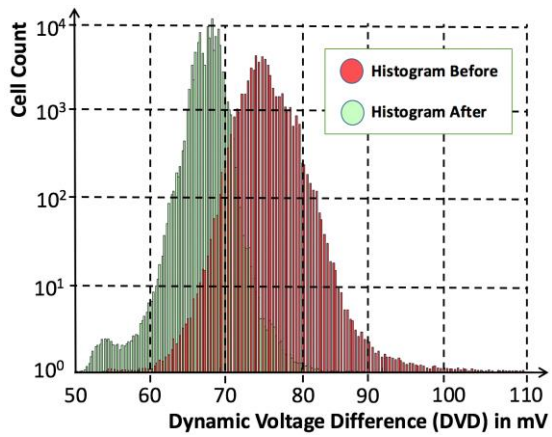

Figure 15. IR improvement after application of the proposed technique

Table II summarize the IR drop improvement obtained for the other implemented benchmarks. As demonstrated, after application of the proposed algorithm, the worst-case IR drop improves between 21%~35%, and mean IR drop improves between 7%~11%, depending on the benchmark. In addition, Table II captures the improvement in the IR drop, when it is averaged over the worst 10, worst 1000 and across all cells.

TABLE II. COMPARISION OF SEVERAL DESIGNS BEFORE AND AFTER APPLYING PROPOSED ALGORITHM

			Worst DVD			Percentage Reduction in			
Design	Cell Count	Reg Count	before (mv)	after (mv)	% reduction	top 10 cells	top 1K cells	all Cells	Iavg(A)
DES	45787	8808	116	82	29.31%	27.12%	16.18%	9.08%	31.12%
Ethernet Mac	33437	10545	89	58	34.83%	32.14%	19.41%	10.62%	26.11%
AES	105116	1595	82	65	20.73%	20.49%	12.09%	7.45%	16.34%
b19	12384	1485	81	57	29.63%	29.37%	21.37%	7.15%	37.04%

6.2 Peak current reduction

The primary objective of the proposed algorithm is to reduce the intensity of IR hot-spots, still it is effective in reducing the peak current as it widens the distribution of clock arrival times to reduce the via current densities. Fig. 10 illustrates the impact of the proposed algorithm in reducing the peak current demand of the DES Cryptography Engine by 31%. The reduction in the peak currents of few other benchmarks are summarized in table II. The proposed technique achieves 16%~37% reduction in the peak current. Note that the proposed algorithm could be skewed to maximize the IR hot-spot mitigation or peak current minimization. However, the two are somewhat correlated.

In terms of peak current reduction, results obtained from this technique are comparable and in range of those reported in the previous work [1] [2] [5] [6] [7]. However, in the previous work there is no regard for IR hot-spot mitigation. Therefore, although it is possible for techniques proposed in the previous work to achieve comparable peak current reduction, they will not be able to minimize the local peak currents densities to mitigate local IR hot spots.

If maximum peak current reduction is desired, NoR should be set to a small number (possibly 1 or 2), and in an extreme case, the algorithm could be modified to touch a larger number of MRRs, or even every MRR in the design to minimize the peak current. However, visiting and optimizing all MRR regions, will create a heavy workload

for the incremental CTS, may require very long runtime, and could result in substantial increase in the number of inserted buffers.

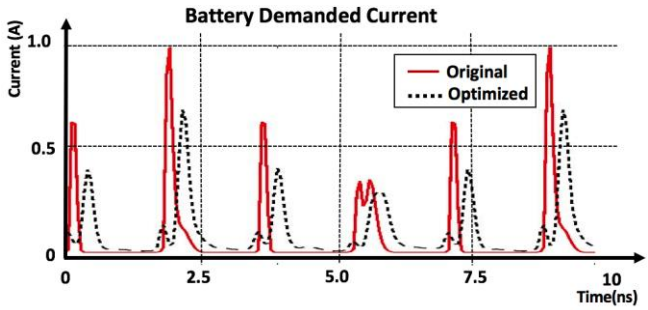

Figure 16. Reduction in the peak current demand

7 PHYSICAL DESIGN AUTOMATION TOOL

7.1 Introduction.

The main steps in the physical design flow are:

- **Synthesis:** Synthesis converts the RTL design usually coded in VHDL or Verilog HDL to gate-level descriptions which the next set of tools can read/understand. This netlist contains information on the cells used, their interconnections, area used, and other details.
- **Floor planning:** determines the shapes and arrangement of sub circuits or modules, as well as the locations of external ports and IP or macro blocks. Design of Power delivery network.
- **Placement:** Finds the spatial locations of all cells within each block.
- **Clock-tree Synthesis (CTS)** : Determines the buffering, gating (e.g., for power management) and routing of the clock signal to meet prescribed skew and delay requirements.
- **Routing** : allocates routing resources that are used for connections; example resources include routing tracks and assigns routes to specific metal layers and routing tracks within the global routing resources.
- **Physical Verification :** Preforming DRC, LVS, Antenna rule checking, Electrical rule checking (ERC)

- **Timing closure:** optimizes circuit performance by specialized placement and routing techniques.

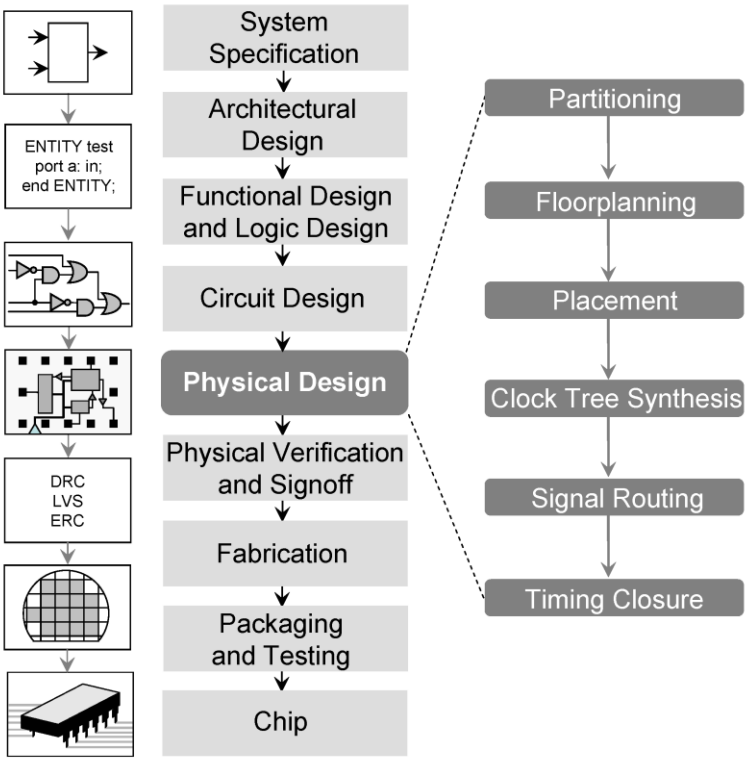

Figure 17. Physical design process

Tools used for performing these steps of Physical design.

- Synthesis is performed using Synopsys Design Compiler
- Floor-Planning, Placement, Clock Tree Synthesis and Routing is performed using Synopsys ICC tool.
- Timing closure is performed using Synopsys Primetime.

These steps are performed using the combination of various API's provided by these tool and TCL (native scripting language on these tools). So It is very tedious to perform each of these steps manually. So Scripts are created using TCL and tool specific apis for performing each step and these scripts are executed on different designs and by providing various inputs like cell library, constrain files and ect. Execution time is large and is also dependent on the size of the design. More number of cells more the time. Even using scripts performing these steps independently is a tedious and time consuming. And management of all steps input and output is also a tedious and difficult work.

So to make physical desing process flow easy, Physical design automation tool is designed and implemented. Using this tool a single command can perform complete physical design flow. This is implemented using GNU make tool.

7.2 Features of Physical design automation tool:

- This Automates Physical Design process flow.
- Provided with name tagging of a the work.
- Can run tool on different designs simultaneously.
- Has a well-defined folder structure for future reference.
- Allow to change Configuration and run the Physical Design process flow.

- Allows to use custom scripts for a specific stage(Synthesis, Floorplan, Placement, CTS, Route)
- Allows to Branch from exiting design at one stage and do rest of the process.
- Keeps track of all tasks done on specific design.

7.3 Usage

Make <TARGET> design = <DESIGN_NAME> stage= <STAGE> tag =<TAGNAME> input = <INPUT_PATH> config =CONF_NAME> output_tag=<Branch_name>

TARGET : pd → physical design

clean → Remove design or stage

help → help

load → Load the design output from specified stage

stat → shows the status of the design

history → shows the history of commands executed recently

DESIGN_NAME : Name of the design

STAGE : all → Does all stages (input path parameter mandatory)

RTL →Just copies the inputs to RTL folder for future reference

DC → Synthesis

FP →Floorplan

Place →Cell Placement

CTS → Clock Tree Synthesis

Route → Signal Routing

TAGNAME : Identifier tag for work

CONF_NAME : if not specified default configuration will be used, if specified will search for CONF_NAME.tcl in Configuration folder

Branch_name : Used for creating a branch from previous stage resutls in TAG and created output TAG would be TAG_ Branch_name

7.4 Sample Usage

```
make help
make clean design=rca64 tag=all
make clean design=rca64 stage=FP tag=TAG17
make pd design=rca64 stage=all tag=TAG17 input =./Inputs/rca64
make pd design=rca64 stage=RTL tag=TAG17 input =./Inputs/rca64
make pd design=rca64 stage=DC
make pd design=rca64 stage=FP tag=TAG17
make pd design=rca64 stage=Place tag=TAG17
```

make pd design=rca64 stage=Route tag=TAG17

make load design=rca64 stage=FP tag=TAG17

make load design=rca64 stage=Place tag=TAG17

make load design=rca64 stage=Route tag=TAG17

make pd design=rca64 stage=FP tag=test1 output_tag=abc

make stat design=rca64

make stat design=rca64 tag=test1

7.5 Steps to use

First time :

Copy Golden_Folder to Home Directory

Cd into Golden_Folder

Test your setup :make pd design=rca64 stage=all tag=test input =./Inputs/rca64

Design Specific

- Update <design>.tcl file in Golden_Folder/Design_Specific/ With design specific data :
    - Example:

      set RTL_SOURCE_FILES "half_adder.v full_adder.v rca64.v

      set SDC_File rca64.sdc ;

set DESIGN_NAME "rca64" ;#

- Create a folder with input Verilog or vhdl files and .sdc file into a folder. Preferably into /Golden_Folder/Inputs/
- Start Using the make tool

Change Configuration

make pd design=rca64 stage=all tag=TAG17 input =./Inputs/rca64 config=New_config

- Create New_config.tcl in \Golden_Folder\Configuration\
- To make new config as default → rename the New_config.tcl to default.tcl and make a back up of existing default.tcl to other config.tcl

Use custom scripts

- Initially make RTL and provide the input path
- make pd design=rca64 stage=RTL tag=test_custom input =./Inputs/rca64
- Then create custom script files (dc.tcl, ICC_FP.tcl, ICC_Place.tcl, ICC_CTS.tcl, ICC_Route.tcl) based on stage you want to run custom script and place into /Designs/<design>/<tag>/ custom_scripts folder.

- Then continue using make as usual. When make finds a custom script, it would use the custom script else it would use the default script provided in Scripts folder.
- Note : the name of the custom scripts should be same as default scripts and should be placed in custom_scripts folder. (this custom_scripts folder is generated only after RTL stage)

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BIOGRAPHY

Bhoopal Gunna is a candidate for Master of Science in Electrical Engineering, with a specialization in VLSI Design and Embedded System from George Mason University. He has been a member of Dr. Avesta Sasan's research lab, since December 2015. He received his Bachelor of Engineering in Electrical and Electronics Engineering from JNTU University, Hyderabad, India.