

COMPENSATION FOR THRESHOLD INSTABILITY OF THIN-FILM  
TRANSISTORS

by

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A Thesis  
Submitted to the  
Graduate Faculty  
of  
George Mason University  
in Partial Fulfillment of  
The Requirements for the Degree  
of  
Master of Science  
Electrical Engineering

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Compensation For Threshold Instability Of Thin-Film Transistors

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## **DEDICATION**

I dedicated this thesis to my parents Gina, Roberto Sr., my wife Mildre, my two wonderful children Sebastian and Santiago.

## **ACKNOWLEDGEMENTS**

I would like to thank my family, friends, and supporters who have made this happen. In addition, I would like to express my gratitude to Dr. Dimitris E. Ioannou for guide me during the past years and for the opportunity to conduct research under his supervision. Furthermore, my special thanks to the committee for their time and consideration.

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## **ABSTRACT**

### **COMPENSATION FOR THRESHOLD INSTABILITY OF THIN-FILM TRANSISTORS**

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George Mason University, 2017

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Organic Light Emitting Diode (OLED) has attracted an incredible interest for display applications due to benefits such as a wide viewing angle, high contrast ratio, vivid color, low power consumption, high response speed in comparison to Liquid Crystal Display (LCD). OLED displays do not require backlight and it can display deeper black color than LCDs. The fast response and self-emissive nature of OLEDs have made this technology a good candidate for three-dimensional displays. The thin and light structure of OLED displays have create a strong interest for researcher to advance the OLED's technology into flexible and transparent displays.

However, the uniformity of the image of OLED displays have been affected by the degradation of OLEDs and by the instability of the threshold of thin-film transistors (TFTs) utilized in the pixel area in displays known as Active-Matrix Light-Emitting

Diodes (AMOLED) displays. TFTs backplane are required for switching and driving current to OLEDs in AMOLED displays. Driver-TFTs are responsible to provide current to each pixel of the AMOLED displays. Subsequently, if the driver-TFTs provide a small variation in the current, then the variation can be distinguished as non-uniformity by the user or MURA effect. The human eyes are very sensitive to changes in luminance and can perceive MURA effects produced by the display. Therefore, there is a recognized need for urgent progress in the display technology to achieve better display quality at a low cost, fast response and accurate compensation.

Currently, several approaches are under investigation and/or evaluation in order to compensate the deterioration of the TFT and/or OLED. However, the speed of the compensation, accuracy of the compensation and the impact of the display resolution are still a concern. Therefore, this thesis describes new driving methodologies and circuit schematics for compensating the instability of threshold of thin-film transistor (TFT) and degradation of organic-light emitting diode (OLED) achieving improvements in the accuracy of the compensation and speed of the circuits.

## **CHAPTER 1 INTRODUCTION**

Over the past years, various categories of flat panel display devices have been developed to replace cathode ray tubes that are heavy and have a large volume. Organic Light Emitting Diode (OLED) display is a category of flat panel display device in which an organic compound is used as a light-emitting material and displays an image by using an organic light-emitting diode generating light due to the recombination of electrons and holes [1] [2]. OLEDs have attracted an incredible interest for display applications. Currently, OLED is considered as the most potential display device. Regularly, OLED displays and Liquid Crystal Display (LCD) are compared side by side [1], where is evident that OLED displays possess several benefit and superior properties than LCD. For example, OLED displays require fewer components than LCDs [1], possesses a wide viewing angle, high contrast ratio, vivid color, low power consumption, high response speed [3][4] than LCDs. The fast response and self-emissive nature of OLEDs have made this technology a good candidate for three-dimensional displays. The thin and light structure of OLED' displays have create a strong interest for researcher to advance the OLED's technology into flexible and transparent displays. Thus, OLED displays have achieved high quality luminance and color purity and are relatively thin and light-weight. The vast number of benefits emerge an immense interest in the current field of the art.

## 1.1 Introduction to Organic Light Emitting Diode

OLEDs are a unique technology, based on the use of organic molecules to conduct large amounts of charge, which recombines to emit light that is bright enough for displays or general lighting. Through electron-hole recombination, a high-energy molecular state is formed. This state is called an exciton, as it behaves like a single molecule with high energy. This exciton generates light after an exciton lifetime period as depicted in Figure 1. The wavelength of this light emission corresponds to the exciton energy, so it is possible to control the color of the emission by adjusting the molecular design of the color center [1].

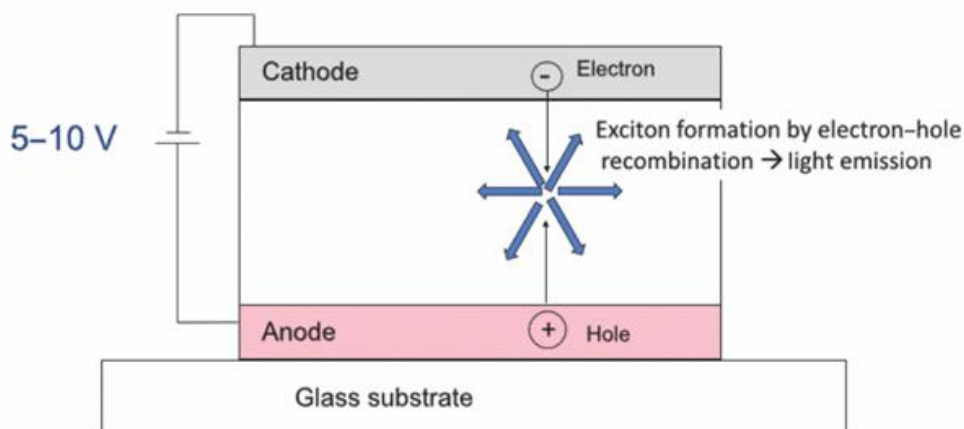


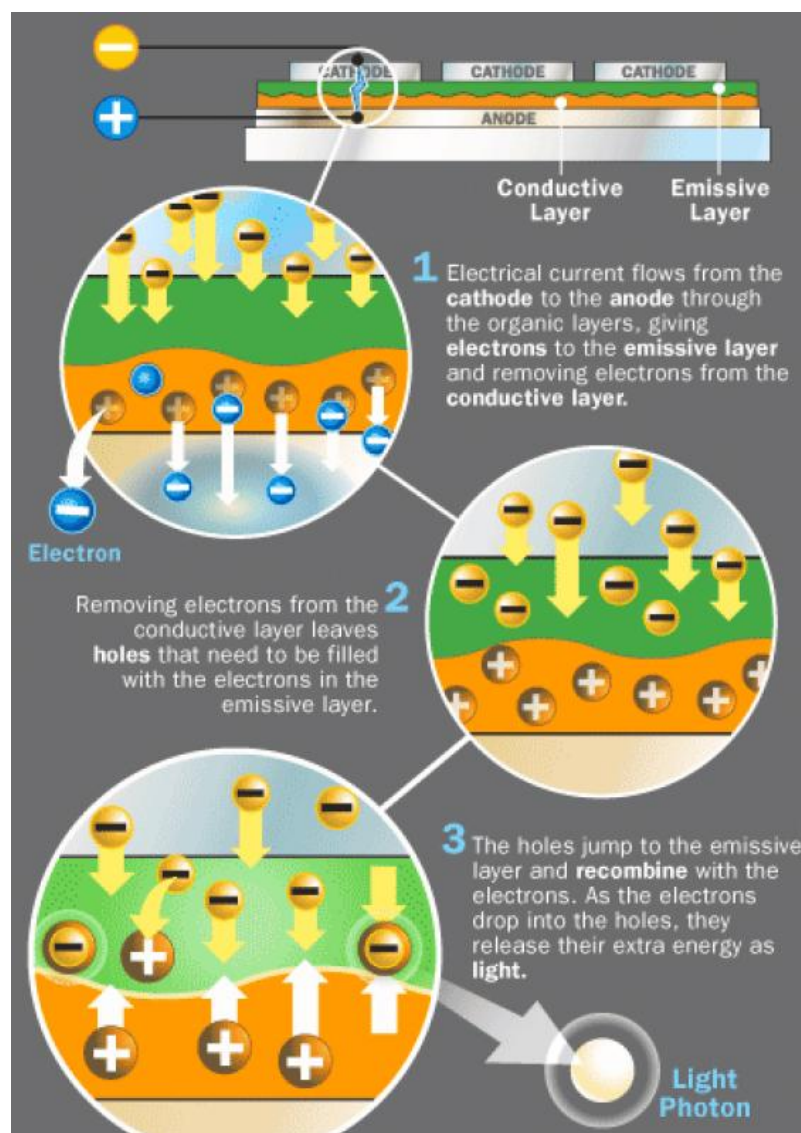
Figure 1: Diagram of the OLED mechanism

OLED display devices include organic molecules or polymers, which are sandwiched between two charged electrodes. One is metallic cathode and the other is a

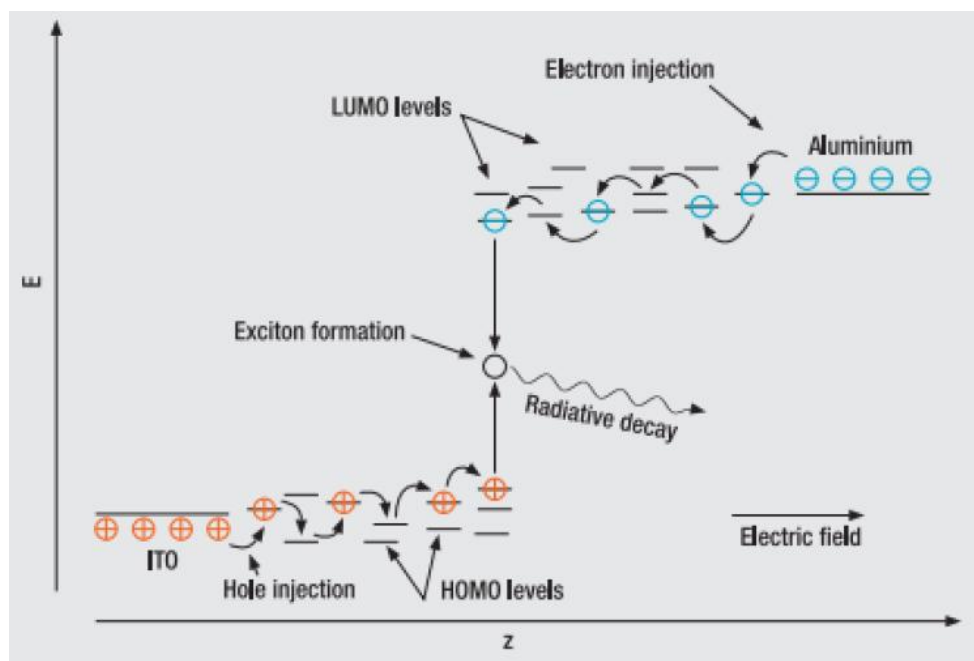
transparent anode, which is usually glass. The most basic polymer OLEDs includes a single organic layer. However, multilayer OLEDs can be fabricated, and so the device efficiency can be improved.

During the operation, a voltage is applied across the OLED such that the anode is positive with respect to the cathode. A current of electrons flows through the device from cathode to anode. As electrons are injected into the emissive layer from the cathode, holes are injected into the conductive layer from anode. Electrostatic forces bring the electrons and holes toward each other and they recombine as shown in Figure 2. The frequency of the radiation of the emission depends on the band gap of the material, in this case the different in energy between the Highest Occupied Molecular Orbital (HOMO) and the Lowest Unoccupied Molecular Orbital (LUMO) [22] and the process is show in Figure 3.





**Figure 2: Basic OLED operation when bias is applied to the cathode and anode. Step 1 shows how the current flows from the cathode to the anode through the organic layers. Step 2 shows electrodes from the conductive layer leaves holes that need to be filled with the electrons in the emissive layer. Step 3 shows the recombination process and finally the light photon emission**



**Figure 3: Electrodes are injected from cathode made of Aluminium material to LUMO levels and holes are injected from anode made of Indium Tin Oxide to HOMO levels**

Indium tin oxide (ITO) is commonly used as the anode material. It is transparent to visible light and has a high work function which promotes injection of holes into HOMO level of the organic layer. Successful application of organic luminescence in light-emitting devices required materials and device structures that overcame the intrinsically high resistivity of the organic materials while achieving balanced charge injection from electrodes into organics [2].

Currently available OLED products are nearly all displays. Given the higher value and price offered for displays, they have been the main focus of OLED development, in their history. OLED-based lighting, on the other hand, has yet to overcome its unique set

of challenges. For lighting applications, products must simultaneously achieve lifetime, color quality, uniformity, brightness, and efficiency acceptable to a consumer [1][2].

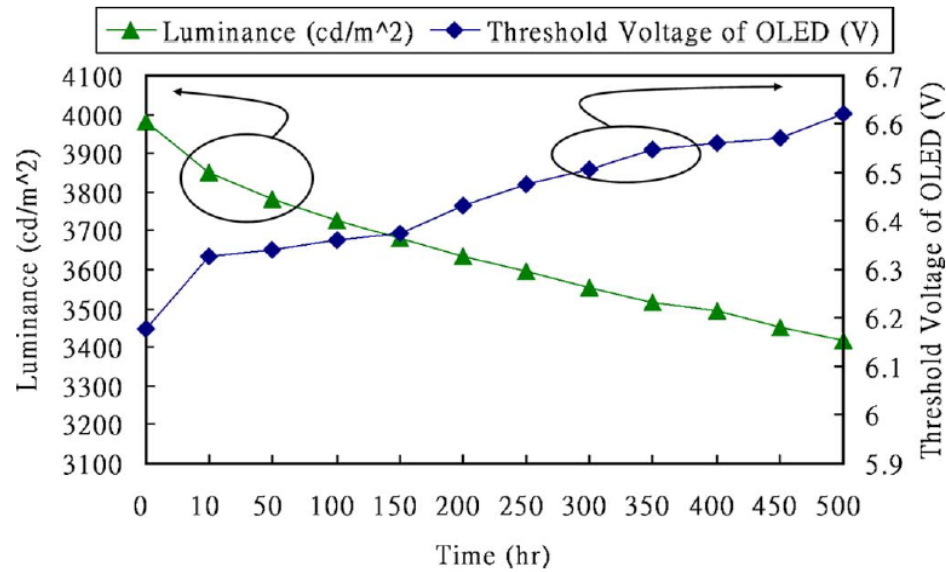
## **1.2 Organic Light Emitting Diode (OLED) displays in comparison to Liquid Crystal displays (LCD)**

OLED displays and Liquid Crystal Display (LCD) are always compared side by side [1], where is evident that OLED displays possess several benefit and superior properties than LCD.

LCD displays use a backlight to illuminate their pixels, while OLED's pixels produce their own light. Backlight adds structure and circuitry to the device. In addition, the light produced by the backlight has to pass several layers. Each of the layers of the LCD rejects light. Color filters in LCD reject a great amount of light and thus affecting the intensity of the light. In contrast to LCD, OLED displays are made of fewer layers than LCDs and can be made of flexible structures and components required by flexible devices. LCD has the problem to turn off which is notable in darker environments. OLED can produce a pure black or strong black with no blooming due to the fact that OLED can turn off their pixels completely, and thus improving the contrast ratio of the image.

Viewing angle is a main concern in LCD display. The image viewed with a wide-view angle in LCD has lower quality than the image viewed from the center or small-view angle. On the other hand, the quality of the display is about the same from any

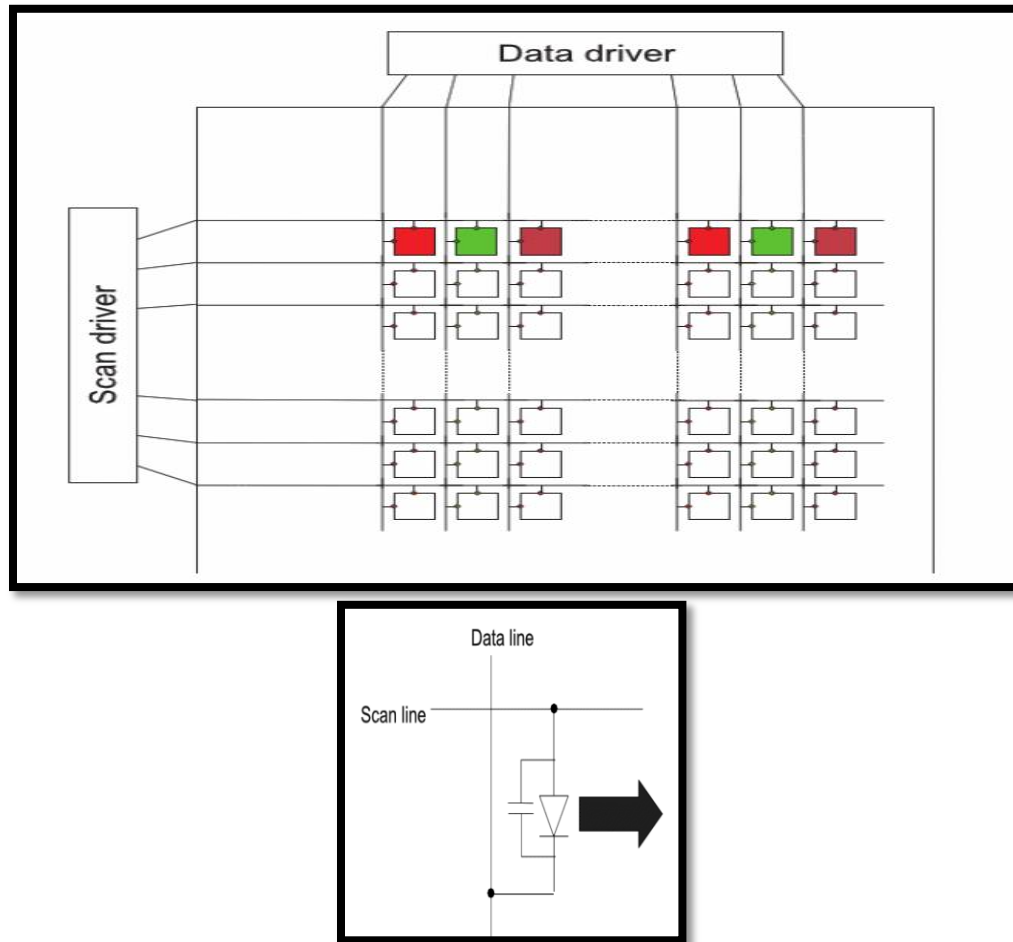
view-angle in OLED displays. However, the major problems in OLED displays are the degradation of OLED over time [23] as shown in Figure 4 and the instability of TFTs.



**Figure 4:** Degradation of OLED over time. The initial threshold voltage of OLED is around 6.1V but it changes to 6.6V after 500 hr

### 1.3 Passive-Matrix OLED and Active-Matrix OLED

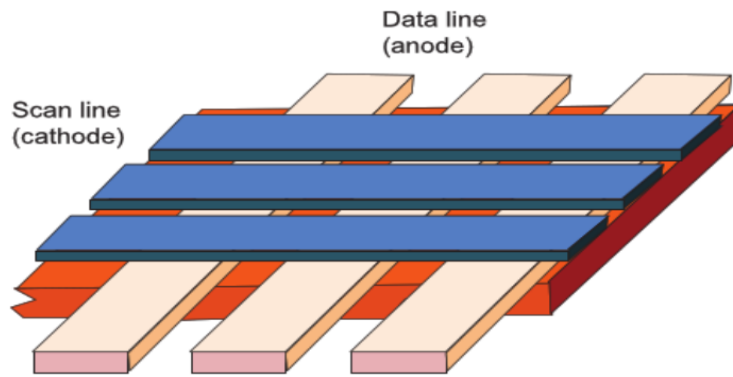
There are several forms of OLED displays such as segment displays, passive matrix displays and active-matrix displays [1]. The most popular are passive matrix OLED (PMOLED) and active matrix OLED (AMOLED). Figure 5 illustrates a PMOLED comprising a data line which is oriented vertically, and a scan line which is oriented horizontally, where OLED devices are fabricated between lines as depicted in pixel circuit schematic in Figure 5.



**Figure 5: Matrix driving of a passive-type OLED display including pixels, data driver and scan driver. Each pixel circuit schematic includes an OLED element intersected by data line and scan line**

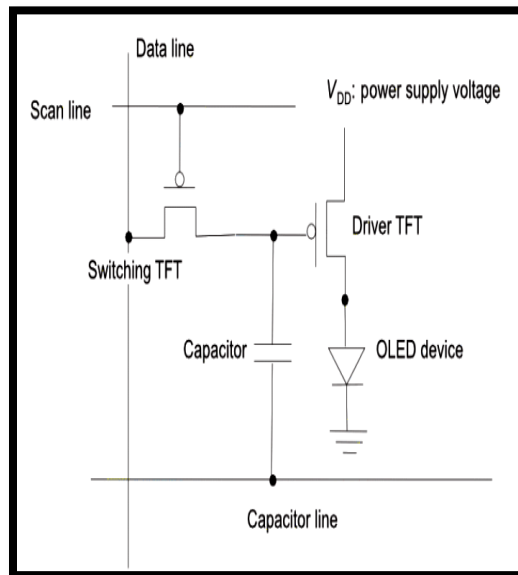
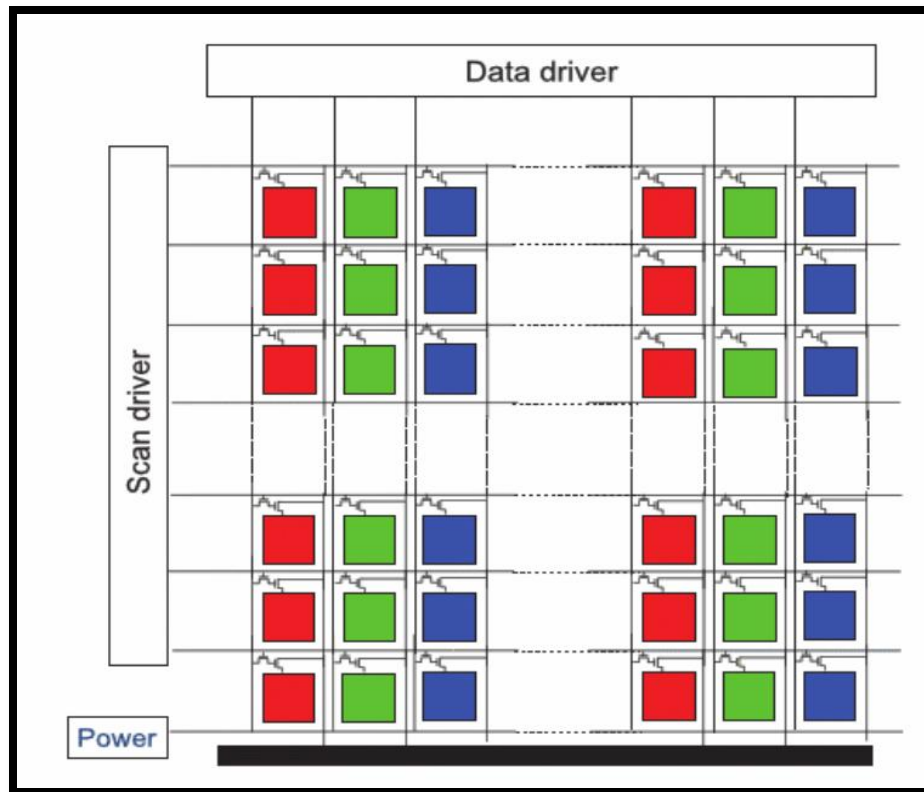
The data lines (anode) and the scan lines (cathode) are arranged perpendicular, where each interception of data lines and scan lines make a pixel as depicted in Figure 6. In addition, Figure 5 illustrates data driver and scan driver for driving data line and scan line respectively. PMOLED does not include active elements in the matrix as also illustrated above. Usually, PMOLED displays have been used more for lower-resolution

displays than high resolution displays because of high brightness needed for high resolution and required due to short emission time, which diminishes lifetime, insufficient charging period for high-resolution display, due to the time loss caused by the charging of the huge parasitic capacitance of passive-matrix OLED displays, and insufficient data line capacitance discharging in a short time, which makes inaccurate low grayscale presentation [1].



**Figure 6: Structure of a passive-matrix OLED display including scan lines and data lines. Each interception of the scan lines with the data lines makes a pixel**

AMOLED comprises pixels arranged in array and belongs to active display type since it includes active elements as depicted in Figure 7. AMOLED has high lighting efficiency and is generally utilized for the large scale display devices of high resolution. AMOLED's pixel comprises a driver transistor (Driver TFT), which is a current driving element. When the electrical current flows through the OLED, the OLED emits light, and the brightness is determined according to the current flowing through the OLED itself.

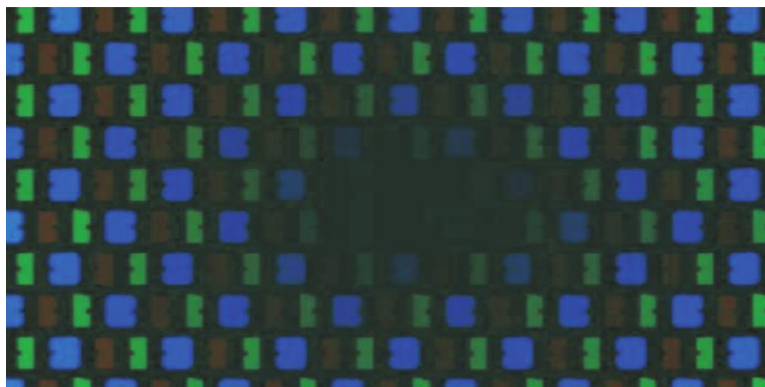


**Figure 7: Active-Matrix OLED display and circuit diagram of two-transistor one-capacitor (2T1C) pixel driving circuit**

## 1.4 MURA Effect

AMOLED pixel driving circuit needs to accomplish the task of converting the voltage signals into the current signals. Thus, a small current variation can be distinguished as non-uniformity or MURA effect [1]. A simple driving method using a 2T1C (two transistors and one capacitor) circuit as depicted in Figure 7, tends to cause yield loss due to MURA [1].

Figure 8 shows an extreme-case example of luminance MURA. The human eye is very sensitive to changes in luminance, so if there is driver TFT current non-uniformity in the display area, it is perceived as MURA. In particular, low-temperature polycrystalline-silicon-thin-film transistor (LTPS TFT) which is treated by excimer laser annealing has a serious MURA issue [1]. Consequently, it is now worthy to examine and compare the most predominant driver transistors in the art.

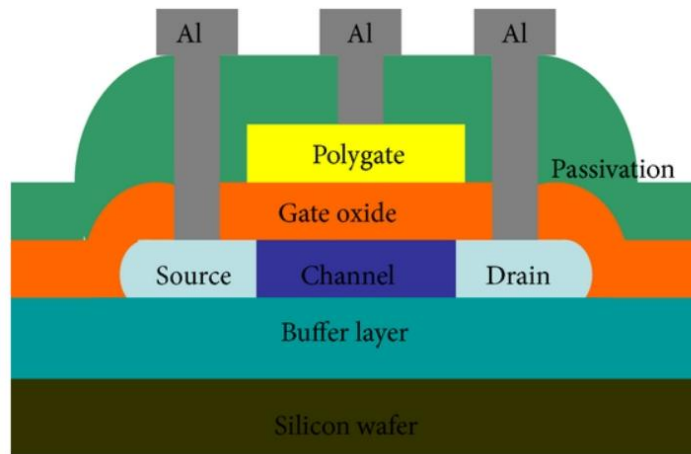


**Figure 8: Image of luminance MURA (non-uniformity) due to variation in threshold voltage in TFTs**



## 1.5 Driving Thin-Film Transistors

The most prevalent thin-film transistors (TFT) are amorphous silicon (a-Si), low-temperature polycrystalline silicon (LTPS) [24] and amorphous indium gallium zinc oxide (a-IGZO). LTPS offers higher mobility than a-Si and a-IGZO and generally lower capacitance compared to a-IGZO depending on device structure [5][6] and depicted in Figure 9.



**Figure 9: Cross-section of Poly-Si TFT fabricated in a silicon wafer**

Low temperature fabrication process (enabling flexible displays) as well as higher stability of threshold voltage shift under positive gate-bias stress has made LTPS-TFTs very attractive for implementing circuits, including image capture, in AMOLED displays [6]. However, it suffers from short range mismatch due to grain boundaries. The fabrication process is more costly especially when it comes to large are scaling due to the more complex processing [6]. Most of the LTPS-TFTs are p-type [5] [7], and so the

power line voltage drop which results in degradation of emission current is an important problem. a-IGZO technology, which belongs to the general category of metal-oxide semiconductor, offers a carrier mobility of at least 15 times higher compared to the silicon-based technology [6]. In general, a-IGZO TFTs have low-cost, and better mobility than a-Si [1] and exhibit better large-area uniformity, scalability with low production cost, and a lower leakage current [8].

In the design of an AMOLED, a main problem to be solved is non-uniformity of luminance among respective pixels of AMOLED. In the current technology, due to limitations of the crystallization process, LTPS TFTs produced on a large-area glass substrate often have non-uniformity on electrical parameters such as threshold voltage, mobility and the like, and such non-uniformity may cause current difference and luminance difference among OLED devices, that is, a MURA-phenomena occurs, which may be perceived by human eyes [9]. In addition, a threshold voltage may drift under a high temperature or supplied with a voltage for a long time in a-Si and a-IGZO resulting in poor image quality [1] [9]. Due to different images as displayed, drifts of threshold voltages of TFTs in respective areas on a panel may be different from each other, which may cause display luminance difference, such display luminance difference often renders in turn an image sticking phenomenon since such display luminance difference has a relation to a previously displayed image [9]. Furthermore, non-uniformity of the electrical characteristics of the OLED devices may also be resulted from non-uniform thickness of the mask during an evaporation process. For the a-Si process constructing

pixel units by adopting N-type TFTs, a storage capacitor therein is connected between a gate of a driving TFT and an anode of the light-emitting device, if voltages at the anodes of the OLED devices of respective pixels are different when a data voltage is transmitted to the gates, the gate-source voltages  $V_{gs}$  actually applied to the TFTs may be different, so that display luminance are different due to different driving currents [9].

Another similar problem to threshold-TFT variation that designers should consider is OLED degradation. Voltage across the OLED device usually increases with time as the OLED becomes degraded [9]. In conclusion, the threshold voltage shift of the TFT and degradation of OLED has direct impact on circuit performance, results in poor image quality and thus compensation is needed.

## **CHAPTER 2 DRIVING METHODS**

Because the threshold voltage of the drive transistor will drift along with time to cause the unstable irradiance of the organic light emitting diode would affect the display effect and because the deterioration of OLED would also affect the display effect.

AMOLED pixel driving circuits and methods need to be equipped with function of compensating the threshold voltage of the driver thin-film transistor and compensating for a change in efficiency due to degradation of an organic light emitting diode [11][12][17].

At this time, there are various kinds of driving methods with compensation for AMOLED pixels such as external compensation method [13], luminance adjusting algorithm method [15], current programming [16] and voltage programming method [1][3] [14][18].

### **2.1 External Compensation method and Adjusting algorithm method**

The external compensation and luminance adjusting algorithm methods can sense, store and compensate for performance variation and/or degradation of driving TFT and OLED [13]. The external compensation improves aperture ratio as well as panel yield due to additional TFTs and capacitors. As noted in Figure 10, the pixel area includes few

transistors T1, T2 and T3. However, the external compensation and luminance adjusting algorithm methods use many additional logic blocks and memories which increase the system cost [3] [19][20].

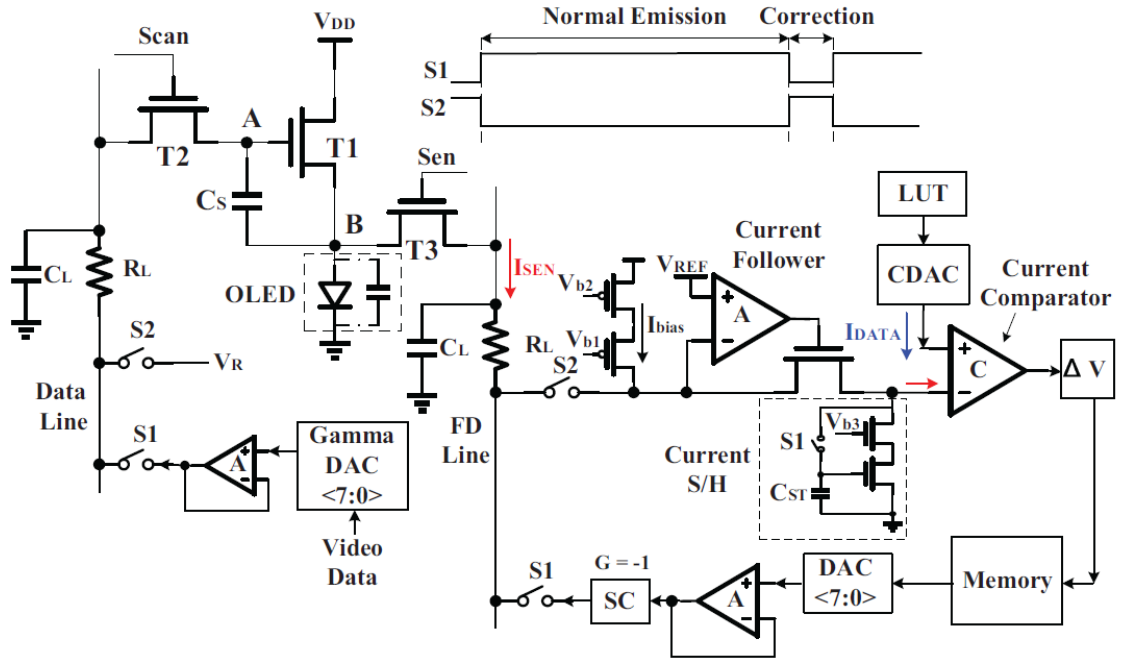


Figure 10: Circuit implement block diagram of a peripheral compensation system, where the aging degradation is calibrated by current sensing while the mobility variation of TFTs can be detected

## 2.2 Current programming algorithm method

The current programming method enables an accurate compensation for performance variations Figure 11 [16], but suffers from a long settling time especially at low level gray [3]. The current scaling method using mirroring TFTs can overcome the

long settling time problem in low level gray, but the mismatch of electronic characteristics of mirroring TFTs cause emission current error [3].

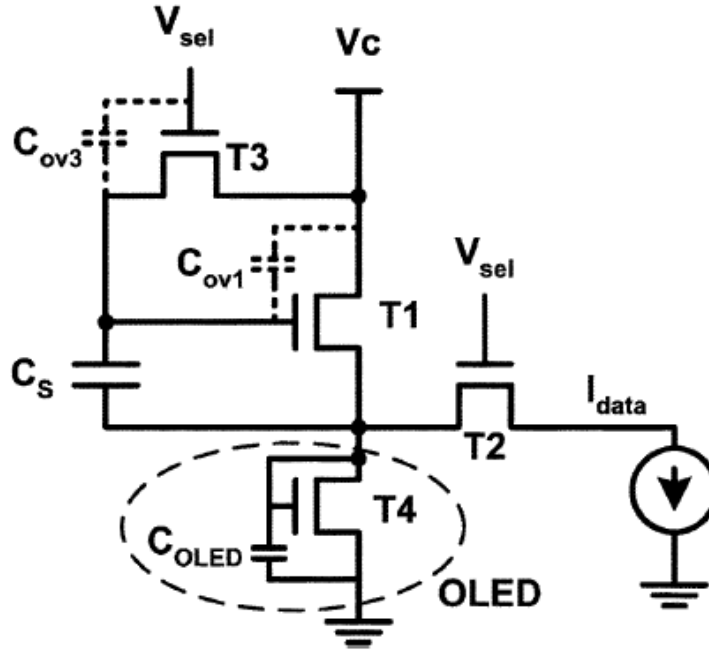


Figure 11: Circuit schematic of a current programming method having 3-TFTs, a storage capacitor and an OLED in each pixel

## 2.3 Voltage programming algorithm methods

The voltage programming method usually allows a fast programming speed but usually cannot ensure an accurate compensation in conventional circuits. Wang et al. shows in Figure 12, a-IGZO pixel circuit adopting 3T1C configuration for use in 3-D AMOLED display. The driving method includes four stages: A) reset stage, B)

compensation stage, C) data input stage and D) emission stage, where the compensation stage is set to 100us [11].

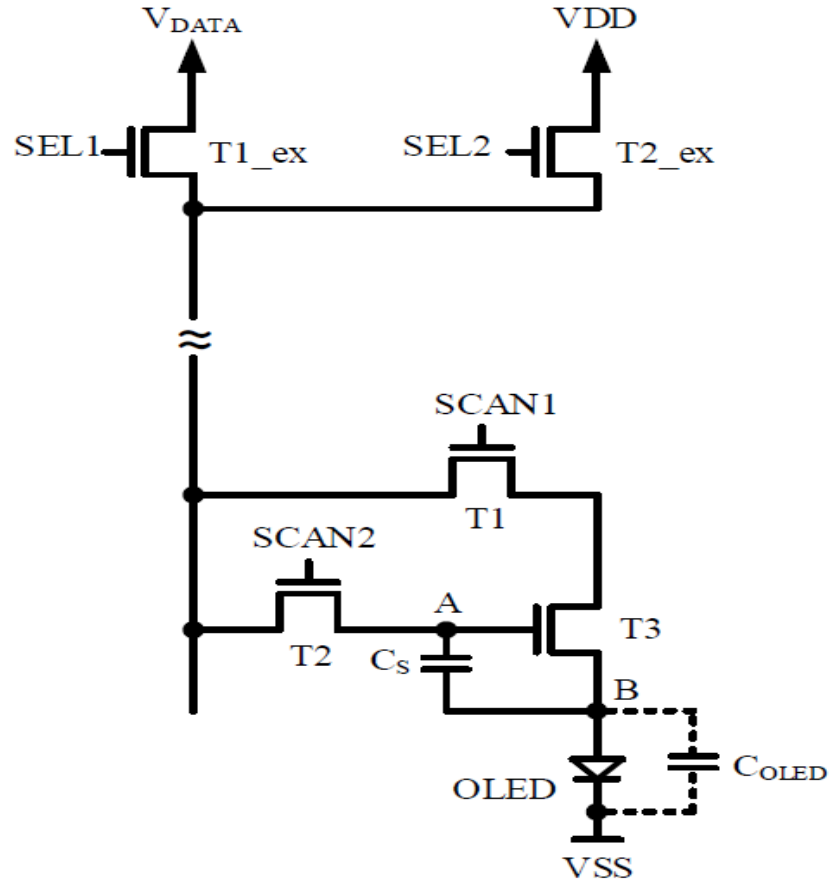
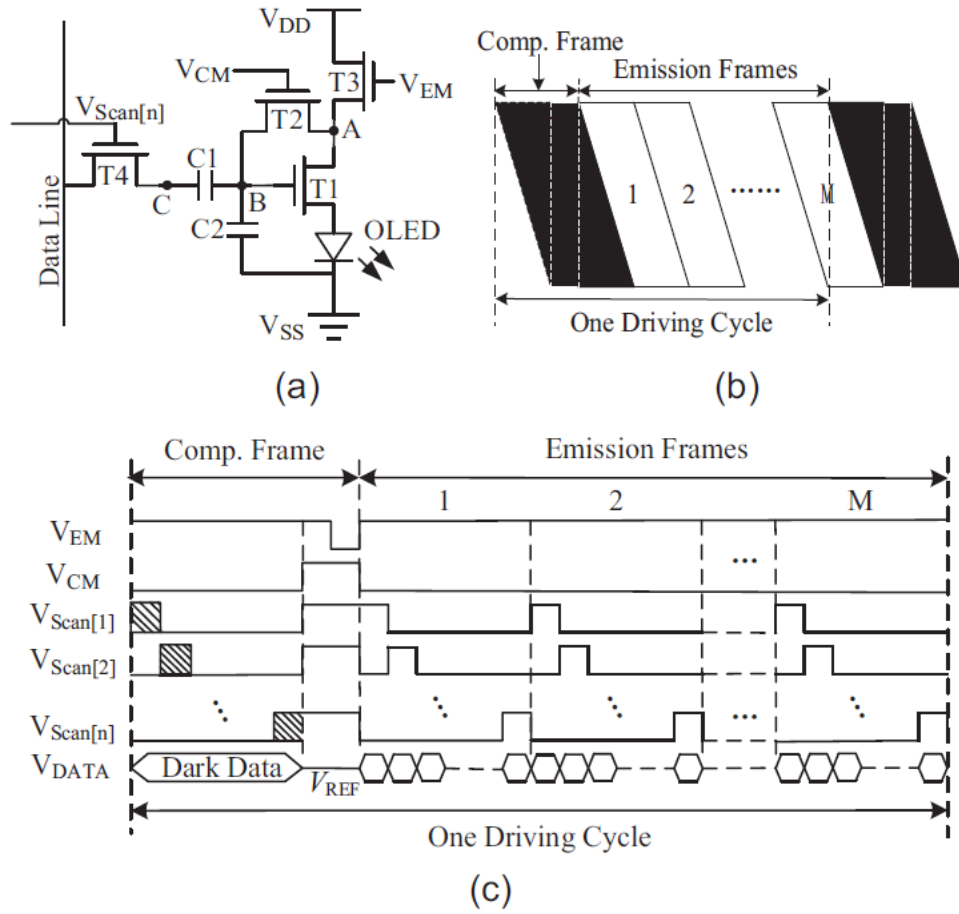


Figure 12: Schematic of conventional pixel circuit including 3 transistors and 1 capacitor in the pixel area using a voltage programming method, where the compensation is set to 100 us.

Meng et al. shows in Figure 13, a current source free separate frame compensated voltage-programmed active organic light emitting diode pixel circuit having four transistors and two capacitors (4T2C schematic) wherein transistors are a-IGZO TFTs.

The driving cycle is divided into two periods wherein a single separate frame for compensation and the other lasts  $M$  frames for emission, where the compensation for all the pixels is carried out simultaneously. However, the circuit has a separate frame for compensation and the emission frames depends on the charge holding at node B in the compensation frame [3].



**Figure 13: (a) Schematic of conventional voltage programming pixel (b) one driving cycle and (c) timing diagram of one driving cycle**



Wang et al. shows in Figure 14 an AMOLED pixel circuit with OLED biased in AC mode comprising a-IGZO TFTs. The circuit includes a 4T1C schematic having a current source line which offers a pulse bias current. However, the compensation time takes milliseconds.

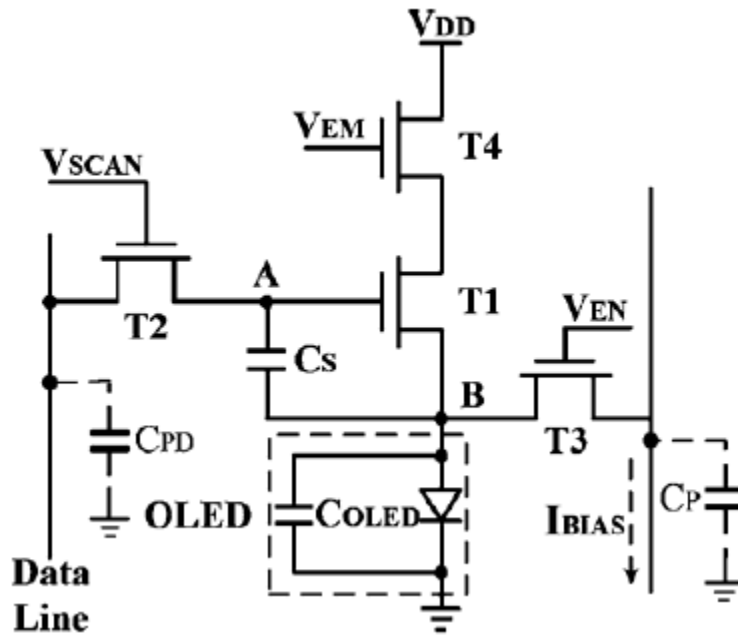


Figure 14: Schematic of conventional pixel circuit having a 4T1C schematic using a-IGZO TFTs, and a current-biased voltage-programmed AMOLED methodology

## CHAPTER 3 COMPENSATION

### 3.1 Compensation Design

As noted in Chapter 2 Driving Methods, the available driving methods for compensation needs further work in order to maximize the OLED display potential. The luminance non-uniformity due to performance variation and/or degradation of driving TFT and OLED have been challenge to obtaining high quality display. Subsequently, a vast number of circuits have been proposed in order to overcome these issues. The main goals in the compensation design are:

- 1) Simple structure, especially in the pixel area. Simple structure reduces the cost of the device either in the pixel area or drivers (external area). In the pixel area, few transistors provide better aperture ratio (better resolution) and brightness uniformity of display, and thus a better image quality.
- 2) Accurate compensation of threshold variation of the driving TFT and/or minimize the error due to the variation. In order to compensate for the threshold variation of the driving TFT, the current should be ideally independent to  $V_{th}$  (threshold of the transistor).

- 3) Accurate compensation of OLED degradation and/or minimize the error due to degradation. The OLED degradation should not affect the luminance of the pixel.
- 4) Proper bias OLED during the compensation period or during non-emission periods. OLED should turn-off during the compensation period and keep OLED negatively biases for a long period in order to suppress OLED degradation.
- 5) High speed requirement (and thus fast programming) is usually a main requirement for today's technology.
- 6) Long compensation period is required in order to achieve low error or ideally perfect compensation. However, speed will be a common trade-off for long programming periods
- 7) As other circuits, power consumption is always a concern.

Numerous approaches have been experimented by researches with the motivation to overcome and/or achieve the goals listed above. In addition, Figure 15 illustrates the trade-off among current error, extraction time for different variations of  $V_{th}$  of TFT [3]. For example, if the extraction time is longer (around 150us) then the error is almost zero.

However, a long compensation period should affect the speed of the circuit. For example, in the ultra-high definition displays, if the frame is 240 Hz, the available extraction time is about 2 $\mu$ s. This would lead to a large current error of 25% [3].

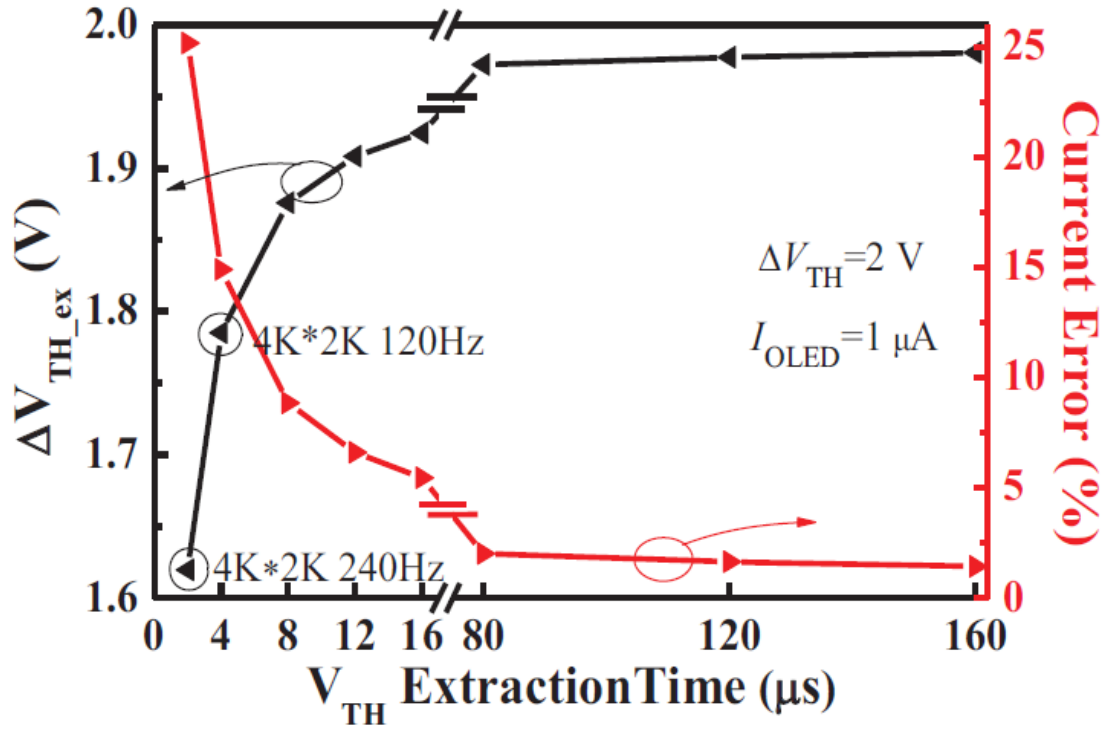
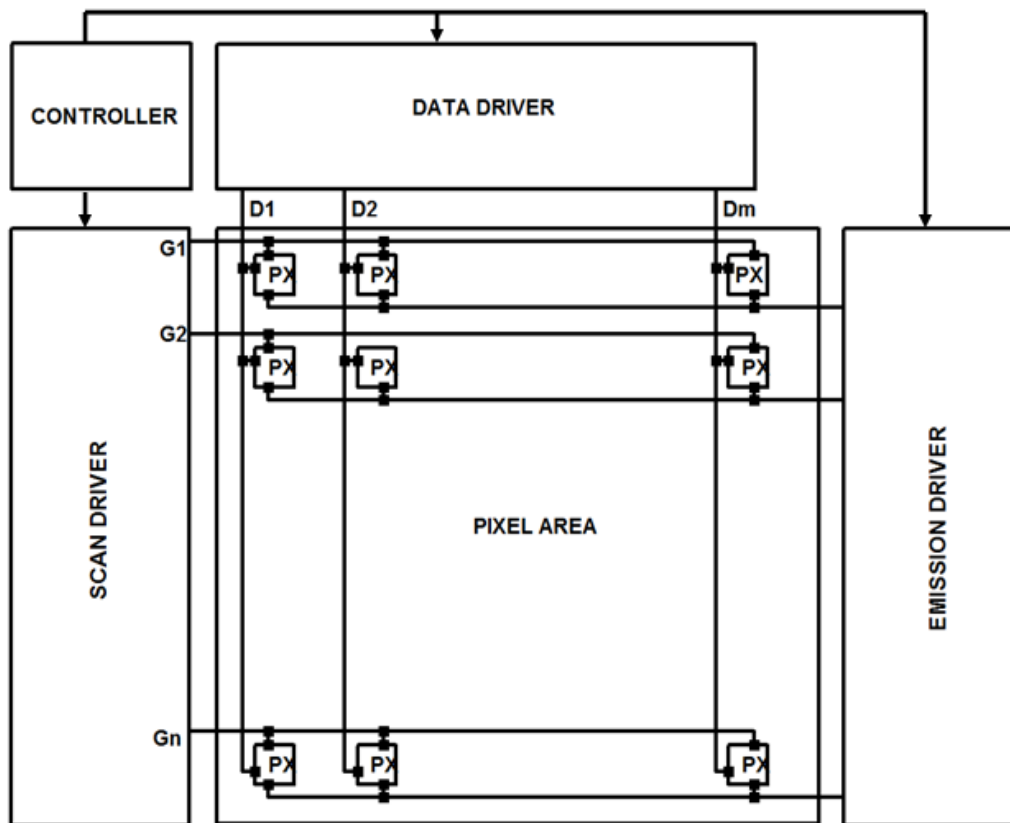


Figure 15: The extracted  $\Delta V_{th}$  values and current error values as a function of  $V_{th}$  extraction time, where a low current error requires a compensation period over 80 $\mu$ s

### 3.2 2T1C TFT-threshold Compensation

Figure 16 illustrates a controller, a pixel area including a plurality of pixels (PX), drivers including scan, data and emission driver. The pixels are driven by a plurality of

scan lines (G1-Gn) connected to the scan driver, a plurality of data lines (D1-Dn) connected to the data driver and plurality of emission lines (Em1-Emx) connected to the emission driver. The PXs are arranged in a matrix pattern and each of them includes transistors and an OLED and thus the display is considered an AMOLED display. Furthermore, Figure 16 illustrates that data, emission, and scan driver are physically separated from each other. However, the emission driver, data driver and scan driver can be integrated.



**Figure 16: Block diagram of an Active-Matrix Light Emitting Diode, pixel area includes a plurality of pixels PX driven by data driver, scan driver and emission driver controlled by a controller**

Figure 17 illustrates a display including a detail layout for only two pixels (PX1 and PX2). However, the display may include any number of PXs. Figure 18 illustrates the driving scheme for a pixel (PX1) including a 2T1C configuration (two transistors and one capacitor).

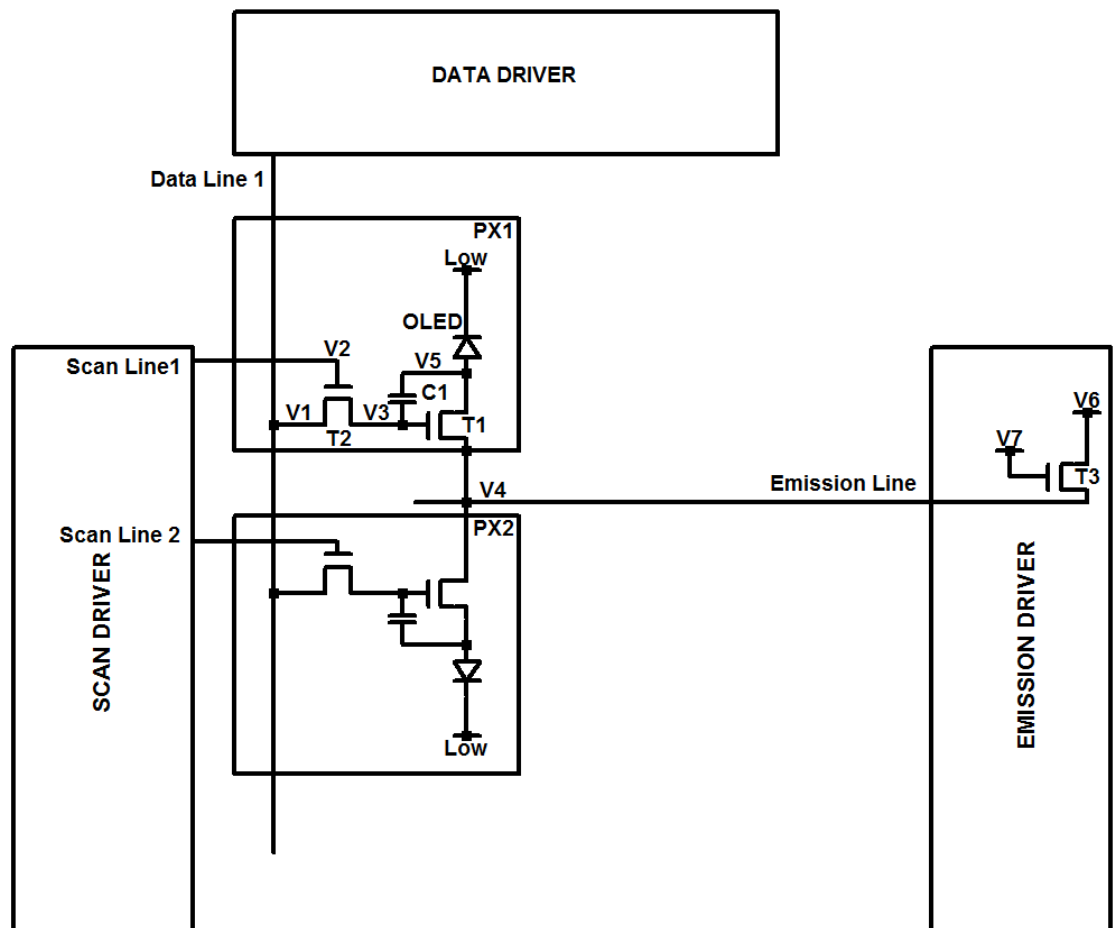
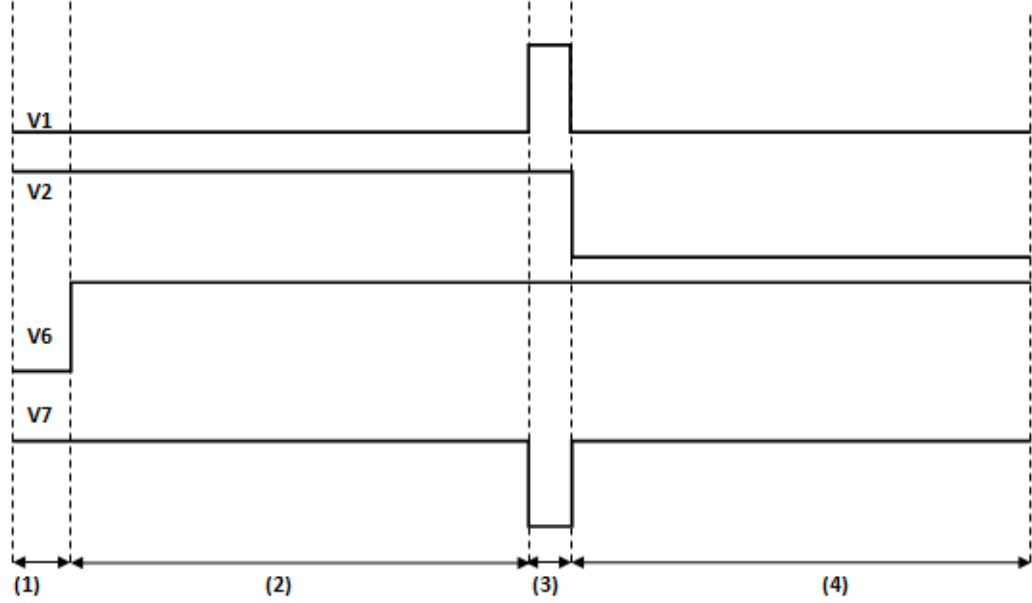


Figure 17: 2T1C pixel schematic, where pixels are driven by scan drivers, emission driver and data driver. Pixel 1 is connected to the drivers through scan line 1, data line 1 and emission line



**Figure 18: Driving Scheme for the 2T1C configuration including (1) initialization, (2) compensation, (3) data programming and (4) emission periods**

The proposed 2T1C pixel circuit operation would be described in conjunction with Figure 17 and Figure 18. T2 is a switching TFT and T1 is the driving TFT, C1 modulates data voltage and the threshold voltage of T1. V1 is the voltage of the first data line and V2 is the voltage of the first scan line, low is the common low voltage of the panel. V4 is the voltage of the first emission line. The operation of the proposed circuit is divided into four steps in each frame, which are initialization (1), compensation (2), data programming (3) and emission (4) as depicted above in Figure 18. In addition, the emission driver includes a switching transistor T3 having a control voltage line V7 connected to a supply voltage V6 and to the PX1 via V4 (emission line).

(1) Initialization

In the initialization step, the first scan line (V2) goes high to turn on T2 in PX1 while V7 goes high to turn on T3 in the emission driver. The voltage of node 3 (V3) is fixed at a first reference voltage (Vref1) through the first data line (V1). The voltage of node 5 (V5) is fixed at a second reference voltage (Vref2) through the driver transistor T1 and the first emission line (V4) which is connected to the supply voltage (V6) during this period. The second reference voltage (Vref2) is a negative voltage provided by the supply voltage (V6) as depicted in Figure 19. Thus, the OLED is reversed bias during the initialization period which not only prevents the OLED from light emitting during the programming period to ensure a high contrast ratio displays, but also suppresses the OLED degradation and thus extends the lifetime of the AMOLED. If a negative bias is applied in an AC mode, the charges in the OLED will migrate in the opposite direction during the negative bias, lowering or even eliminating the internal field and thereby restoring the OLED threshold voltage to the initial level [21].



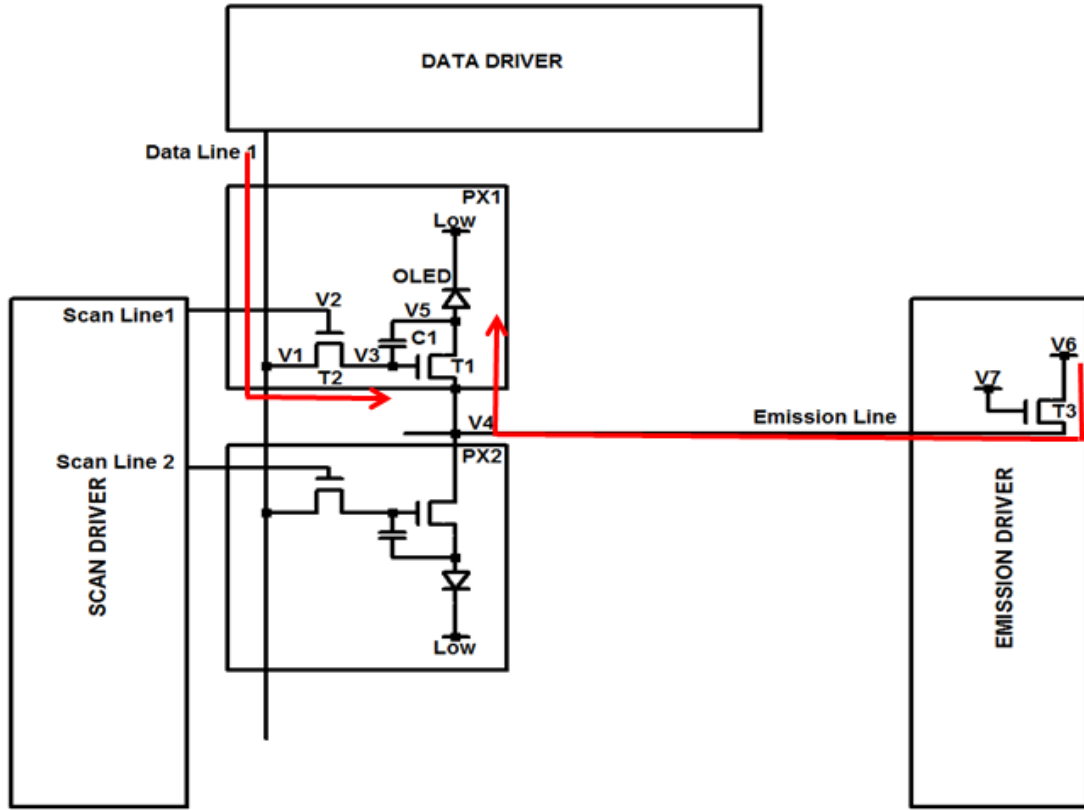


Figure 19: Initialization period (reset operation), where nodes V3 and V5 are reset to predetermined values and V5 is a negative value less than V3

## (2) Compensation

In the compensation step, the first scan line (V2) maintains a high voltage to maintain on T2 in PX1 and V7 maintains a high voltage to maintain on T3 in the emission driver. The voltage of node 3 (V3) is maintained at a first reference signal (Vref1) through the first data line (V1). However, the supply voltage (V6) supplies a high voltage to the first emission line (V4). Thus, the voltage of node 5 (V5) is charged up through the driver transistor T1 until T1 is turned off. In the end of this period, the

voltage of node 5 (V5) reaches a  $-V_{th}$  voltage, where  $-V_{th}$  is the threshold voltage of the driver transistor T1 and operation is shown in Figure 20. Likewise the initialization period, the OLED is reversed bias which not only prevents the OLED from light emitting during the compensation period to ensure a high contrast ratio displays, but also suppresses the OLED degradation and thus extends the lifetime of the AMOLED. Furthermore, the compensation is performed simultaneously for the entire display panel.

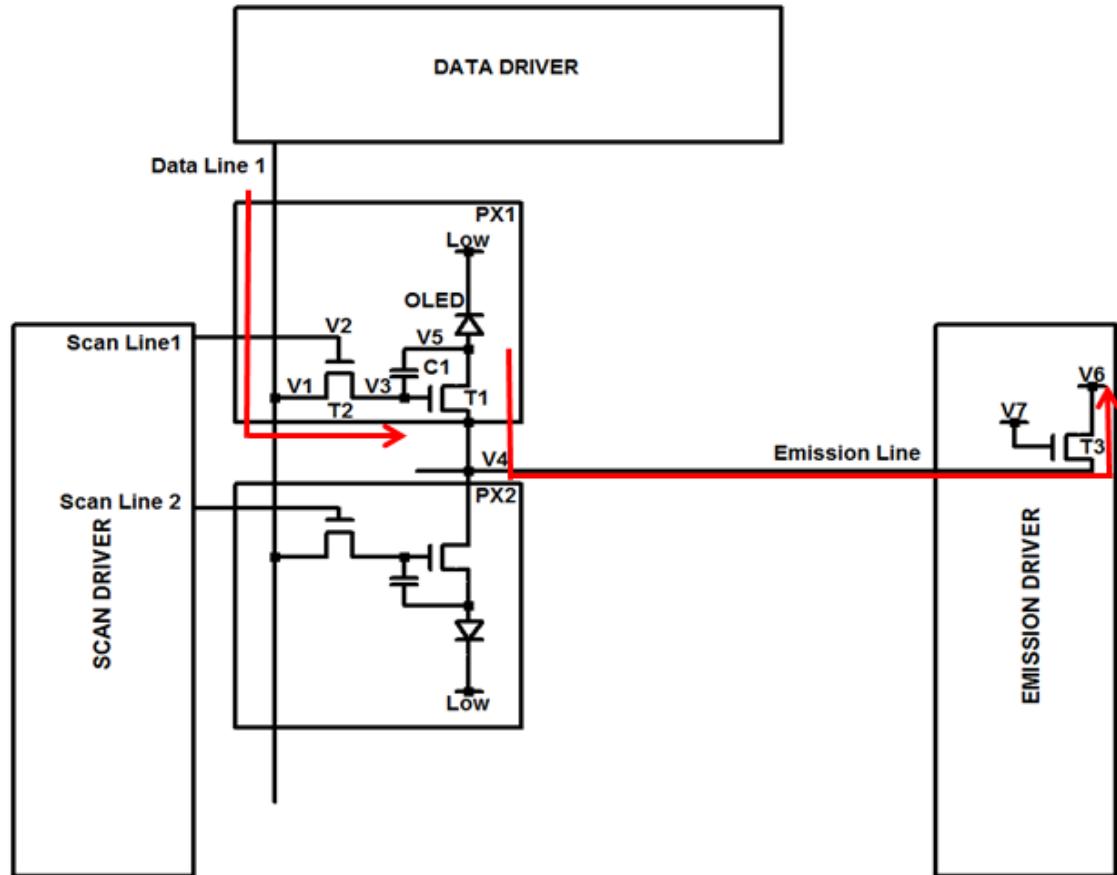


Figure 20: Compensation period, V3 is maintained at a first reference signal and V5 is charged up through T1 and T3 until V5 reaches a  $-V_{th}$  voltage

### (3) Data Programming

During the Data Programming, the first scan line (V2) maintains a high voltage to turn on T2 in PX1. However, V7 goes low to turn off T3 in the emission driver, and thus the first emission line (V4) comprises a high-Z stage. The data voltage (Vdata) is applied to node 3 (V3) through T2 and the first data line (V1) as shown in Figure 21. Based on the charge conservation, node 5 (V5) is modulated as

$$V5 = (Vdata - Vref1) * \frac{C1}{C1 + C_{oled}} - Vth \quad (1)$$

The data programming cycle is performed sequentially for the entire display panel. Furthermore, the voltage of node 5 (V5) should be less than the threshold voltage  $V_t$  of the OLED in order to prevent the OLED from light emitting during the programming period to ensure a high contrast ratio displays.

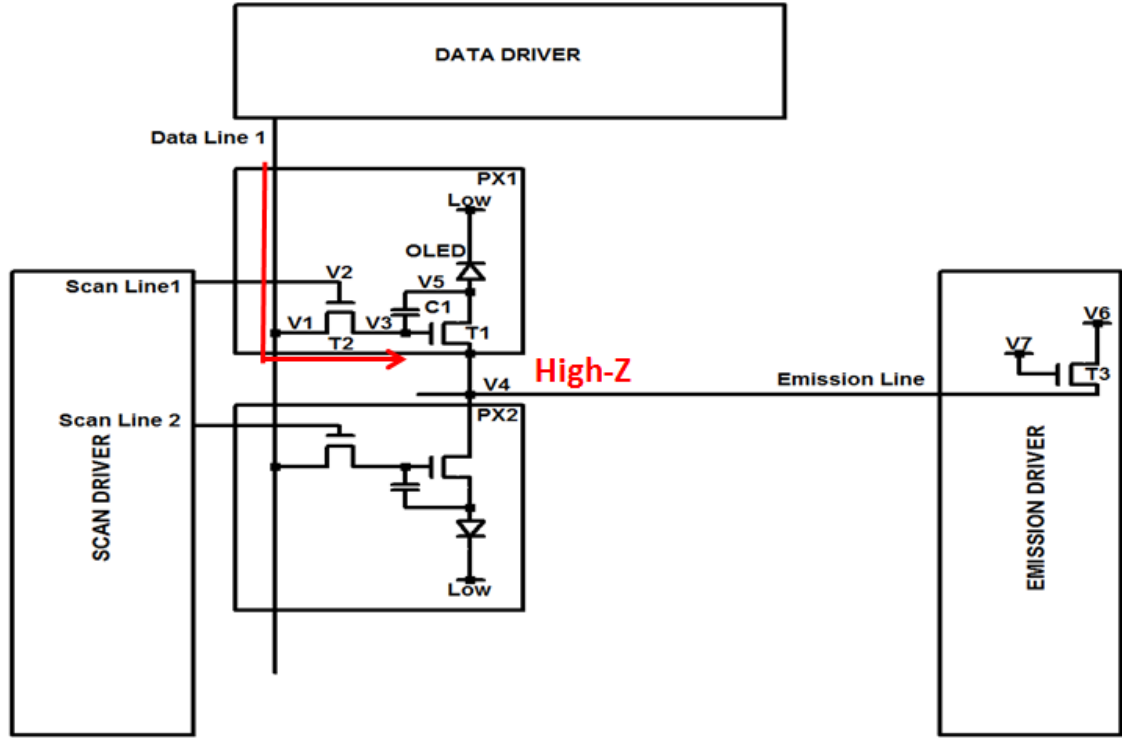


Figure 21: Data voltage is applied to V3, and V5 is modulated accordingly while V4 has a High-Z stage

#### (4) Emission

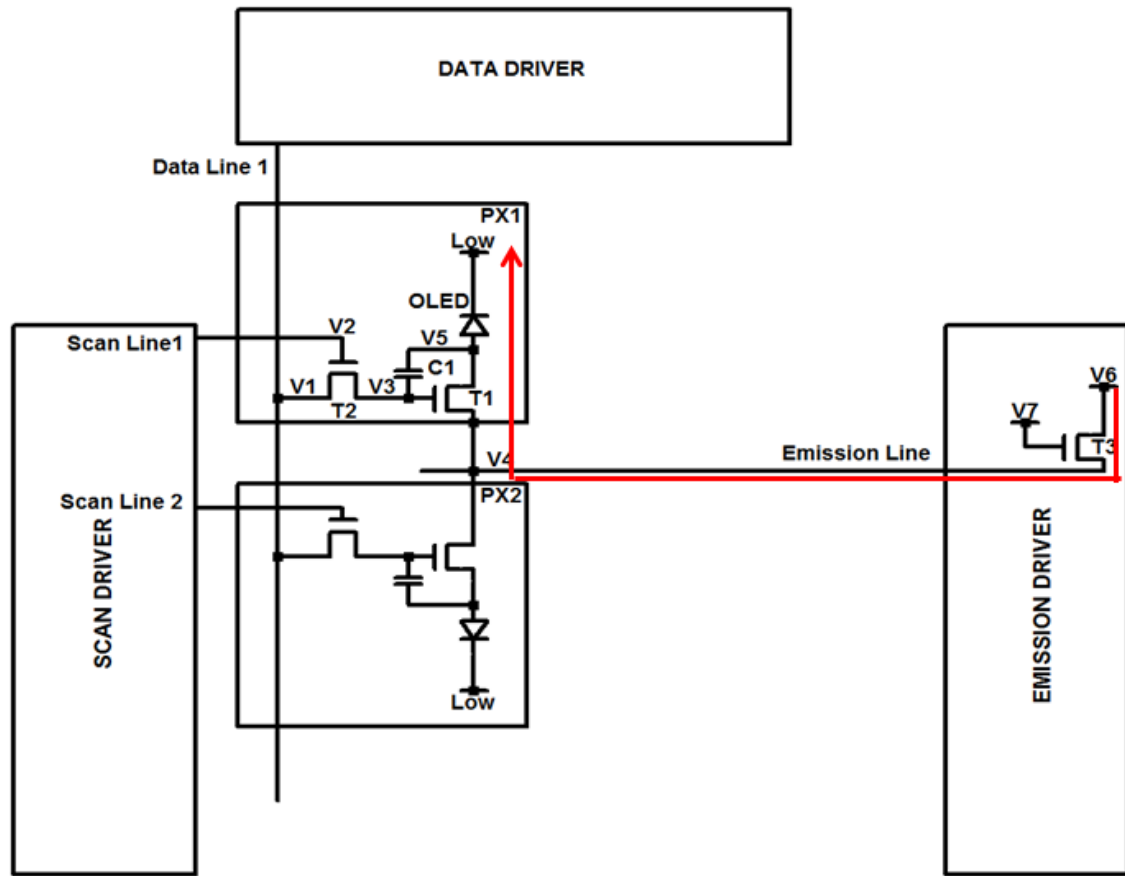
After the data programming period, the first scan line (V2) goes to low to turn off T2 in PX1. Moreover, V7 changes to high to turn on T3 in the emission driver, and thus a high voltage V6 is supplied to the first emission line V4 as shown in Figure 22. The gate-source voltage of driver transistor T1 at the end of (3) period is

$$VGST1 = (Vdata - Vref1) * \frac{C_{oled}}{C1 + C_{oled}} + V_{th} \quad (2)$$

The OLED current could be expressed as

$$\begin{aligned}
I_{OLED} &= \frac{KT_1}{2} (VGST_1 - V_{th})^2 \\
I_{OLED} &= \frac{KT_1}{2} \left( (V_{data} - V_{ref1}) * \frac{C_{oled}}{C_1 + C_{oled}} + V_{th} - V_{th} \right)^2 \\
I_{OLED} &= \frac{KT_1}{2} \left( (V_{data} - V_{ref1}) * \frac{C_{oled}}{C_1 + C_{oled}} \right)^2 \quad (3)
\end{aligned}$$

KT1 is  $\mu_n * C_{ox} * (W/L)$ . Based on the above equation, the emission current is independent of the  $V_{th}$  of T1 and the OLED voltage. Consequently, the proposed circuit compensates the instability of threshold of thin-film transistor (TFT) and degradation of organic-light emitting diode (OLED).



**Figure 22:** High voltage is applied to V4 through the emission line, and the current starts flowing through the OLED

To verify the proposed pixel circuit, the circuit simulation is performed using AIM-SPICE software and the model is a Low Temperature Poly-silicon LTPS (level = 16). The circuit parameters are listed in Table 1. The OLED is modeled by a diode-connected TFT in parallel with a capacitor.

**Table 1: Simulation Parameters of the proposed 2T1C schematic including sizing of the transistors and voltage supplied by the data line, scan line and emission line**

W/L (T1)	8 $\mu$ /5 $\mu$
W/L (T2)	5 $\mu$ /5 $\mu$
W/L (T3)	50 $\mu$ /5 $\mu$
C1	0.3pf
V6 (supply voltage)	-3 to 10v
Low (common voltage)	0V
V7 (control voltage)	2v to 15v
V1 (data voltage, first reference voltage)	0v to 3v
V2 (scan voltage)	-1v to 10v

Figure 23 and Figure 24 illustrate transient simulations including waveforms V3 (gate of T1), V5 (source of T1) and Ioled (current of OLED) corresponding to PX1. As appreciated above, the threshold of the driver transistor T1 is stored at the end of the compensation period (2) and so the circuit compensates accurately the instability of the driver TFT. In addition, Figure 23 and Figure 24 illustrate that the OLED is reverse bias during the reset, compensating and programming period and thus improving the degradation of the OLED.

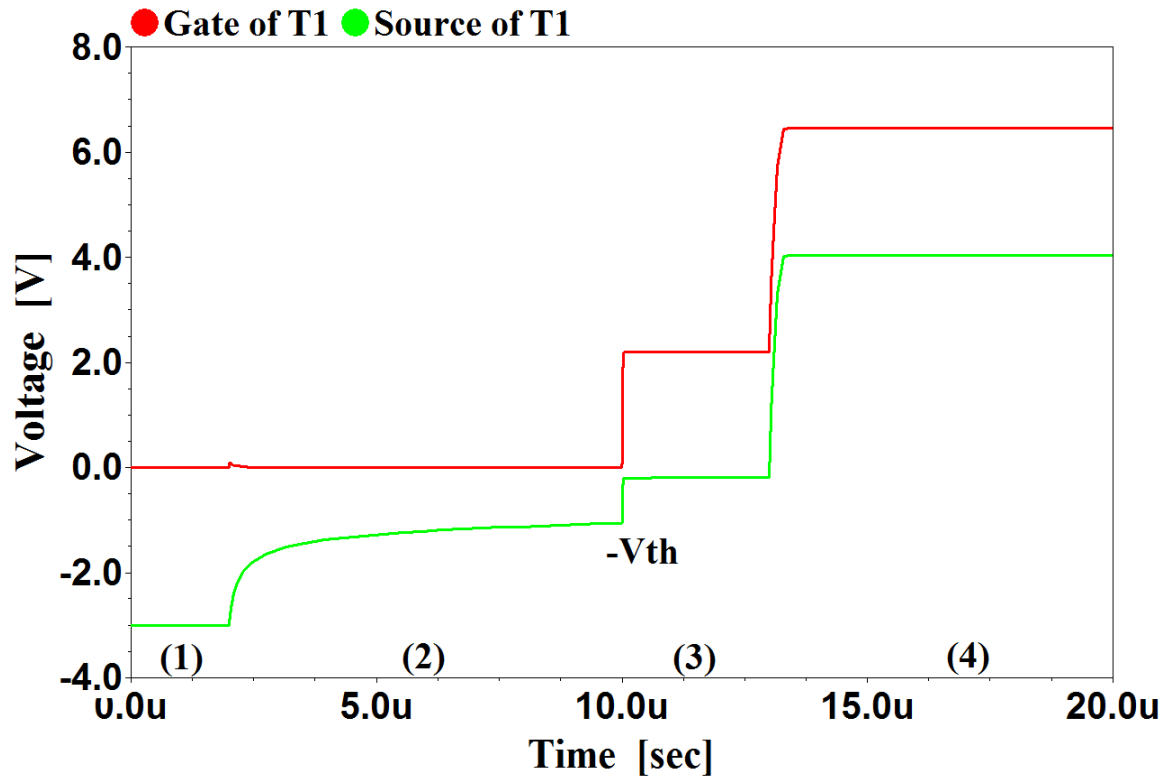


Figure 23: Simulated transient characteristics when data is 2.2V including the initialization period (1), compensation period (2), data programming period (3) and emission period (4).  $-V_{th}$  is stored in node 5 at the end of the compensation period



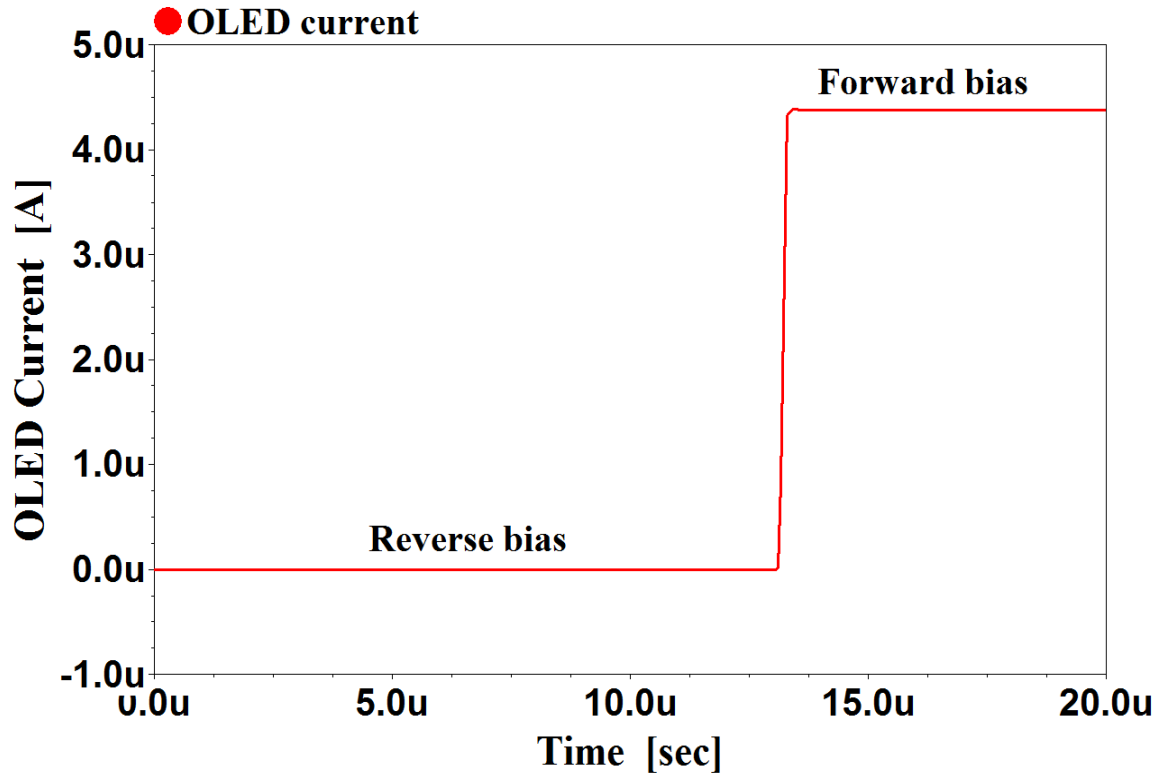
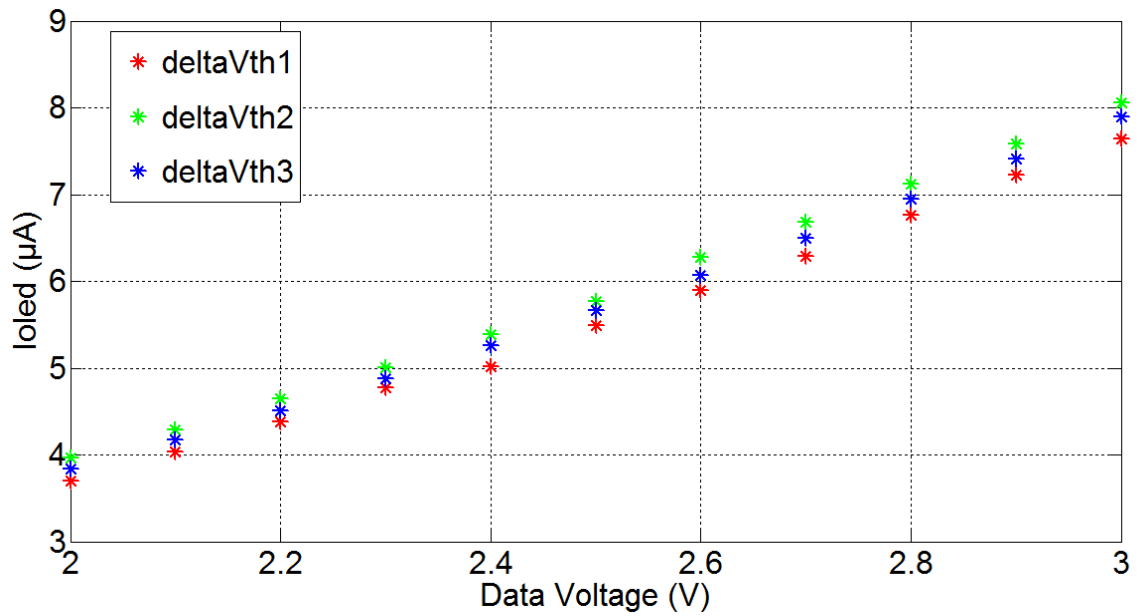


Figure 24: Simulated Ioled characteristics when data is 2.2V showing that the OLED is reversed bias during non-emission periods and forward bias during emission period

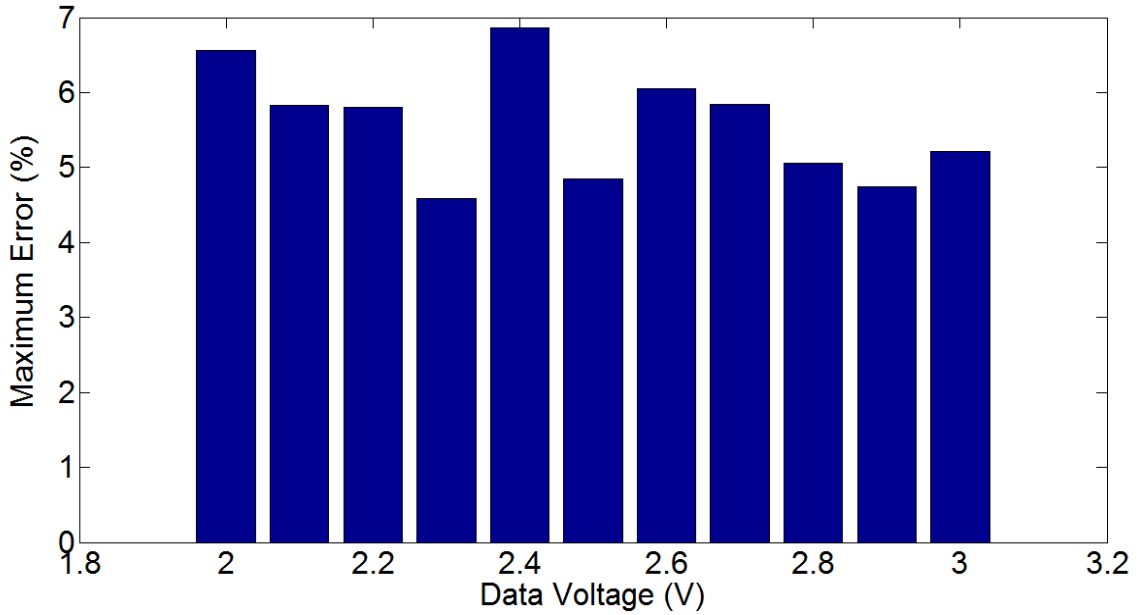
Figure 25 illustrates the simulated voltage data versus current for different variations of  $V_{th}$ , where  $\Delta V_{th1}$  includes a variation of -0.5V of the threshold voltage,  $\Delta V_{th2}$  includes a variation of 0V of the threshold voltage and  $\Delta V_{th3}$  includes a variation of 0.5V. Figure 26 illustrates the maximum error percentage per each data voltage calculated as

$$Error = 100 * \left(1 - \left(\frac{I_{min}}{I_{max}}\right)\right) \quad (4)$$

$I_{min}$  is the minimum OLED current corresponding to a fixed data voltage and variable  $\Delta V_{th}$ .  $I_{max}$  is the maximum OLED current corresponding to a fixed data voltage and variable  $\Delta V_{th}$ . As depicted in Figure 26, the maximum error percentage is below to 7% for each data voltage.



**Figure 25: Simulated compensation results of the proposed circuit with  $I_{oled}$  versus  $V_{data}$  for different variation of  $V_{th}$ ,  $\Delta V_{th1}$  corresponds to a variation of -0.5V of the threshold voltage,  $\Delta V_{th2}$  corresponds to a variation of 0V of the threshold voltage and  $\Delta V_{th3}$  corresponds to a variation of 0.5V of the threshold voltage**



**Figure 26: Data Voltage versus Maximum Error (%) of the circuit, the Maximum Error is the error for the maximum variation of current for each data voltage.**

Therefore, it is demonstrated that an accurate compensation for threshold voltage variation of the driver transistor and degradation of OLED using a simple 2T1C circuit schematic having an error less than 7% have been achieved. In addition, the initialization period and compensation operation take about  $13\mu\text{s}$ , and thus improving the speed of the circuit. Furthermore, it is worthy to mention that the error of conventional 2T1C reaches up 90% and the compensating period of conventional pixel layouts are over  $50\mu\text{s}$ .

### **3.3 Simultaneous compensation and data programming periods**

The goals achieved by using simultaneous compensation and data programming periods driving methodology:

- Possible extension of the length of compensation period in order to improve accuracy without affecting the display's speed operation. In fact, display's speed operation can be increased since compensation and data programming are performed concurrently
- Allow operation at 240Hz for HD and UHD
- Realizable simultaneous emission (SE) method utilized in 2D and/or 3D. Because of longer emission period and low crosstalk requirements in 3D displays, SE has higher super image quality than progressive emission PE for the time division methods. Thus, potential applications of the simultaneous compensation and data programming periods are 2D/3D displays with a high operation of 240 Hz.

### **3.4 Simultaneous Compensation and Data Programming Periods having two sharing transistors**

Figure 27 illustrates an active area of a display panel including the layout for only three neighbors' pixels. The display may include any number of PXs as depicted in Figure 16. Each pixel includes four unshared transistors. The first pixel includes two shared transistors (M7 and M5) as annotated in Figure 27, which are shared with neighbors' pixels. The shared regions are implemented to decrease the number of transistors per pixel and thus improving the resolution of the display. The first pixel includes global voltages lines V4, V8, V12, Low and Emission Line. Figure 28 illustrates the driving scheme for the proposed circuit.

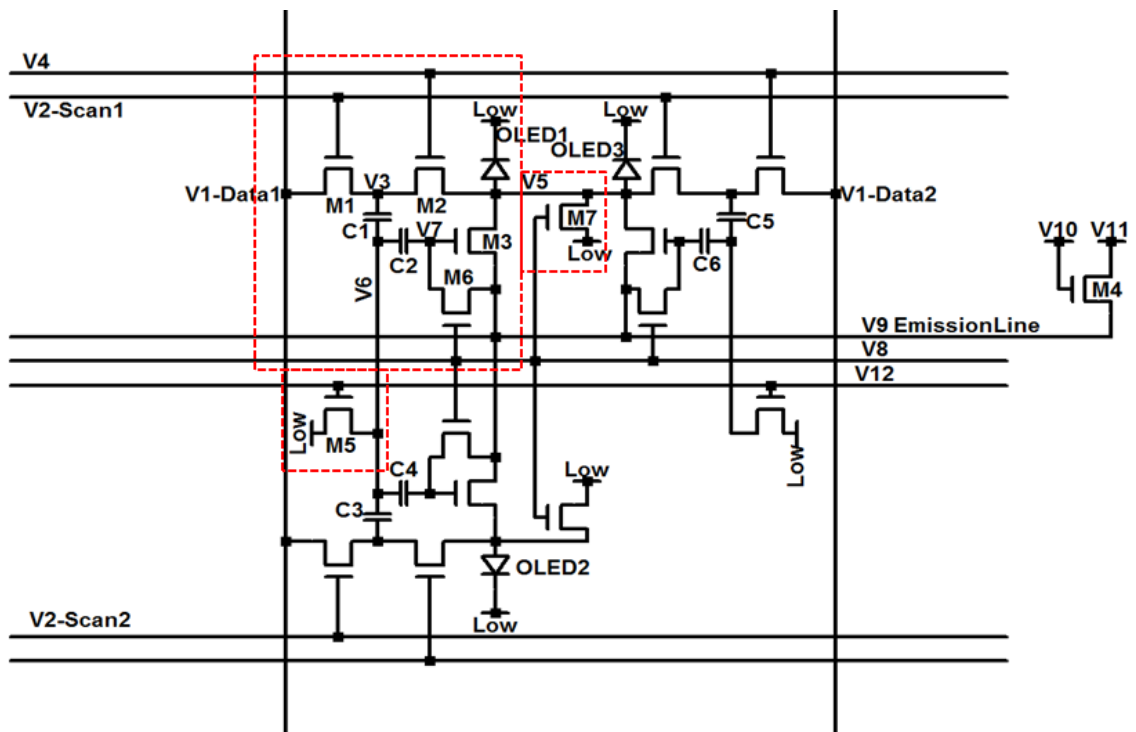
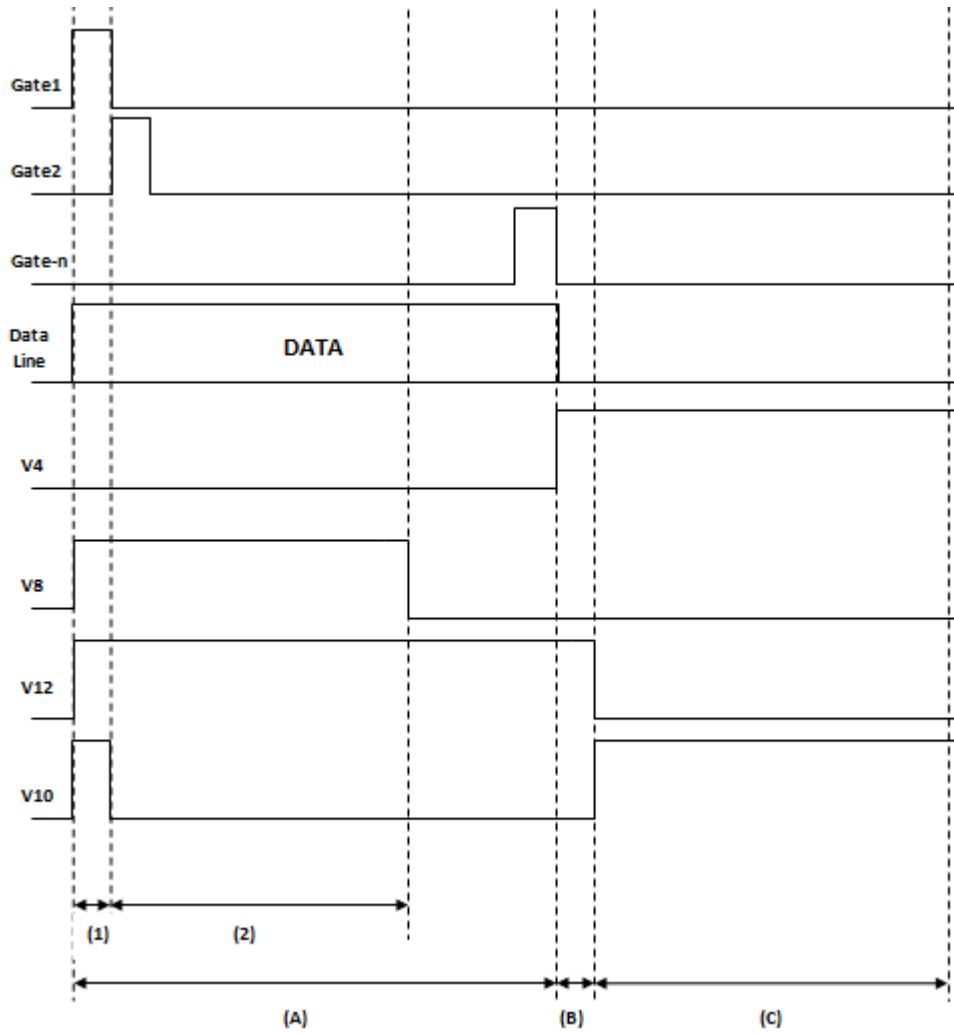


Figure 27: Circuit schematic of a simultaneous compensation and data programming periods having two sharing transistors in order to improve the aperture ratio of the pixel.



**Figure 28: Driving Scheme for the proposed circuit including three periods (A) first part of the data programming, (B) second part of the data programming and (C) emission period, where initialization period (1) and compensation period (2) are performed while (A) is performed**

The proposed circuit operation would be described in conjunction with Figure 27 and Figure 28. M1, M2, M4-M7 are switching TFTs and M3 is the driving TFT, C1 and C2 modulate data voltage and the threshold voltage of M3. V1 is the data line and V2 is the scan line. V10 is the control voltage line of M4 located in the emission driver. V11 is high power supply connected to V9 when M4 is turned-on. The emission driver is located

in the peripheral of the active area of the display. The emission driver can be separated from the data and gate driver as depicted in Figure 16 or integrated. The operation of the proposed circuit is divided in two steps in each frame, where the first step performs the data programming (A-B) and compensation simultaneously (1-2). The second step (C) is the emission period. The data programming is divided in two parts (A) and (B) and the compensation is divided in two parts (1) and (2), where (1) is the initialization stage and (2) is the final compensation stage.

(A) First part of Data programming

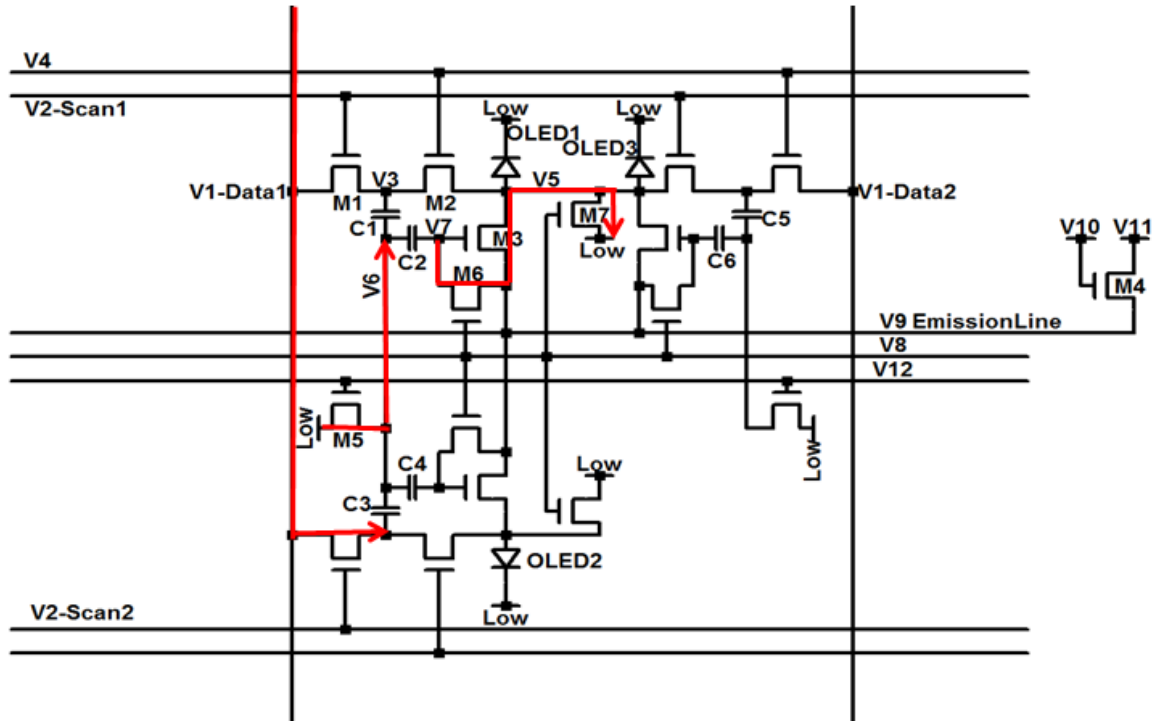
(1) Initialization Step

In the initialization step, the control voltage V10 goes high to turn on M4 in the emission driver. At the same time, global voltages V8 and V12 carries a high voltage to turn on M5, M6 and M7. Thus, a reset signal V11 is supplied to node 9 (V9), and to node 7 (V7) through M6. Nodes 6 (V6), 5 (V5) reset to a low potential via transistors M5 and M7. Simultaneously, the data driver and scan driver begin to write data into node 3 (V3) by turning on the transistor M1 as shown in Figure 29. The data programming is performed sequentially for entire display while the pixels resets and compensates, where the data comprises a negative voltage. Subsequently, the OLED is reversed bias during the initialization period which prevents the OLED from light emitting during this period to ensure a high contrast ratio displays.





remaining display regions. The data writing time is only  $1.9\mu\text{s}$  per row and thus allowing operation at 240Hz for HD (1920x1080) and UHD (4096x2160). The length of the reset period (1) compensation period (2) can be as long as the length of the programming period (A) and can be adjusted in order to maximize the compensation accuracy. Subsequently, this approach would be able to increase the accuracy of the compensation. In addition, the OLED can be reversed bias during the compensation period which prevents the OLED from light emitting during this period to ensure a high contrast ratio displays.



**Figure 30: (A) First part of data programming and (2) compensation step, data programming is performed for remaining pixels sequentially while V7 for all the pixels discharge through the diode connected TFT M3 until V7 reaches Vth**

(B) Second part of Data programming

At the end of the first part of data programming period, all nodes 3 (V3) for the entire display panel carry the corresponding data voltage where the data comprises negative value, and all nodes 7 (V7) for the respective display pixels carry the corresponding threshold voltage  $V_{th}$ . During the second part of data programming period, node 4 goes to high turning on M2 while M1, M6, M7 and M4 are off as shown in Figure 31. Node 12 keeps a high voltage to maintain on M5. At the end of the second part of data programming period, node 5 (V5) is modulate as

$$V5^{final} = \frac{COLED * V5^{init} + C1 * V3^{init}}{C1 + Coled} \quad (5)$$

$V5^{final}$  is the final voltage of V5,  $V5^{init}$  and  $V3^{init}$  are the initial voltages of V3 and V5 respectively. In addition, V5 represents the source of the driver transistor M3 and V7 represents the gate of the driver transistor M3, where V7 holds  $V_{th}$  at the end of the second part of the programming period. Furthermore,  $V5^{final}$  carries a negative value since the data provided by the data driver is negative. Consequently, the OLED is reversed bias during this period which prevents the OLED from light emitting during this period to ensure a high contrast ratio displays. The second part of the data programming is only  $5\mu s$  performed simultaneously for all the pixels.

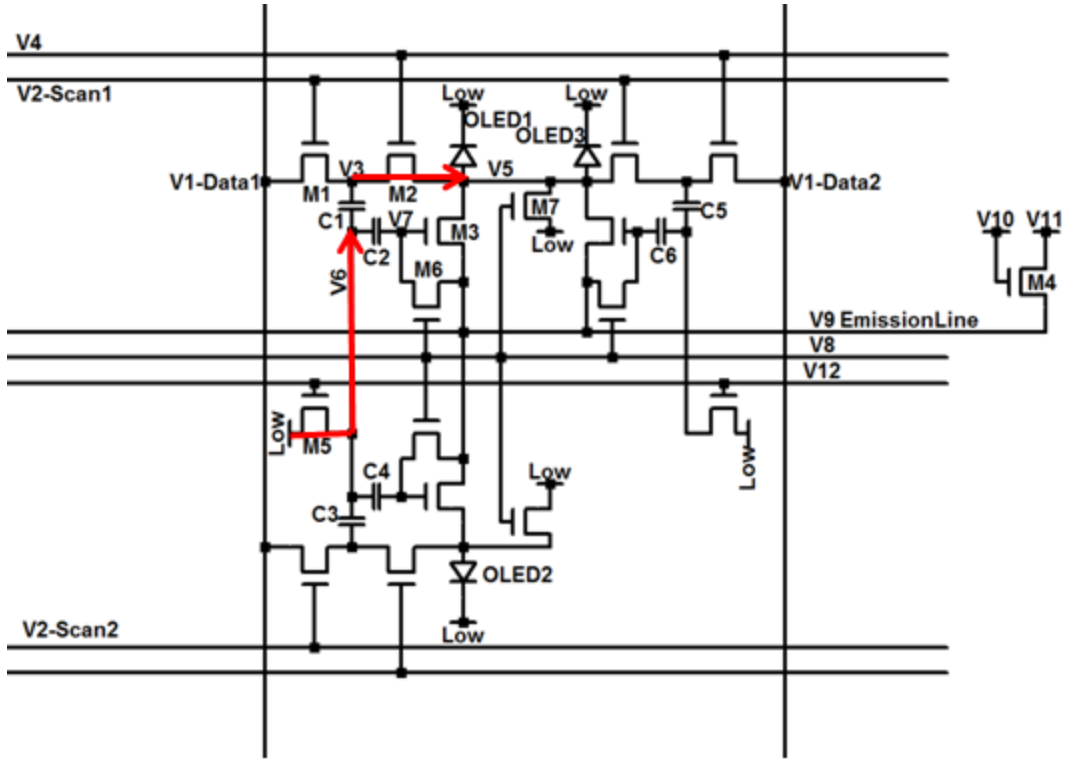


Figure 31: Second part of data programming, V5 is modulated for all the pixels by V3 which includes the data voltage while node 6 is fixed to predetermined voltage.

### (C) Emission

After the first and second data programming period, voltage lines 8 (V8), 12 (V12), scan lines (V2) carry a low voltage to turning off M1, M5, M6 and M7. However, voltage lines 4 (V4) and 10 (V10) carry a high voltage to turning on M4 and M2. Therefore, the gate-source voltage of driver transistor T3 at the of (B) period is

$$VGST3 = Vth - V5^{final} \quad (6)$$

$V5^{final}$  is a negative value and the OLED current could be expressed as

$$I_{OLED} = \frac{KM3}{2} (VGSM3 - V_{th})^2 = \frac{KM3}{2} (-V5^{final})^2 \quad (7)$$

$KM3$  is  $\mu_n * C_{ox} * (W/L)$ . Based on the above equation, the emission current is independent of the  $V_{th}$  of  $M3$  and the OLED voltage, where the operation is depicted in Figure 32. Consequently, the proposed circuit compensates the instability of threshold of thin-film transistor (TFT) and degradation of organic-light emitting diode (OLED). In addition, the proposed circuit should be able to compensate and write data at the same time.

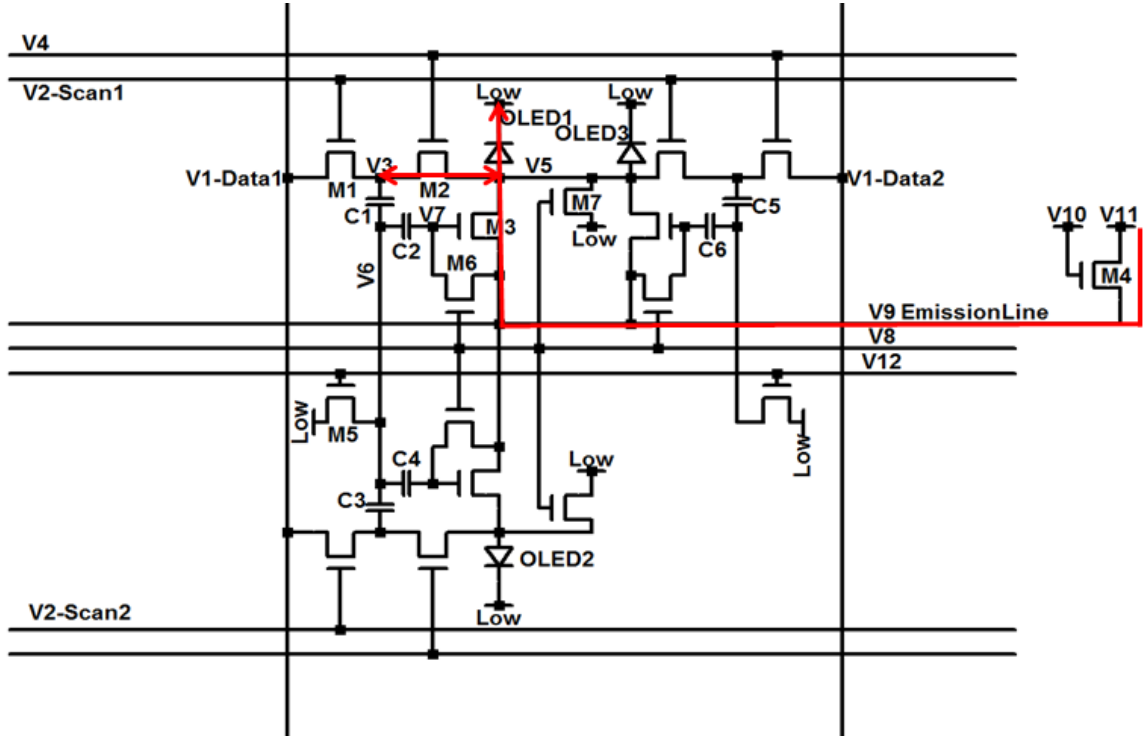


Figure 32: Emission Line raises  $V9$  and thus current flows through the OLED based on the voltage stored in  $C1$  and  $C2$

To verify the proposed pixel circuit, the circuit simulation is performed using AIM-SPICE software and the model is a Low Temperature Poly-silicon LTPS (level = 16). The circuit parameters are listed in Table 2. The OLED is modeled by a diode-connected TFT in parallel with a capacitor.

**Table 2: Simulation Parameters of the proposed simultaneous compensation and data programming periods using two sharing transistors including sizing of the transistors, capacitors and voltage supplied by the data line, scan line, emission line and the global lines**

W/L (M1)	5 $\mu$ /5 $\mu$
W/L (M2)	9 $\mu$ /5 $\mu$
W/L (M3)	6 $\mu$ /5 $\mu$
W/L (M4)	20 $\mu$ /5 $\mu$
W/L (M5)	5 $\mu$ /5 $\mu$
W/L (M6)	5 $\mu$ /5 $\mu$
W/L (M7)	5 $\mu$ /5 $\mu$
C1	1pf
C2	5pf
V2 (scan voltage)	-10v to 0v
V1 (data voltage)	-2v to -8v
V4	-10 to 15v
V8	-10 to 15v
V12	-1 to 10v
V10	-10V to 20v
V11	5 to 15v

Low (common voltage)	0V
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Figure 33 and Figure 34 illustrate transient simulations including waveforms V7 (gate of M3), V5 (source of M3) and Ioled (current of OLED) corresponding to pixel 1. As shown above, the threshold of the driver transistor M3 is stored at the end of the compensation period (2) in order to compensate for the instability of the TFT. In addition, Figure 33 and Figure 34 illustrate that the OLED is reverse bias during the initialization, compensation, first programming data and second programming data period. Subsequently, the proposed circuit improves the degradation of the OLED.

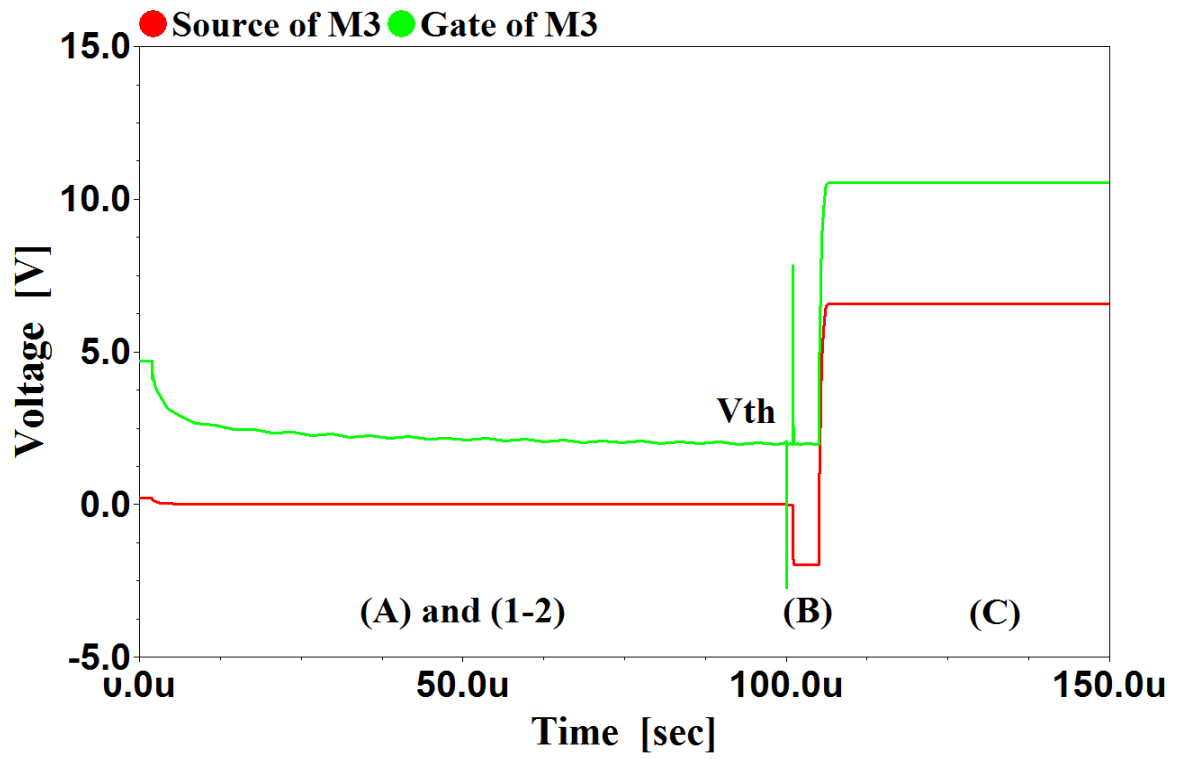


Figure 33: Simulated transient characteristics of V7 and V5 when data is -8V including first programming period (A), second programming period (B), emission period (C) and compensation period (1-2), where  $V_{th}$  is stored in node V7 at the end of the compensation period

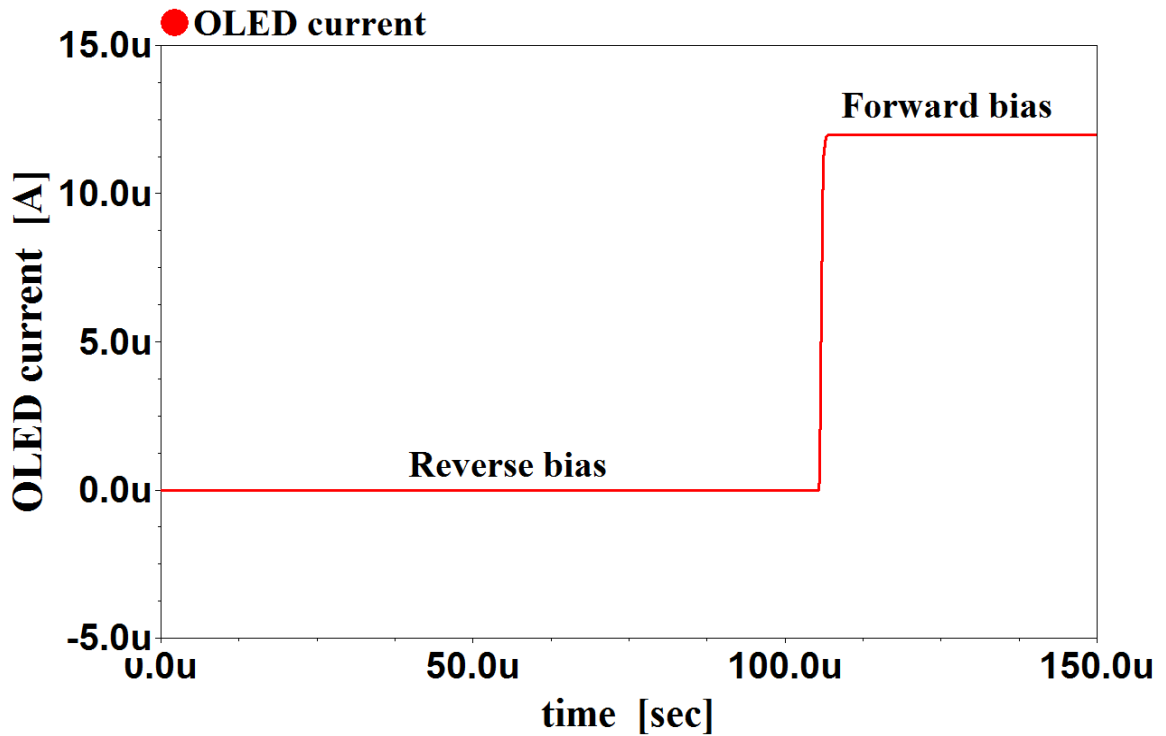


Figure 34: Simulated Ioled Characteristics when data is -8v, OLED is reversed bias during the non-emission periods and forward bias during the emission period

Figure 35 illustrates the simulated voltage data versus current for different variations of  $V_{th}$ , where  $\Delta V_{th1}$  includes a variation of -0.5 of the threshold voltage,  $\Delta V_{th2}$  includes a variation of 0 of the threshold voltage and  $\Delta V_{th3}$  includes a variation of 0.5 of the threshold voltage. Figure 36 illustrates the maximum error percentage corresponding to a particular data voltage calculated as suggested in equation 4. As depicted in Figure 36, the maximum error percentage is below to 3.6%.



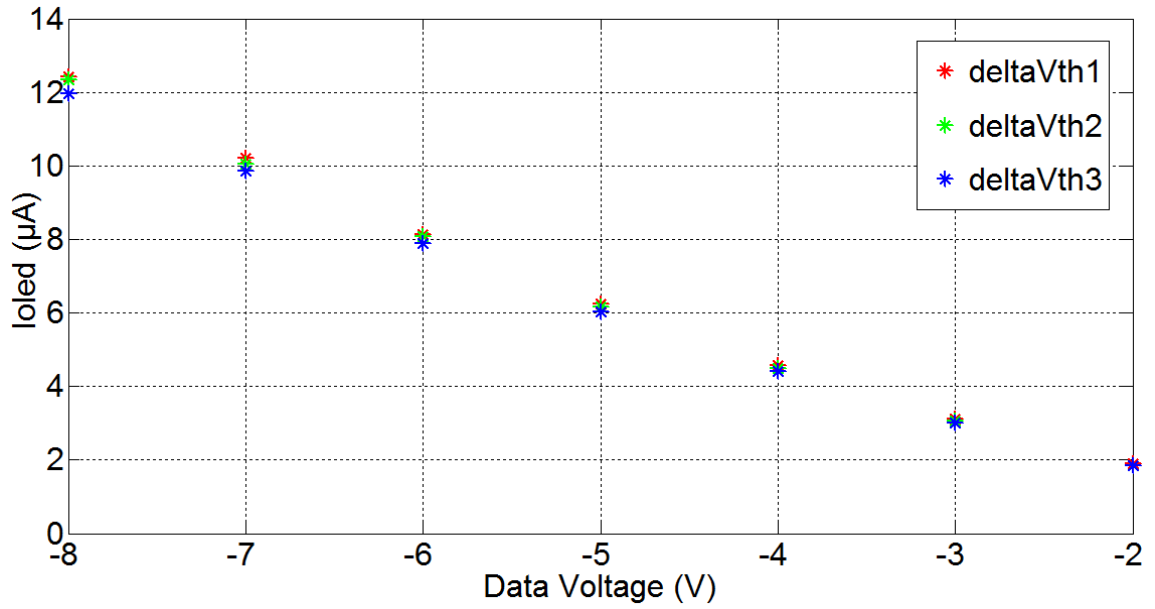


Figure 35: Simulated compensation results of the proposed circuit with  $I_{oled}$  versus  $V_{data}$  for different variation of  $V_{th}$ , deltaVth1 corresponds to a variation of -0.5V of the threshold voltage, deltaVth2 corresponds to a variation of 0V of the threshold voltage and deltaVth3 corresponds to a variation of 0.5V of the threshold voltage

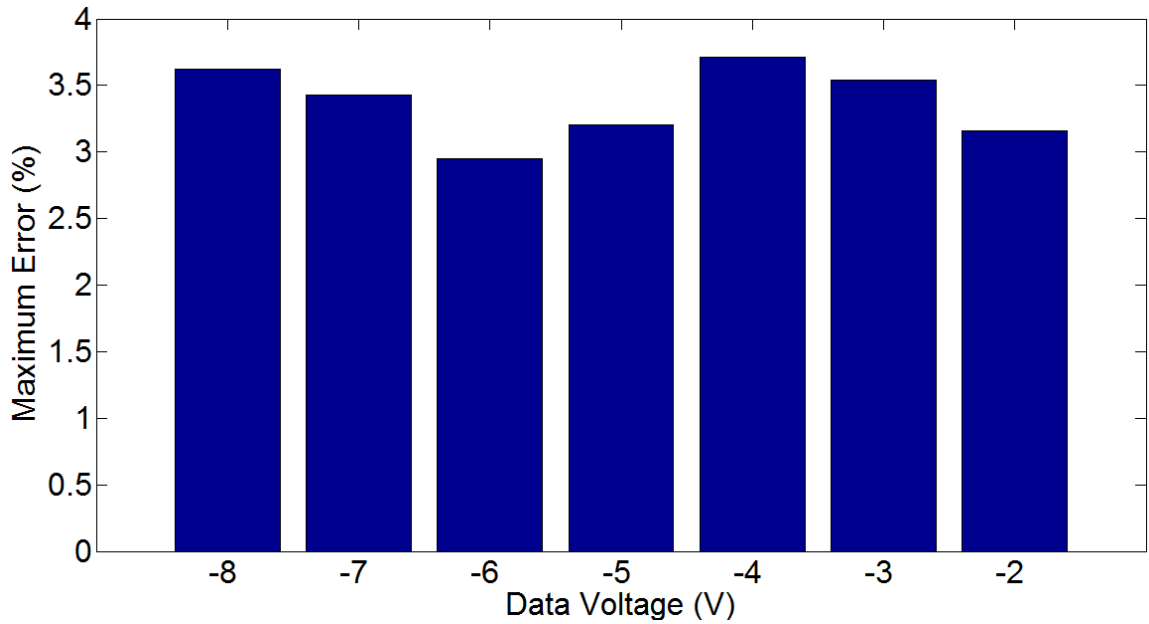


Figure 36: Data Voltage versus Maximum Error (%) of the circuit, the Maximum Error is the error for the maximum variation of current for each data voltage.

Therefore, it is demonstrated that an accurate compensation for threshold voltage variation of the driver transistor and degradation of OLED using a simultaneous data and compensation period have been achieved due to the generation of a long compensation period. The long compensation period is possible since the compensation and the data programming run concurrently. The proposed method allows operation at 240Hz for HD and UHD.

### **3.5 Simultaneous Compensation and Data programming periods having a sharing transistor**

Figure 37 illustrates an active area of a display panel including the layout for only two neighbors' pixels. However, the display any include any number of PXs as depicted in Figure 16. The first pixel includes four unshared transistors and one shared transistor (M6) as annotated in Figure 37. The share region is implemented to decrease the number of transistors per pixel and thus improving the resolution of the display. Thus, pluralities of share regions are located among neighbors' pixels. The first pixel includes global voltages V4, V8, V10, Low and Emission Lines. Figure 38 illustrates the driving scheme for the proposed circuit.

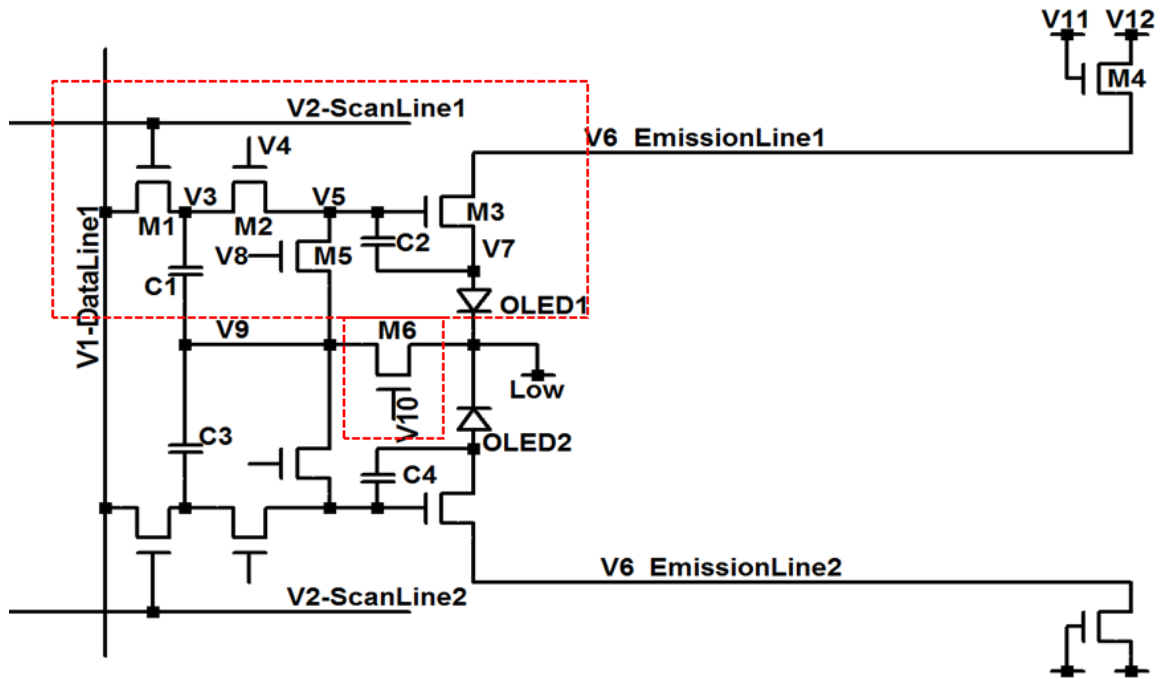
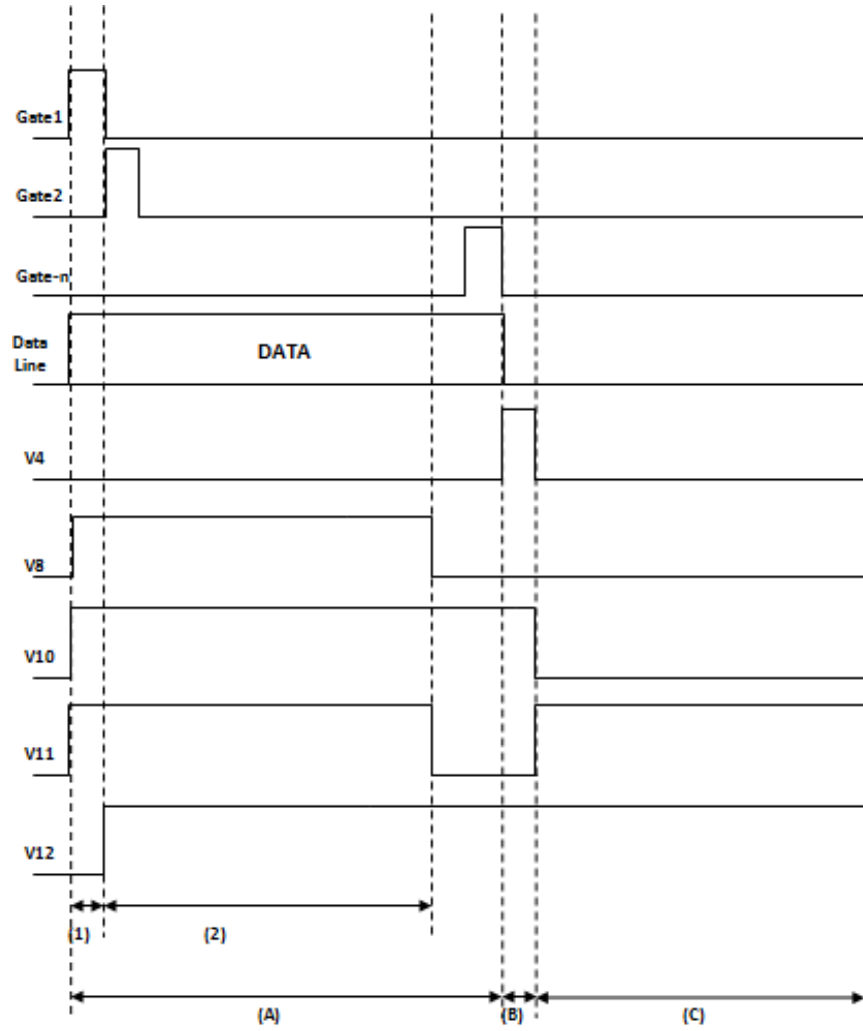


Figure 37: Circuit schematic of a simultaneous compensation and data programming periods having one sharing transistor in order to improve the aperture ratio of the pixel.



**Figure 38: Driving Scheme for the proposed circuit including (A) first part of the data programming, (B) second part of the data programming and (C) emission period, where initialization period (1) and compensation period (2) are performed while (A) is performed**

The proposed circuit operation would be described in conjunction with Figure 37 and Figure 38. M1, M2 and M4-M6 are switching TFTs and M3 is the driving TFT, C1 and C2 modulate data voltage and the threshold voltage of M3. V1 is the data line, which is connected to the data driver as shown in Figure 16. V2 is the scan line, which is

connected to the gate driver as shown in Figure 16. V11 is the control voltage line of M4 located in the emission driver. V12 is a power supply connected to the emission line V6 when M4 is turned on. V12 also provides a reset signal to node 7. The emission driver is located in the outer region of the active area of the display as depicted in Figure 16. The operation of the proposed is divided in two steps in each frame, where the first step performs the data programming (A-B) and compensation simultaneously (1-2). The second step (c) is the emission period. The data programming is divided in two parts (A) and (B) and the compensation is divided in two parts (1) and (2), where (1) is the initialization step and (2) is the final compensation step.

(A) First part of Data programming

(1) Initialization Step

In the initialization step, the control voltage V11 goes high to turn on M4 while V8 and V10 go high to turn on M5 and M6. Thus, node 5 (V5) is fixed at a first reference voltage through M5 and M6 and node 7 (V7) is reset to a negative potential (V12) through M4, M3 and the emission line (V6). Simultaneously, the data driver and scan driver start writing data into node 3 (V3) by turning on the transistor M1. The data programming is performed sequentially for entire display while the pixels reset and compensate. The data writing time is only  $1.9\mu\text{s}$  per row and thus allowing operation at 240Hz for HD (1920x1080) and UHD (4096x2160). The operation of this period is shown in Figure 39. In addition, the OLED is reversed bias during the initialization period since the reset potential provided by the emission driver is negative which not only

prevents the OLED from light emitting during the programming period to ensure a high contrast ratio displays, but also suppresses the OLED degradation and thus extends the lifetime of the AMOLED.

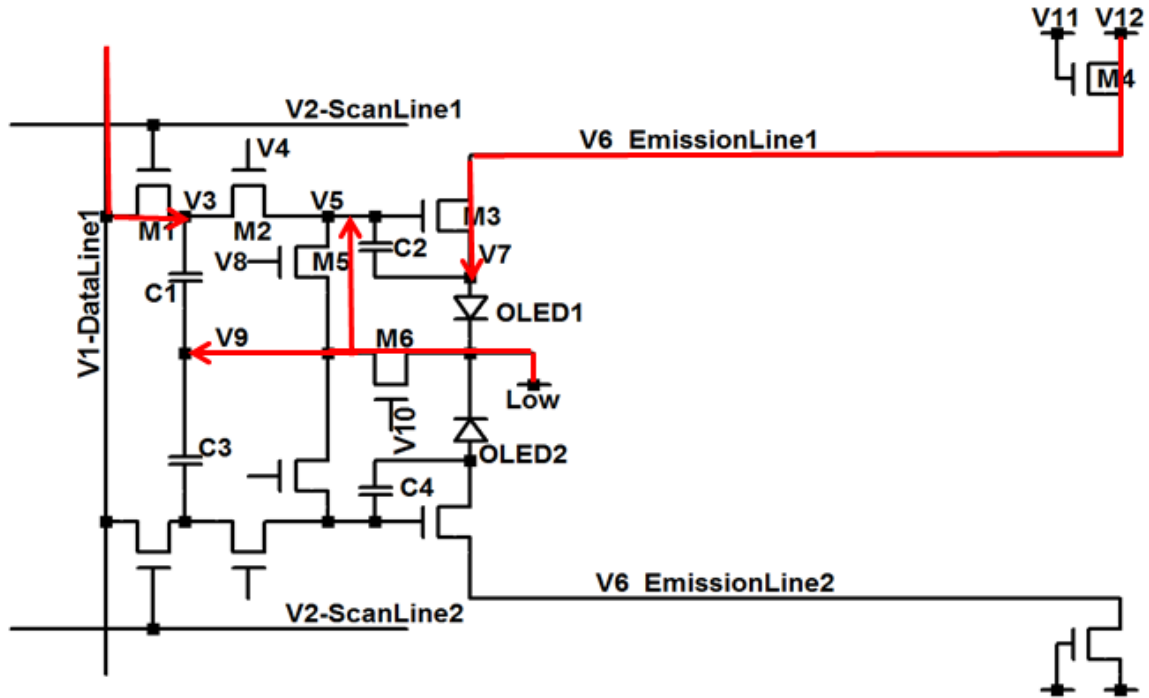


Figure 39: (A) First part of data programming and (1) initialization step, data voltage is programmed into V3 while V5 and V9 are fixed to a low voltage, and V7 is programmed to a negative predetermined value via TFT M3

## (2) Compensation Stage

During the compensation step, the voltage lines V8 and V10 maintain a high voltage to keep on M5 and M6. Thus, node 5 (V5) is fixed to a first reference voltage ( $V_{ref1}$ ). V11 maintains a high voltage to keep on M4 in the emission driver. However,

the power supply V12 is changed to a high voltage which is connected to the emission line through M4. Therefore, the voltage of node 7 (V7) is charged up through the driver transistor M3, M4 and the emission line until M3 is turned off. In the end of this period, the voltage of node 7 (V7) reaches a  $-V_{th}$  voltage, where  $-V_{th}$  is the threshold voltage of the driver transistor M3. During the compensation stage, the data driver and scan driver continue writing data sequentially for the remaining display pixels as shown in Figure 40. The length of the reset period (1) compensation period (2) can be as long as the length of the programming period (A). Subsequently, this approach would be able to increase the accuracy of the compensation due to the fact that the length of the compensation period can be adjusted in order to maximize the accuracy and minimize the error. In addition, the OLED is reversed bias during the compensation period which prevents the OLED from light emitting during this period to ensure a high contrast ratio displays.





$$V5^{final} = \frac{C2*V5^{init} + C1*V3^{init}}{C1 + C2} \quad (8)$$

$V5^{final}$  is the final voltage of V5,  $V5^{init}$  and  $V3^{init}$  are the initial voltage of V3 and V5 respectively. In addition, V5 represents the gate of the driver transistor M3 and V7 represents the source of the driver transistor M3. Based on the charge conservation, node 7 (V7) is modulated as

$$V7 = (V5^{final} - V5^{init}) * \frac{C2}{C2 + C_{oled}} - V_{th} \quad (9)$$

V7 carries a voltage value less than the threshold of the OLED at the end of the second part of the programming period. Consequently, the OLED is off during this period which prevents the OLED from light emitting during this period to ensure a high contrast ratio displays. The second part of the data programming is only 10 $\mu$ s performed simultaneously for all the pixels and the operation is illustrated in Figure 41.

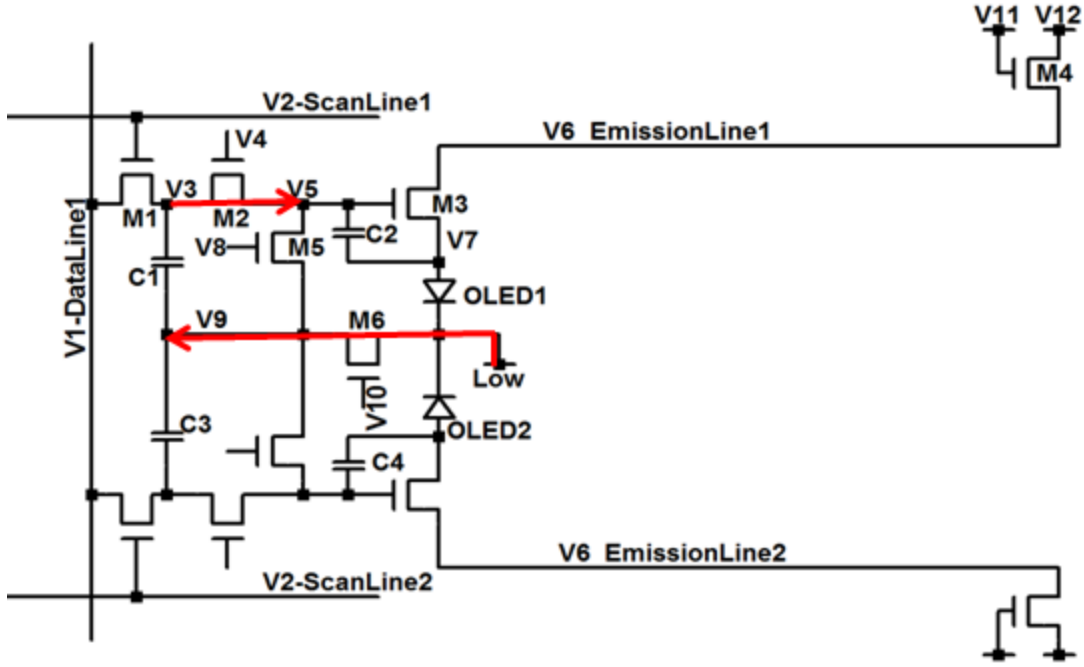


Figure 41: Second part of data programming, V5 is modulated for all the pixels by V3 which includes the data voltage while node 9 is fixed to predetermined voltage.

#### (A) Emission

After the first and second data programming period, voltage lines V8, V10, V4 and scan lines (V2) carry a low voltage to turning off M1, M2, M5 and M6. However, control voltage line 11 carries a high voltage to turning on M4. Therefore, the gate-source voltage of driver transistor T3 at the of (B) period is

$$VGSM3 = (V5^{final} - V5^{init}) * \frac{C_{oled}}{C1 + C_{oled}} + V_{th} \quad (10)$$

As mentioned above, the final voltage of V5 depends from V3 and thus from the data voltage according to equation (8). The OLED current could be expressed as

$$\begin{aligned}
I_{OLED} &= \frac{KM3}{2} (VGSM3 - V_{th})^2 \\
I_{OLED} &= \frac{KM3}{2} \left( (V5^{final} - V5^{init}) * \frac{C_{oled}}{C1 + C_{oled}} + V_{th} - V_{th} \right)^2 \\
I_{OLED} &= \frac{KM3}{2} \left( (V5^{final} - V5^{init}) * \frac{C_{oled}}{C1 + C_{oled}} \right)^2 \tag{11}
\end{aligned}$$

$KM3$  is  $\mu_n * C_{ox} * (W/L)$  and the operation is illustrated Figure 42. Based on the above equation, the emission current is independent of the  $V_{th}$  of M3 and the OLED voltage. Consequently, the proposed circuit compensates the instability of threshold of thin-film transistor (TFT) and degradation of organic-light emitting diode (OLED). In addition, the proposed circuit should be able to compensates and write data at the same time.

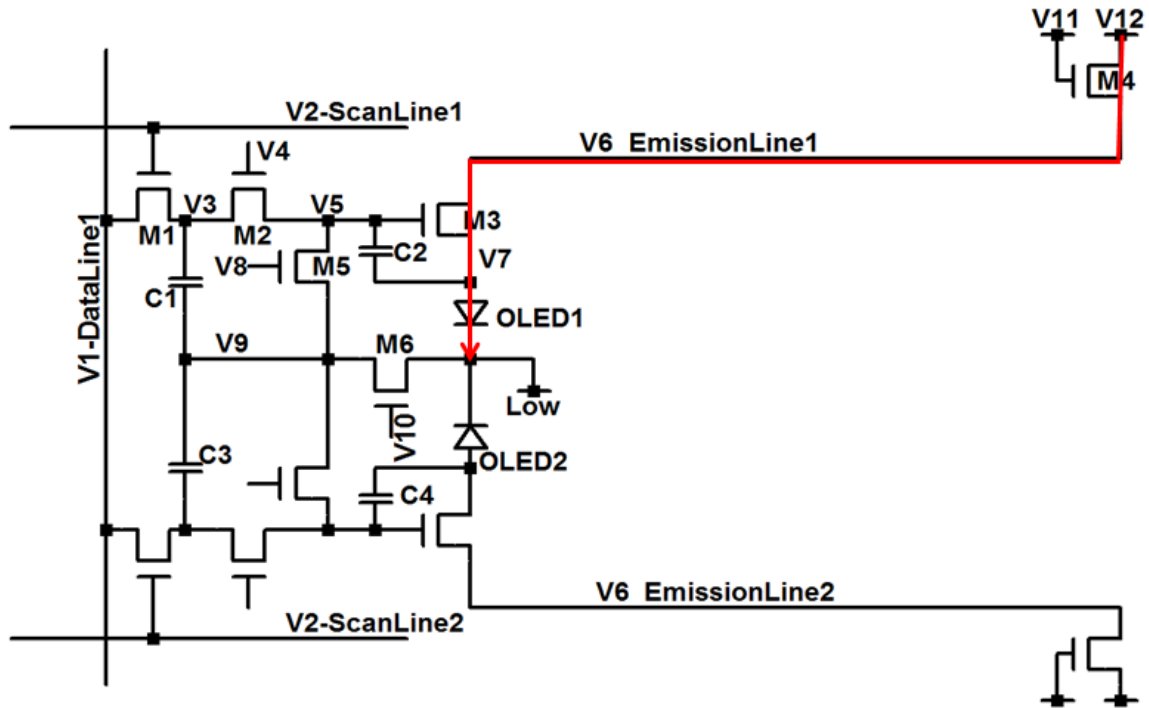


Figure 42: Emission Line raises V6 and thus current flows through the OLED based on the voltage stored in C2

To verify the proposed pixel circuit, the circuit simulation is performed using AIM-SPICE software and the model is a Low Temperature Poly-silicon LTPS (level = 16). The circuit parameters are listed in Table 3. The OLED is modeled by a diode-connected TFT in parallel with a capacitor.

**Table 3: Simulation Parameters of the proposed simultaneous compensation and data programming periods using one sharing transistors including sizing of the transistors, capacitors and voltage supplied by the data line, scan line, emission line and the global lines**

W/L (M1)	6 $\mu$ /5 $\mu$
W/L (M2)	5 $\mu$ /5 $\mu$
W/L (M3)	3 $\mu$ /5.2 $\mu$
W/L (M4)	100 $\mu$ /5 $\mu$
W/L (M5)	5 $\mu$ /5 $\mu$
W/L (M6)	5 $\mu$ /5 $\mu$
C1	4pf
C2	5pf
V2 (scan voltage)	0v to 15v
V1 (data voltage)	8v to 10v
V4	0v to 15v
V8	0v to 5v
V12	-5 to 10v
V10	0V to 5v
V11	0 to 20v
Low (common voltage)	0V

Figure 43 and Figure 44 illustrate transient simulations including waveforms V5 (gate of M3), V7 (source of M3) and Ioled (current of OLED) corresponding to pixel 1. As shown above, the threshold of the driver transistor M3 is stored at the end of the compensation period (2) in order to compensate for the instability of the TFT. In addition,

Figure 43 and Figure 44 illustrate that the OLED is reverse bias during the initialization, compensation, first programming data and second programming data period. Subsequently, the proposed circuit improves the degradation of the OLED.

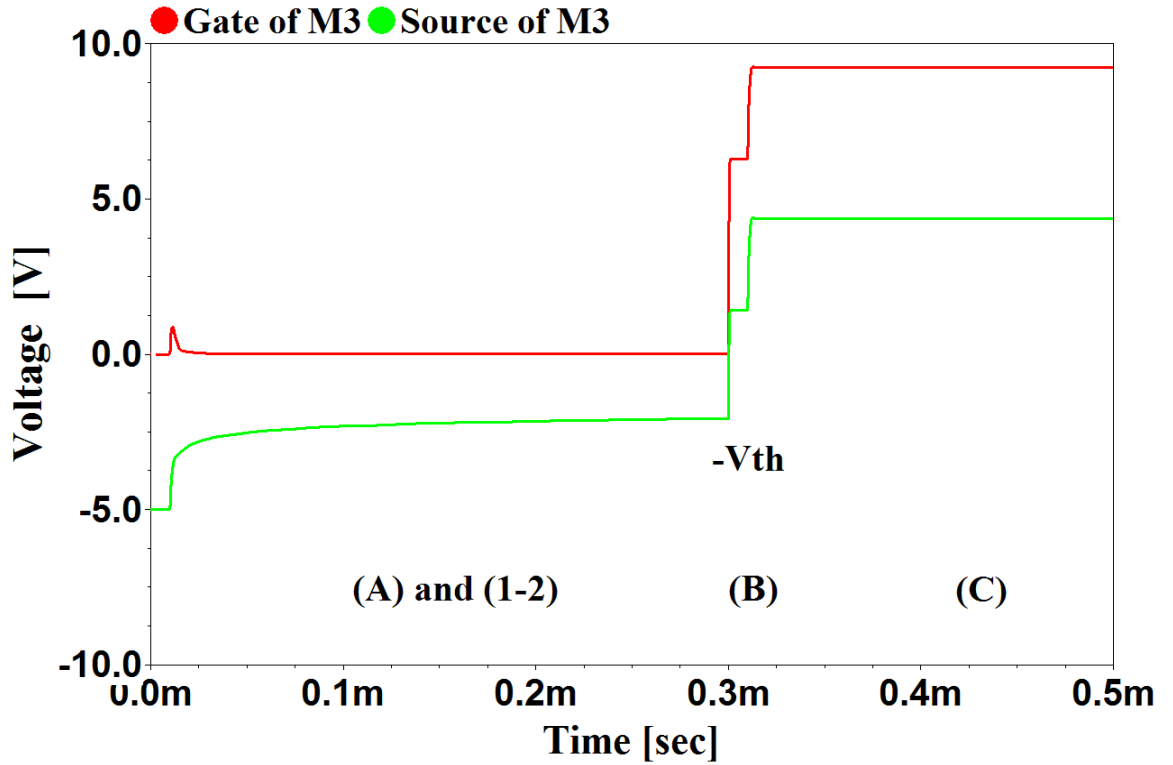


Figure 43: Simulated transient characteristics of V5 and V7 when data is 8V including first programming period (A), second programming period (B), emission period (C) and compensation period (1-2), where  $-V_{th}$  is stored in node V7 at the end of the compensation period

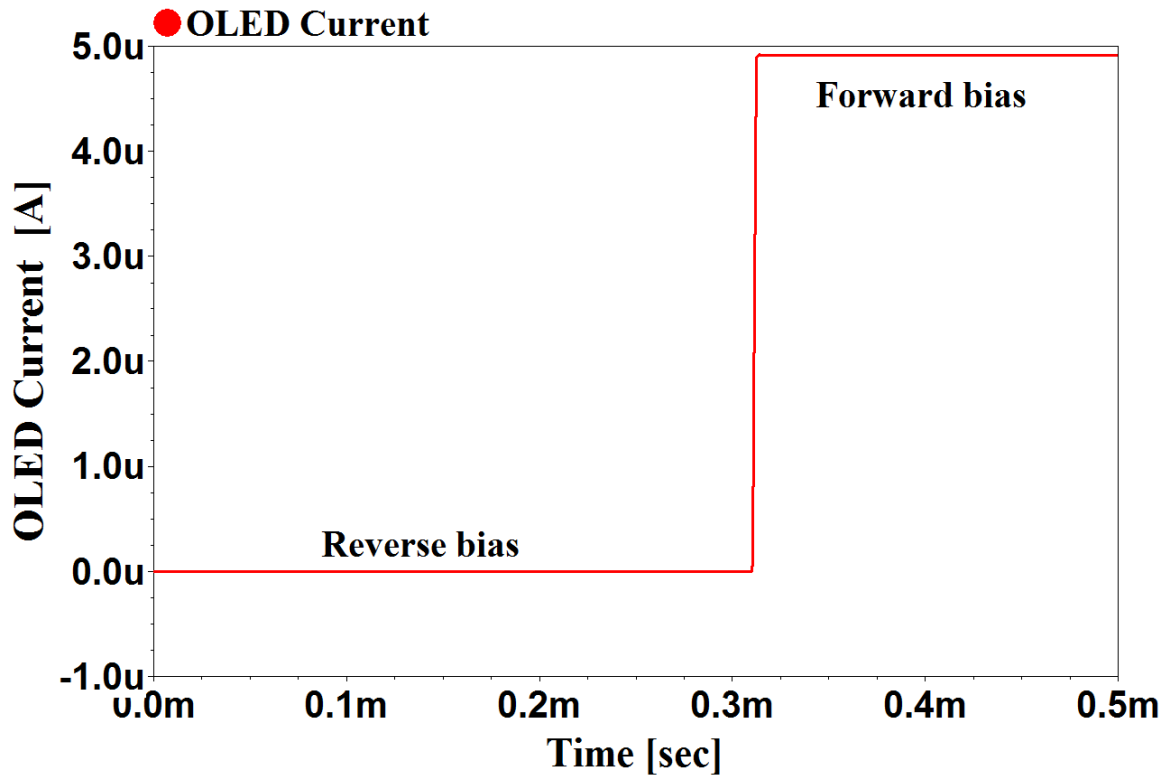
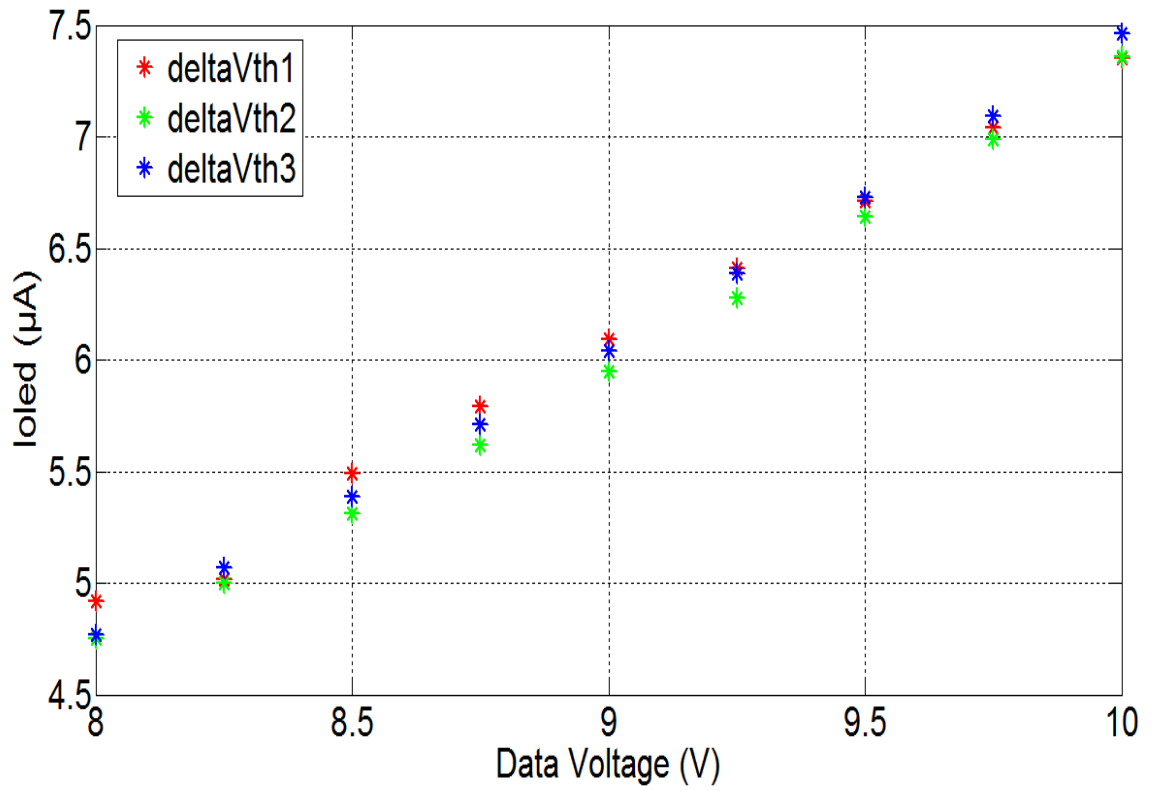


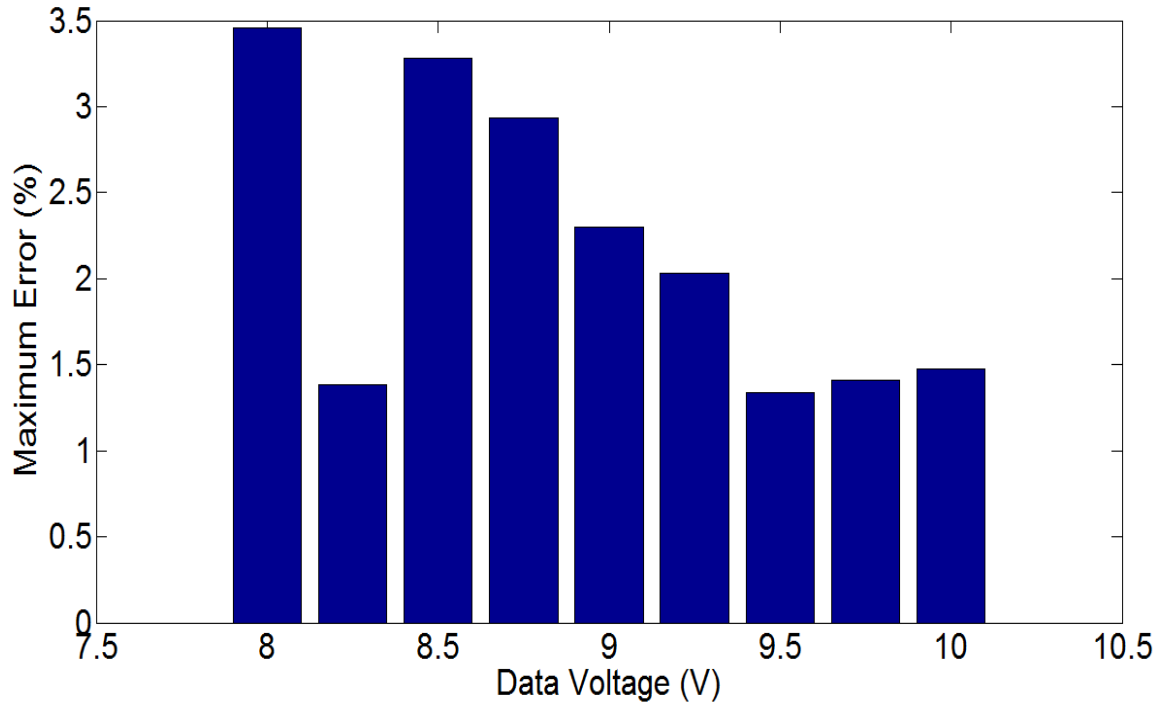
Figure 44: Simulated Ioled Characteristics when data is 8V, OLED is reversed bias during the non-emission periods and forward bias during the emission period

Figure 45 illustrates the simulated voltage data versus current for different variations of  $V_{th}$ , where  $\Delta V_{th1}$  includes a variation of -0.5 of the threshold voltage,  $\Delta V_{th2}$  includes a variation of 0 of the threshold voltage and  $\Delta V_{th3}$  includes a variation of 0.5 of the threshold voltage. Figure 46 illustrates the maximum error percentage corresponding to a particular data voltage calculated as suggested in equation 4. As depicted in Figure 46, the maximum error percentage is below to 3.4%.



**Figure 45: Simulated compensation results of the proposed circuit with  $I_{oled}$  versus  $V_{data}$  for different variation of  $V_{th}$ ,  $\Delta V_{th1}$  corresponds to a variation of  $-0.5V$  of the threshold voltage,  $\Delta V_{th2}$  corresponds to a variation of  $0V$  of the threshold voltage and  $\Delta V_{th3}$  corresponds to a variation of  $0.5V$  of the threshold voltage**





**Figure 46: Data Voltage versus Maximum Error (%) of the circuit, the Maximum Error is the error for the maximum variation of current for each data voltage.**

Therefore, it is demonstrated that an accurate compensation for threshold voltage variation of the driver transistor and degradation of OLED using a simultaneous data and compensation period have been achieved due to the generation of a long compensation period. The long compensation period is possible since the compensation and the data programming is performed concurrently.

## CHAPTER 4 SUMMARY

### 4.1 Comparison of proposed circuits

Table 4: Comparison result of the proposed circuits based on number of transistors, capacitors, length of compensation period and accuracy error.

	2T1C	Simultaneous Data/Compensation 1	Simultaneous Data/Compensation 2
Unshared Transistors and Capacitors	2 transistors, 1 capacitor	4 transistors, 2 capacitors	4 transistors, 2 capacitors
Shared Transistors	none	2 sharing transistors	1 sharing transistor
Length of compensation period	10 $\mu$ s	100 $\mu$ s	300 $\mu$ s
Accuracy Error	7%	3.6%	3.4%

Table 4 illustrates that the proposed circuits are capable to enhance accuracy of the compensation. The 2T1C design includes a simple schematic made of two transistors and one capacitor. However, the accuracy error is greater than the other approaches due to the small compensation period. The simultaneous data/compensation approaches improve the accuracy by about 50% with respect to a 2T1C. However, it increases the

number of active elements and capacitor. This issue has been alleviated by the incorporation of sharing transistors.

## **4.2 Conclusion**

As demonstrated in previous sections, the compensation of threshold variation of the driver transistor and OLED degradation are critical and top priorities in the development of OLED's display technology. However, the trade-off of compensation, speed and error provides a plurality of challenges. Specially, as the frequency of operation increases, the response time and thus the compensation becomes a difficult task to accomplish. Similarly, as the resolution increases, the pixel schematic design needs to be more efficient. Therefore, the plurality of trade-off and requirements for next display generations attest that there is a huge room for developments and improvements. Several approaches have been investigated in this thesis in order to compensate the deterioration of the TFT and OLED. It have been demonstrated that an accurate compensation for threshold voltage variation of the driver transistor and degradation of OLED using a simultaneous data and compensation period have been achieved due to the generation of a long compensation period. The long compensation period is realizable due to the fact that the compensation and the data programming periods are performed concurrently. The maximum error was 3.6% for a first approach and 3.4% for a second approach when compensation and data programming periods are performed simultaneously. In addition, an accurate compensation for threshold voltage variation of the driver transistor and

degradation of OLED have been explored using a simple 2T1C circuit schematic having an error less than 7% which is a huge improvement in comparison to the 90% error of conventional 2T1C. The operation of the compensation takes around 13  $\mu$ s for proposed 2T1C schematic which is below to the conventional proposed circuits. Furthermore, it have been shown that the number of the transistors have decreased by using sharing transistors and thus improving the resolution and cost of the display. Consequently, the new driving methodologies and circuit schematics have been improved the performance of display pixel circuit with a accurate compensation of the instability of threshold of thin-film transistor (TFT) and degradation of organic-light emitting diode (OLED).

### **4.3 Future Work**

The author of this paper visualizes that future work should be based on improving the speed by generating plurality of task at the same time. In other words, two operation or three operations can be driven at the same period including but not limited to resetting, compensating and writing data. In addition, further improvement should be focus on new materials for the driver transistor, OLEDs and more compact designs. Sharing lines, sharing transistors or capacitor among pixels should help to improve the aperture ratio of the pixel.

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## **BIOGRAPHY**

Roberto W. Flores was born in Guayaquil, Ecuador, in 1987. He received his Bachelor of Science in Electrical Engineering from The City College of New York in 2012. Currently, He is pursuing the Master of Science in Electrical Engineering from George Mason University, Fairfax, VA in the field of Microelectronics and Nanotechnology.