NOVEL MOLECULAR MEMORY ON SI AND TWO-DIMENSIONAL MATERIALS

by

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Table of Contents

List of Tables

List of Figures

Abstract

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The dimensional scaling down of microelectronics to further increase the storage ability and density is confronting the fundamental and physical limit. The performance of high density, low power consumption non-volatile memory as the important part in portable electronic devices like cellphone, tablet and laptop will have a drastic impact on these devices. Molecular electronic technology has attracted much attention due to its nanoscale features, flexibly tunable properties and tremendous application prospects, etc. Replacing the currently used traditional flash memory with high-performance Flash-based molecular non-volatile memory for further scaling down, will be an effective method for increasing storage density and stability.

In this study, we introduce the development of molecular electronics in the application of non-volatile memory. Recently, solid-state non-volatile memory devices based on redox-active molecules have been reported, exhibiting fast speed, low operation voltage,

excellent endurance and multi-bit storage, outperforming the conventional floating-gate flash memory. I have fabricated and characterized a kind of Flash-like Ru molecular memory devices. This Ru molecular exhibit excellent memory window under high-frequency CV measurement. The programming and erasing response speed are also suitable for Flash memory applications. The stability of our molecular memory devices is demonstrated by endurance characterization for more than 10^5 cycles. The charge storage in these molecular memory devices is basically derived from the intrinsic redox processes lead by a sweeping gate voltage bias. Compare with the traditional flash memory, the intrinsic redox and the stable molecular properties lead to a very reliable and high-density charge storage ability.

Two-dimensional materials, especially layered transition metal dichalcogenides (TMDCs), such as molybdenum disulfide (MoS2) and tungsten diselenide (WSe2) have recently become superstar materials as nanomaterials for future flexible, portable and high-performance electronic devices due to their excellent physical, electrical and mechanical properties. We have developed approaches of redox-active molecule attachment on 2-dimensional materials. Redox-active molecular memory based on 2-dimensional materials have been fabricated and measured. Our finding about redox-active molecule provides many opportunities for novel non-volatile memory applications.

Chapter 1 Introduction

1.1 The development of CMOS scaling and Impact on Memory

The scaling of Metal-Oxide-Semiconductor field-effect transistor (MOSFET) will continues with the new emerging technologies to extend Complementary Metal-Oxide-Semiconductor (CMOS) beyond 22-nm technology node have been proposed by the 2013 International Technology Roadmap for Semic. onductors (ITRS) [1]. However, the conventional path of scaling planar CMOS will face significant challenges set by performance and power consumption requirements. Dennard et al. set forth the trend of CMOS scaling has deviated from the prediction of Moore and the scaling rules due to technical and physical limitation in recent years [2, 3]. System scaling enabled by Moore's scaling is more and more challenged with the scarcity of resources such as power and interconnect bandwidth. Particularly due to the development of cloud, seamless interaction of big-data and instant data have become a necessity [4]. 5-nm node where the lithography scale approaches a few times of atom diameter will probably be the stop point of future CMOS scaling [5-7]. Scaling limitation of thin gate oxide, channel length modulation and system series resistance have become a growing concern about maintaining density, speed, reliability and power dissipation despite the introduction of high-k materials.

Different approaches toward CMOS scaling challenge has been proposed and reported. For example, process based on silicon-on-insulator (SOI) structure, 3-D FET structure and

SiGe BiCMOS technology are considered as effective method to avoid the doping, carrier transportation and series resistance scaling. [8-12]

High-performance, low energy cost and reliable systems built on CMOS architecture are still pursuing driven by development of big-data and instant data [13]. Despite the slow down of CMOS logic device scaling, semiconductor industry growth explosively in this decade. The richness of proposed new materials and novel structures provide opportunities for future semiconductor device applications. DNA methodology, single electron devices, molecular electronics and quantum computing are considered as promising new technologies which receive more and more attention both in industrial and academic research.

Memory device is an essential component in many of these electronic devices for data processing, storage, and communication. With the development of IT technology, Huge market demand has been created for high performance semiconductor devices for future applications in memory and emerging portable/wearable electronic devices. Solid-state mass storage occupies a growth portion of memory market, due to its compatibility with CMOS process technology, non-volatile keep the data without power supply and reliability in harsh environment without mechanical parts. Typically, non-volatile memory including these types of memory: ferroelectric random-access memory (FeRAM), Magnetic random-access memory (MRAM), resistive random-access memory (RRAM), phase-change random-access memory (PCRAM), and Flash memory [14-17]. They have been well developed and investigated during these decades.

Non-volatile memory is typically applied for the long-term storage task. Which

usually does not need extremely fast Program/Erase (P/E) speed or integration density. the non-volatile market is expected to gain momentum due to explosive development of portable, smart device and big-data centers. A variant of charge storage memory referred to as Flash memory is widely used in consumer electronic products such as cell phones and music players while NAND Flash-based solid-state disks (SSDs) are increasingly displacing hard disk drives as the primary storage device in laptops, desktops, and even data centers [18]. The industry is expected to gain momentum owing to increasing demand for high scalable, fast and economical memory solutions. With increasing data there is an increasing need to manage and store the data and information for future references. The growing demand for mass storage and universal storage devices is expected to favor market growth over the forecast period. High designing cost and stability in extreme environmental conditions is expected to hinder the growth over the next decades.

Emerging nonvolatile memory technologies such as magnetic random-access memory (MRAM), ferroelectric random-access memory (FeRAM), phase-change memory (PCRAM), resistive random-access memory (RRAM), and molecular flash-like memory, combine the speed of static random-access memory (SRAM), the density of dynamic random-access memory (DRAM), and the non-volatility of Flash memory and so become very attractive as another possibility for future memory architecture. Table 1.1 compares different mainstream non-volatile memory performance.

Table 1. Performance comparison of different non-volatile memory

	NAND Flash	PCRAM	FERAM	MRAM	RRAM
Structure	1T	1T1R	1T1C	1T1R	1T1R
Program voltage	>10V	<3V	1~3V	~2V	1V
Read voltage	2V	2V	~3V	1.5V	0.5V
Speed	ms	ns	ns	ns	ns
Retention	10 years	10 years	10 years	10 years	10 years
Endurance	10^5	10^9	10^{12}	10^{14}	10^5

From Table 1, we can find out that each of them has drawbacks and the best candidate for next-generation non-volatile memory technology is undetermined. As such, scientist and engineers have been devoting effort on emerging technologies aiming to go beyond physical limitations and potentially replace all or most of the existing semiconductor memory technologies [19-20].

1.2 Flash memory technology

All through the non-volatile memory candidates for primary storage, Flash memory is the most widely investigated and commercialized non-volatile memory. Flash memory market size is more than 30 billion dollars in fy2016 as a major part of total memory revenue [21]. Flash memory is a very successful industrial product due to its fast read times, good reliability and compatibility with CMOS process technology [22-23].

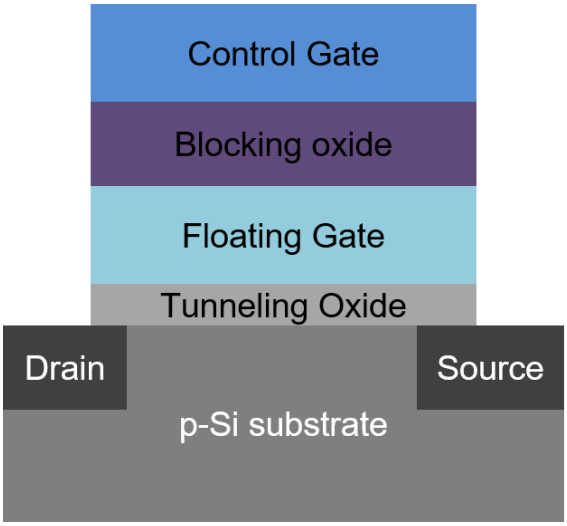

Figure 1 Illustration of a floating-gate Flash memory cell

Figure 1.1 shows the structure of a Flash memory cell. Also known as the floating gate memory, a Flash memory cell is composited by intercalate a floating gate inside the MOSFET gate oxide. The storage method of a Flash memory is trapping and de-trapping electrons in the floating gate, which is sandwiched by a relatively thick blocking oxide layer and a thin tunneling oxide, respectively. As the isolation by two nearby dielectric oxide, the stored electrons can remain for a long period. Flash memory was supposed to replace the Electrically erasable and programmable read-only memory (EEPROM) rapidly in every application at the end of 1980s. There are two main memory architecture of flash memory – NOR flash memory and NAND flash memory based on the way that the memory cells are organized. Two type memory architectures are illustrated in Figure 1.2.

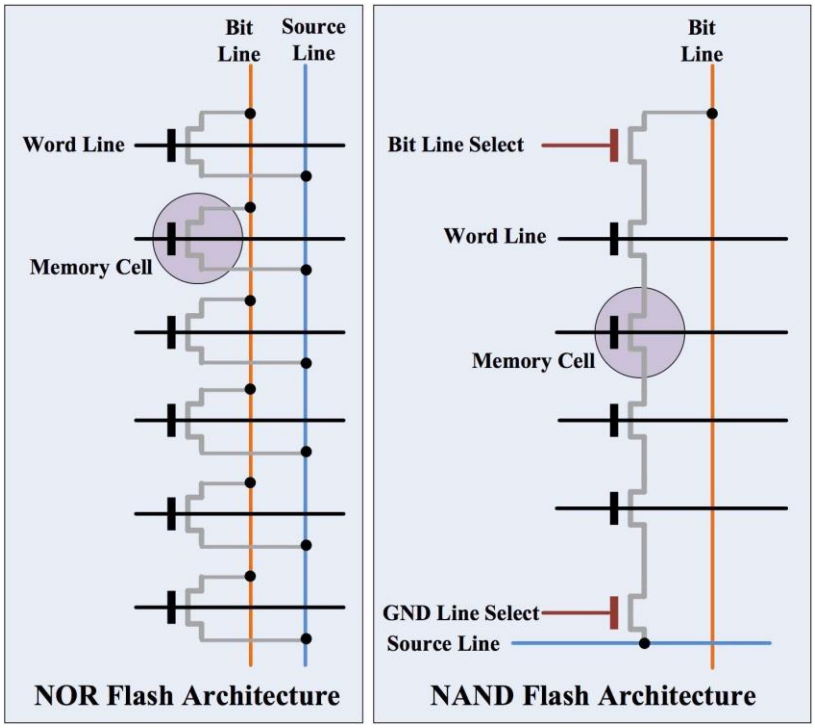

Figure 2 NOR and NAND Flash architecture

Toshiba developed flash memory from EEPROM in the early 1980s and commercialized flash memory in 1984. First NAND flash memory technology was presented by Toshiba at IEEE international Electron Devices Meeting (IEDM) in 1987 and Intel introduced the first commercial NOR flash chip in 1988. In NAND flash memory, several memory cells (typically 8 cells) are connected in series similar to a NAND gate, by that NAND flash memory realized the reduction of memory cell area so that a lower bit cost could be achieved. In NOR flash memory, one end of each memory cell is connected to the source line and the other end directly to a bit line resembling a NOR gate. The advantage of NOR flash architecture is address lines are enough to map the entire memory range and gives real random access and short read times. But the memory cell size is larger

and the per bit cost is higher than NAND structure. Based on the cons and pros, NAND flash memory is mainly used for data storage application and NOR flash memory can be used in embedded systems.

In both NAND and NOR flash memory, the cells are organized into erase blocks. This strategy helps compromise the memory performance and fabrication cost. Also, flash memory is able to erase the stored information by entire blocks, lead to a very fast update speed comparing with EEPROM, which update its data by one byte at a time. Flash memory is considered as a preferable technology for many applications which required multi-time reading and writing of large numbers of data, for example, solid state drive and portable memory stick. The storage density, total capacity and performance keep increase as the development of technology scaling. Now the flash memory scalability has already down to 12 nm by Samsung, Micron and Toshiba. The floating gate transistor architecture of a flash memory is compatible with traditional CMOS process. In addition, 3-D flash memory architecture was first manufactured and commercialized by Samsung in 2014, which open a new door to improve the flash memory storage capacity. Figure 1.3 illustrates the schematic architecture of 3-D flash memory.

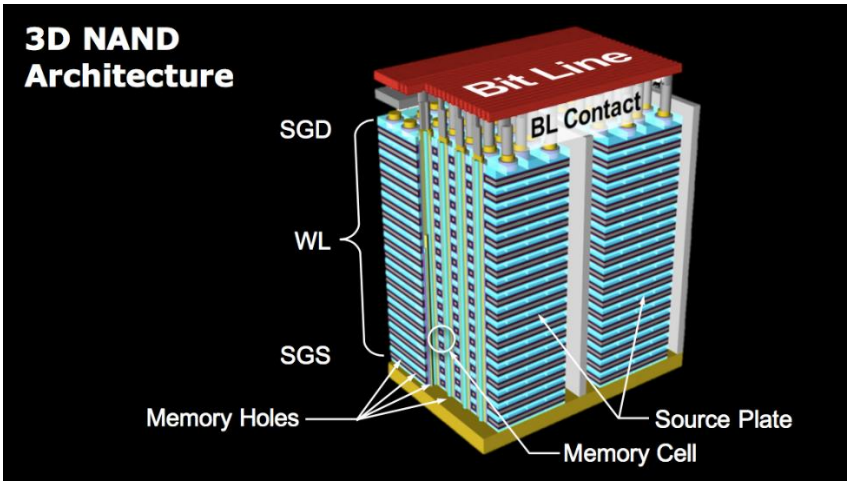

Figure 3 Schematic of 3-D flash architecture

However, the integration limit of flash memory is approaching. The further scaling limitation constrain the flash memory capacity increase. Nowadays, research on memory is toward these goals: lowering operation voltage, scaling down the single memory size and increase the density of state in on cell by multilevel. To keep the trend of continuous scaling, revolutionary changes might happen on traditional flash memory.

1.3 Beyond the floating gate structure

Further scaling requires very thin vertical dielectrics to solve the short channel effects and optimize the memory performance. But serious leakage occurs when the tunneling oxide thickness is below 7 nm due to the defect in tunneling oxide caused by multi program/erase operations, thus lower the memory reliability [24-25]. A conventional floating gate memory device must keep the thickness of tunneling oxide at least 8 nm to

meet 10 years retention time requirement. This necessity will limit flash memory further scaling. Moreover, conventional flash memory still requires a large operation voltage at about 12-15V, which is much larger than CMOS logic devices. For conventional flash memory, if the tunneling oxide could be scaled down to 2nm, the operation voltage could be reduced to 4V. However, the retention time would also be reduced from 10 years to 10 seconds due to stress-induced leakage current (SILC) showing in figure 1.4.

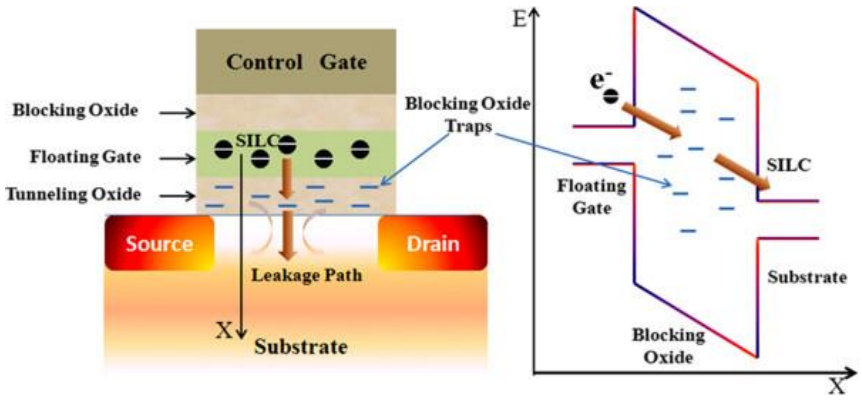

Figure 4 Schematic picture of Strees-induced leakage current (SILC)

The limitation of the tunneling oxide thickness becomes more and more important, Novel storage concepts and materials is becoming attractive as a reasonable solution to overcome some of the further scaling challenge. Charge trapping non-volatile memory is an attractive new flash technology by replace the poly-silicon floating gate with dielectric charge trapping materials [26-28]. The charge trapping non-volatile memory displayed better scalability, good reliability and relative lower operation voltage. Charge trapping

memory technology is derived from the basic structure of conventional flash memory. The Charge trapping memory devices is basically replaced gate oxide of a MOSFET with oxide-charge trapping material-oxide dielectric. Comparing with conventional floating gate flash memory, charge trapping memory has a better retention performance when tunneling oxide is below 8 nm [29]. Besides, charge trapping memory exhibits many other advantages like higher P/E speed. Typically, there are three types of charge trapping memory: polysilicon-oxide-nitride-oxide-silicon (SONOS) memory, nitride based read-only memory (NROM), and nanocrystal memory (NCM) [30-33]. Among these charge trapping memory, the NROM occupied good retention time by applying thicker tunnel layer, but thus lead to higher P/E voltages, and corresponding large power consumption and relative complex voltage pump. NCM's memory performance is good but to keep thee uniformity and control the size of nanocrystal layer is still under research. There is a long journey for NCM from lab to market.

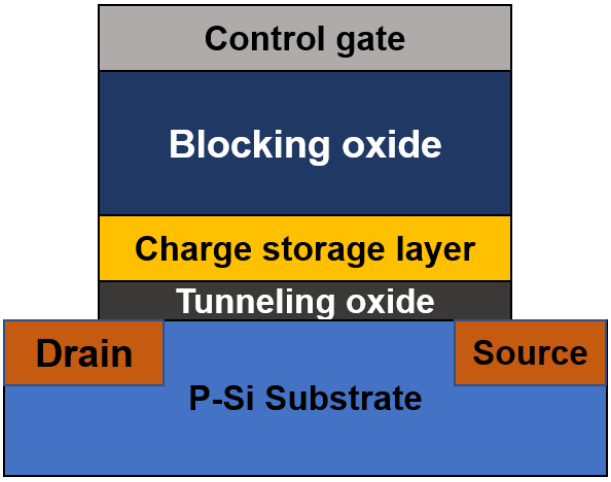

Figure 5 Schematic plot of a SONOS memory cell

SONOS memory has been proposed as a flash technology in 1980s, it exhibits many advantages like easy to fabricate, higher P/E speed, low programing voltage and corresponding low power consumption, even more promising in further scaling according to the ITRS [34]. Figure 1.5 demonstrated the schematic structure of a SONOS memory cell. In SONOS memory, the charge is stored in Si_3N_4 layer. The discrete traps distribution in Si_3N_4 make sure the store charges will not whole leaked through a single defect in tunneling layer, which is better than conventional floating gate memory. The SONOS structure can relieve the scaling problem, but the tunneling oxide thickness about 6 nm is still thick. Shallow-level traps is the reason of leakage at high temperature while scaling down the tunneling oxide thickness which contribute to poor retention property. When the trap level is shallow, erase saturation and vertical electron migration degrade the memory performance [35-36]. Erase saturation is another important draw back of the SONOS memory, it defined as the erase less as the erase voltage increased. Thus, the SONOS

memory cannot be used for NAND flash memory unless important technology innovation.

Recently, many non-volatile memory devices have been proposed on the basis of changing charge storage materials and new memory conception. An important work to improve is gain a trade-off between P/E speed and memory reliability. Many high-k materials including thin films and nanocrystals, such as HfO_2, TiO_2 and ZrO_2, have been proposed as the charge trapping materials to acquire a better scalability and memory performance [37-40]. The memory retention and P/E speed can be improved by applying thicker high-k materials with larger band gap as the blocking oxide materials while the equivalent gate oxide thickness (EOT) is similar. HfO_2 and Al_2O_3 are considered as future blocking oxide candidate to decrease the electric field through the structure [41].

The introduction of molecular electronics provides a new methodology for flash structure improvement. A molecular memory is a non-volatile memory technology that uses organic molecule as the data store material. Memory devices based on organic materials represent one of the emerging technologies [42] for information storage media to improve the memory performance and satisfy the exponential demand for high-density nonvolatile memory for low-power portable devices. In comparison with the traditional flash memory devices, molecular flash memory can be fabricated at low cost and operated with low-power consumption [43]. The types of organic molecules that have been demonstrated with a remarkable memory effect [44-46] and with different basic memory mechanisms have been reported in recent years. The reported new molecule-containing memory included flash memory, resistive switching memory, chargeable electret memory and ferroelectric memory. Among them, the flash memory based on redox-active molecules

has attracted great interest due to their inherent and relatively stable redox process for charge storage [47-51]. Substantial improvement in memory window, retention, endurance and multibit storage capability have been achieved by applying organic molecular floating gate.

The drawback of molecular flash memory is the instability of organic molecule under high temperature. Some redox molecules are not stable at 200 ℃ or higher temperature due to evaporation or other reactions. To solve this problem, specific condition and environment need to employ during the fabrication and CMOS integration process. Although molecular memory can achieve very good performance in some memory characteristics, there is trade-off between each aspect of memory characteristics. Overall, molecular flash memory with the integration of redox molecules in solid-state structure is still attractive due to the intrinsic properties of molecule and compatibility with the CMOS fabrication process. Many studies on organic molecule-based charge trapping memory devices have been reported. Lee et al, reported a strong memory behavior induced by n-type doping to p-type conjugated polymers [28]. Tseng et al, reported a retention improvement caused by applying a double-floating gate which has both hole carrier trap units and electron carrier trap units, with the flexible pentacene molecule acting as the channel allowing a study of the stress effect on flexible charge trapping memory devices [53].

Despite the drawbacks, molecular flash memory with the integration of redox-active molecules into a solid-state structure has still attracted intensive attention lately, due to its excellent performance and compatibility with the CMOS fabrication process. For instance,

devices with metal-molecule-metal structure have been well studied, but this structure is vulnerable to defects and metal penetration. A study on preventing contact metal penetration into the molecular layer in the metal-insulator-molecule-metal structure. But this structure suffers from a series of gate leakage problems. Kim *et al.* reported a study on a metal-oxide-semiconductor structure with molecules encapsulated in gate dielectrics. But the device reliability was not well investigated. [48,51] Up to now, not many studies have yet been reported of the solid-state molecular Flash memory device P/E endurance at fast speed and long time retention. This dissertation focuses on developing hybrid molecular Flash like memory containing redox molecules as store center for charge storage medium to replace current primary data storage drive. We have developed a Si-molecular integration process to preserve the intrinsic redox properties and studied the charge storage properties of the molecular memory. The devices exhibit high P/E speed and low operation voltages and excellent endurance: the devices shows almost no degradation after 10^5 P/E cycles. Robust charge storage behavior can be obtained by employing redox-active molecules with discrete redox states, enabling very stable storage in a given memory storage location. In this thesis, we have demonstrated that the hybrid integration of redox-active molecules on a Si based structure and 2-Dimensional materials is very attractive for high-performance non-volatile memory applications.

1.4 Overview of dissertation

This dissertation This dissertation has been presented in six chapters.

Chapter 1 (this chapter) gives a brief overview to readers about this dissertation. It starts with the history and development of scaling technology. Different non-volatile memories have been discussed. We find the advantages and drawbacks of each kind of memory devices. Chapter 2 presents a thoroughly discussion of the development of molecular non-volatile memory. the novel dielectric and molecular non-volatile memory structure. Fabrication approaches and memory characterization methodology will also be presented in this chapter. Chapter 3 presents the experiment details and characterization of redox-active molecular charge storage memory. Chapter 4 presents the process variation control. It is essential to get stable devices and high uniformity. Several important process like molecule attachment have been discussed in this chapter. Chapter 5 shows 2-D TMDC material based redox molecular memory devices fabrication process and the memory performance. Chapter 6 summarizes this research and presents a path to future research efforts related to this work.

Chapter 2 Fabrication, Operation and Characterization of Molecular Memory

2.1 Introduction

Molecular memory, among the new emerging memory candidates in recent years, is considered promising, particularly for the aim of reducing the size per cell and enhancing the memory speed, density and reliability. Molecular electronic devices are typically fabricated by forming a self-assembled monolayer (SAM) or multi-layer on different surfaces with very inexpensive and simple processing methods. Moreover, molecular memory works by the controlling of fewer electrons at the molecule scale and, therefore, has potential for low-power and ultra-high-density memory applications with a lower fabrication cost. In order to further improve the molecular memory performance. We focused on the gate stack engineering with high-k dielectric materials and redox-active molecules for access flash memory devices with fast P/E speed, good reliability, high storage density and low power consumption. We demonstrated a capacitor structure memory cells, by which charging, discharging and other memory properties can be measured straightforwardly. Metrology of Si based redox-molecular non-volatile memory in the MOSFET technique can be realized by current semiconductor electronics characterization technologies.

As the development of molecular electronics and the integration between semiconductor technology and molecular electronics devices, the Si-molecule hybrid devices will gradually become accessible both in modern electronics research and industry. Great efforts have been made to integrate molecules as the active component for fulfillment of future electronic devices.

2.2 Recent development of molecular memory.

2.2.1 Early stage of molecular memory

Two fundamentally different method to fabricate molecular electronics devices are graphically termed “top-down” and “bottom-up”. Instead of top-down, which includes making nano-scale structures by machining and etching techniques, molecular electronics rely on the “bottom-up” approach, by using the molecule self-assembly property. Bottom-up refers to building organic or inorganic structures by atom-by-atom or molecule-by-molecule techniques. In the past few decades, research on molecular electronics has been focusing more and more on the combination of top-down device fabrication (mainly lithography) with bottom-up molecule self-assembly.

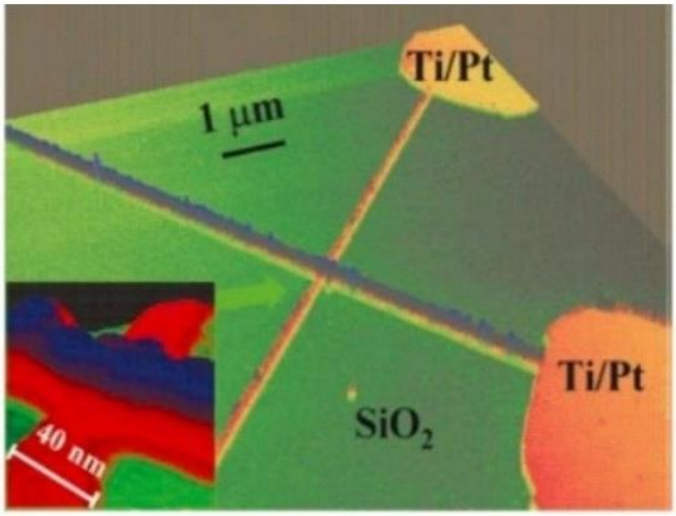

Figure 6 Atomic force microscopy image of a nanoscale cross-point molecular switching device

The crossbar molecular circuit is one of the earliest logic forms of molecular memory arrays. The switching element is a metal/molecule/metal sandwich junction, wherein the molecules are located at the cross-section of two nanoscale metal wires. The early demonstration of such junction molecular switching devices utilized molecules consisting of two mechanically interlocked rings [54-57], the AFM image of the junction they fabricate is shown in figure 2.1. The molecular monolayers were deposited as a film. The mechanical motion of these molecules is an activated redox process, and two stable and electrochemically-switchable states of the molecules form the logic on and off states. The molecular switching devices can exhibit a ~10^2 on/off current ratio, but with limited endurance cycles numbers. Based on such switching devices, an 8 × 8 crossbar has been built by the Hewlett-Packard research group [58]. This approach has the advantage of architectural simplicity and the potential of high density via fabrication of high-density

nanowires array. However, this approach has two major drawbacks, including a high rate of defective switching elements and the difficulty in controlling the metal/molecule interface. Even though a defect-tolerant architecture had been established earlier, the metal/molecule problems in such junction switching devices and crossbar circuits are still to be addressed [59]. In later research work, it was reported that the electron transport phenomena in the metal/molecule/metal junction were molecule independent; instead, they were dominated by electrode reactions with molecules, and the intrinsic spacing of the energy levels might be modified [60–62]. Another architecture utilizing metal/molecule/metal junction is the so-called nanocell molecular circuit, proposed by researchers at Rice University and Yale University [63–66]. A nanocell is a two-dimensional network of self-assembled metallic particles connected by molecules that show reprogrammable negative differential resistance [63,64]. The nanocell is surrounded by a small number of lithographically-defined metal lines that provide input and output leads. The active component for a nanocell is also a metal/molecule/metal switch, and one pathway may include more than one molecular switch [67-69]. The molecule pathways can be learned first by developing appropriate computation algorithms; then, the whole cell can be programmed to realize a particular function. Such a nanocell molecular circuit uses similar molecular switches as the crossbar molecular circuit, but the circuit architecture is quite different. Compared to the crossbar approach, the nanocell approach has the advantages of large-scale circuit fabrication and integration. However, the disadvantage is that it relies on complex programming mechanism. Meanwhile, both the nanocell and crossbar approaches may have the same difficulty in controlling the

metal/molecule interface.

In addition to the metal/molecule/metal switching devices, molecules have also been tested as the channel material in a standard MOSFET structure [70–73]. With the replacement of the high-k dielectric with an ultra-thin SAM of an organic active layer in a field-effect transistor (FET), the researchers from Infineon have reported an organic field-effect transistor (OFET) with low operation and low gate leakage current, the structure of this molecular FET is shown in figure 2.2.

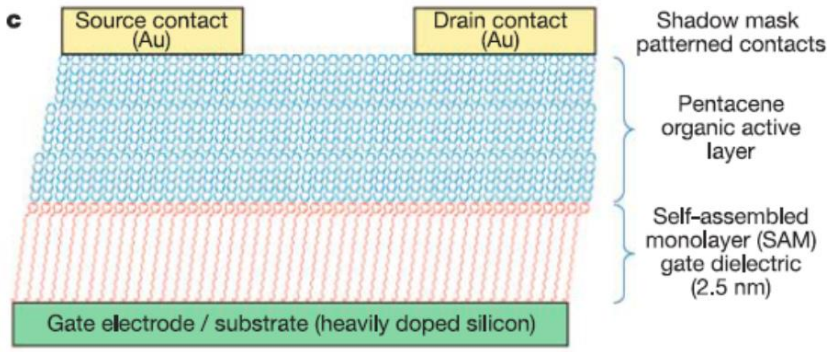

Figure 7 structure of a pentacene organic FET

2.2.2 Non-volatile memory based on redox-active

Appropriate modifications of the molecular structures and switching elements have been designed to change the switching kinetics and to enhance the performance for different memory applications. Different device platforms have been engineered to interface with the molecules, such as dielectrics, oxides, nanowires, carbon nanotubes, and

so forth. A well-known method to achieve a memory effect is by employing redox-active elements. The redox mechanism involves electrons being transferred from one element to another, such that a donor element gives up an electron (oxidation) to an accepting element (reduction). This process usually requires an external stimulus for redox reactions, such as an electric field or change in temperature. Such redox-active molecule-based memory devices can show fast speed, low operation voltage and high reliability, due to the intrinsic redox behavior of the molecules. Therefore, it is very attractive for flash memory device applications.

The research group at North Carolina State University proposed hybrid CMOS/molecular memory devices, in which the redox-active charge-storage molecules were incorporated into Si structures to generate a new class of electronic memory devices [74-78]. These redox-active molecules, which can be designed to self-assemble on surfaces as monolayers, exhibit charge-storage states at discrete voltage levels. This approach can provide a smooth transition from CMOS technology to molecular electronics technology by integrating develop CMOS technology with naturally derived molecular properties, the capacitor structure they developed is shown in figure 2.3 with equivalent circuit.

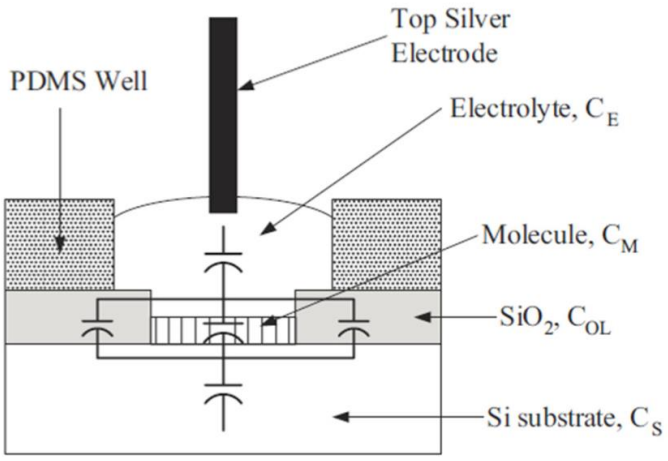

Figure 8 Schematic of electrolyte-molecule -Si capacitor structure and corresponding equivalent circuit.

The capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics also exhibited clear capacitance and conductance peaks associated with charging and discharging in the molecules. Similarly, multiple peaks were observed with the Por-BzOH EMOS capacitor due to its two charged states. Interestingly, the two charged states within molecules, such as Por-BzOH, can be employed for a multi-bit storage application to further enhance the memory density. Despite using a redox molecule exhibiting multiple charged states, an alternative and perhaps more efficient strategy to achieve higher memory bits is afforded by simply mixing different redox-active molecules whose potentials are well separated. Fc-BzOH and Por-BzOH SAMs have been mixed on Si, and the mixed SAMs exhibit well-defined redox states [79]. The mixed SAM approach is very attractive owing to the fact that this approach is synthetically far simpler than preparing a single molecule that exhibits three or more redox states. In addition, the potential of the redox

charged states is more distinct than that of a single molecular redox center with multiple charged states. However, the disadvantage of this method is that the density of a given peak goes down [80]. Nevertheless, this mixed SAM approach still paves the way for constructing multi-bit memory storage devices.

2.2.3 Towards better memory performance

The conventional polysilicon floating-gate flash memory has benefited the semiconductor memory technology for decades, due to its scalability, compatibility with CMOS process, and so forth. It relies on hot electron injection from the channel into the floating gate through a tunneling oxide layer. By attaching redox-active molecules to Si as the floating gate in the CMOS structure, one can further enhance the cell density and reduce the cell variations. The combination of top-down lithography and bottom-up molecule self-assembly processes renders a uniform charge density, and the monodisperse nature of the molecular orbitals leading to distinct energy levels can enable precise controlling of charged states [81].

The self-assembly process of the redox-active molecules to form a solid-state molecular memory enables not only high-quality attachment of molecules to semiconductor surfaces, but also uniform and high-density fabrication of low-cost devices and circuits. The disadvantages of molecular flash memory mainly lie in its reliability in volatile environments. Some redox-active molecules are instable or even do not function at temperatures higher than 200 degree due to evaporation or redox center reaction. Under volatile environments with oxygen or water, the molecule's bond might be broken, leading to poor redox behavior. As a result, some specific conditions and environments need to be

taken into account when integrating such redox molecules in CMOS devices and circuits. Future molecular technology requires advancement in both molecule properties and device integration processes.

The researchers from North Carolina State University reported a study on preventing contact metal penetration into the molecular layer in the metal-insulator-molecule-metal structure [82]. Similar work demonstrating that redox properties of molecules can be preserved after thin film encapsulation, such as atomic layer deposition (ALD), initiated the investigation on high-performance solid-state molecular memory [83]. The Cornell University research group reported a study on a metal-oxide-semiconductor (MOS) structure with molecules encapsulated in a high-k dielectric and functioning as the charge storage medium [84, 85]. molecules with different redox centers, which can show one and two charged states, have been studied for multi-bit memory. With the electrostatics determined by the alignment between the highest occupied or the lowest unoccupied molecular orbital (HOMO or LUMO, respectively) energy levels and the charge neutrality level of the dielectric, the asymmetric charge injection behavior in flat-band voltage shift (DVFB) vs. programming voltage measurement is due to the Fermi-level pinning between the molecules and the high-k dielectric [86-88]. The three programmable molecular orbital states of the 5-(4-Carboxyphenyl)-10,15,20,-triphenyl-porphyrin-Co(II) (CoP) molecule have been experimentally observed and are attractive for low-variation multi-bit memory applications. The engineering by the same group on the tunnel layer has greatly enhanced the electron retention and programming performance by forming an organic-inorganic tunnel barrier [85].

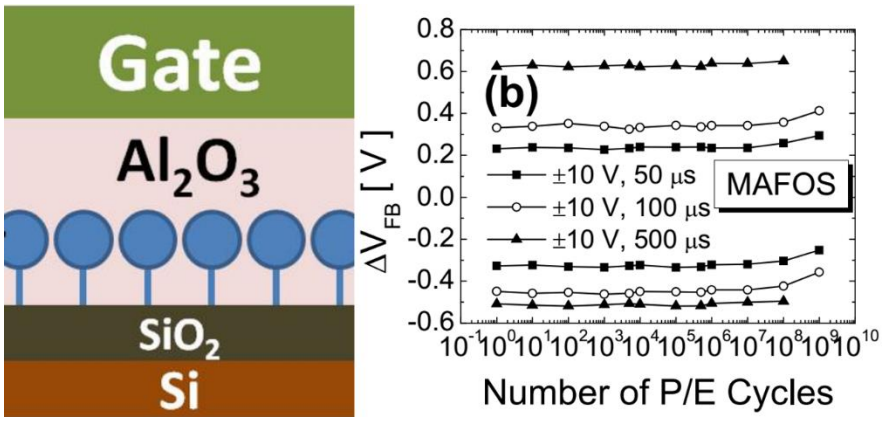

Figure 9 Schematic of α-ferrocenylethanol molecular memory structure and the excellent endurance property

Recently, the NIST researchers have reported a similar capacitor-structure molecular non-volatile memory, but with enhanced charge retention and excellent endurance [89]. The molecular memory uses an α-ferrocenylethanol redox molecule, which has a very simple structure and one redox center. With the molecules attached to the SiO_2 tunnel oxide and encapsulated in the ALD Al_2O_3 dielectric, the solid-state molecular memory exhibited excellent memory behavior, such as a sufficient memory window, good retention and endurance. Even though only ~15% of the molecules were effectively involved in the redox processes after ALD, effective memory can be realized

with sufficient charge density. These characteristics are attributed to the intrinsic redox behavior of the ferrocene molecule and the effective protection from the presence of the gate dielectric covering the molecule SAM. The molecular memory showed excellent endurance properties, with negligible memory window degradation after 10^9 P/E cycles, which is about 10,000 times better than that of the conventional floating gate memory (1

$\times 10^5$ P/E cycles), the schematic structure of their capacitor memory structure and great endurance characteristics are shown in figure 2.4. However, the operation voltage of such molecular memory is still high, and the operation speed needs to be improved. Further study of the molecular memory depends on the engineering of redox-active molecules, such as molecules with multiple redox centers and a proper linker for multi-bit memory, and the device structure engineering to optimize the dielectric stack thickness and improve the molecule/dielectric interface. Such an exploration will be a significant breakthrough in the quest for charge-storage non-volatile memory and will enable the application of flash-like devices for future on-chip memory applications.

2.3 Fabrication of Si based redox-active molecular flash memory

The capacitor structure flash memory cells were fabricated by applying standard photolithography and film deposition procedures. Dielectric stacks parameters including the tunneling oxide, redox-molecular charge storage layer, and blocking oxide were employed and optimized. The attachment of redox-active molecules on Si/SiO_2 surfaces was fulfilled by self-assembled monolayers (SAMs) on Si/SiO_2 surfaces. The connection between SAMs and Si/SiO_2 surfaces is covalent bond through AUS linkage material. The process procedures are as the following list:

(1) Stand RCA clean process is employed on Si wafer prior to fabrication process

(2) A 290 nm SiO_2 film is thermally grown on low-doped p-type (100) Si wafer substrates (~10^{16} cm^{-3} Boron doped) by dry oxidation in CMOS oxidation furnace.

(3) Arrays of squares with different active area ranging from 100 to 10000 μm^2 are

defined on the wafer by photolithography with Suss MA-6 and/or MA-8 aligner.

(4) Buffered oxide etch (BOE) solution and 2 % hydrofluoric (HF) acid are used for the removing of oxide defined by lithography process to get the arrays of experimental window areas in the 290 nm thermal SiO_2.

(5) The tunneling oxide (thin SiO_2) is grow by rapid thermal oxidation (RTO) instantly after step (4), different oxide thickness can be defined by adjusting the temperature and RTO process time.

(6) The redox molecules solution is prepared by dissolving the molecules in designated solvent. Dichloromethane and toluene are used to dissolve redox molecules for attachment process in this work.

(7) The molecular film is realized by self-assembling process on window areas by 'click' chemical reaction. First, AUS linkage material is attached by immersing the substrate into AUS solution with 95 ℃ hotplate for 2-3 hours with a loose cover. The liquid evaporation helps the attachment process. After that, mix the Ru molecule solution and other proper solution which helps the attachment process evenly and drop them into Sodium L-ascorbate solution slow and evenly, then immerse the AUS covered substrate into the container covered with loose lid. The Ru molecule will be attached on substrate after several hours in room temperature. The attachment process is conducted in a glovebox with N_2 environment. The attachment conditions are same for both attachment on Si and SiO_2 surfaces. Figure 2.5 shown the illustration of molecule attachment process.

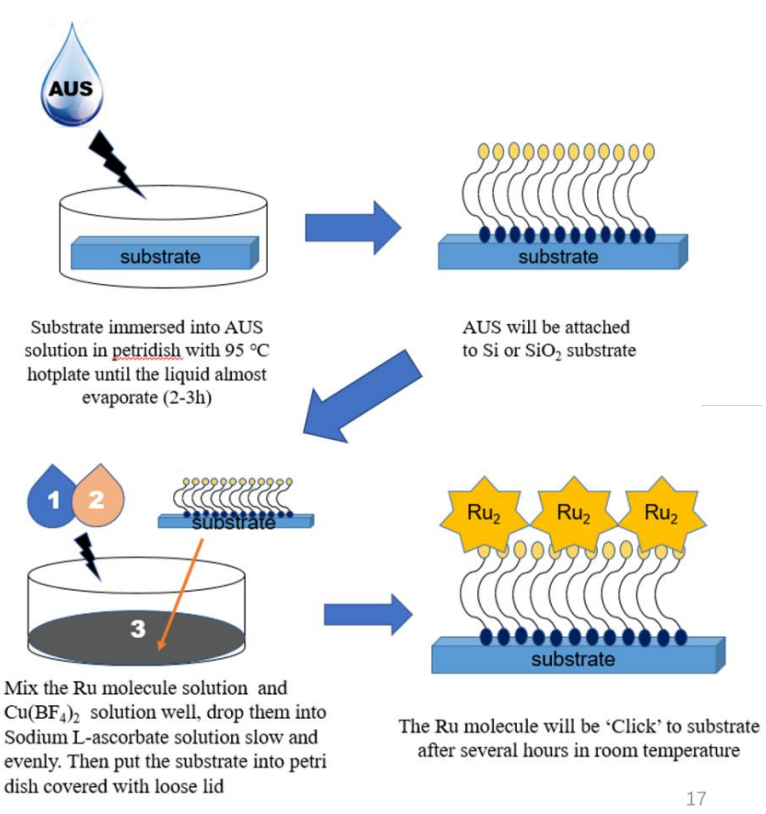

Figure 10 Illustration of molecule attachment process

(8) After the molecular film was formed, two cycles of 5 min sonication clean was applied to rinse the attached sample for removing physisorbed residuals on the surface with DCM solvent.

(9) The attached samples were separated into two groups: one group for attachment characterization like X-ray photoelectron spectroscopy (XPS) and Atomic Force Microscope (AFM); the other group is for molecular memory device fabrications. This group of samples will immediately load into the Atomic Layer Deposition (ALD) vacuum chamber right after the sonication clean for blocking oxide Al_2O_3. The ALD operation

temperature is set to 100 ℃ in case of the instability of organic molecule, with H_2O and TMA as precursors.

(10) As the final step, Pd was deposited and patterned on the top of the devices as the top gate by photolithography and E-beam evaporation, followed by the lift-off process.

The samples for XPS and AFM are prepared by doing molecule attachment on highly doped p-type Si substrate without patterned structure, but the attaching recipe and process is same as the previous described methods.

Attachment of target molecules and successfully encapsulated by ALD deposition Al_2O_3 is the key point of the redox molecular memory fabrication process. The molecular film was characterized by CyV, XPS and AFM measurements. Somme samples after deposition a thin layer of ALD Al_2O_3 are measured by XPS, and the results demonstrated the molecule survived in the low temperature ALD process. The capacitor memory device fabrication is illustrating in Figure 2.6.

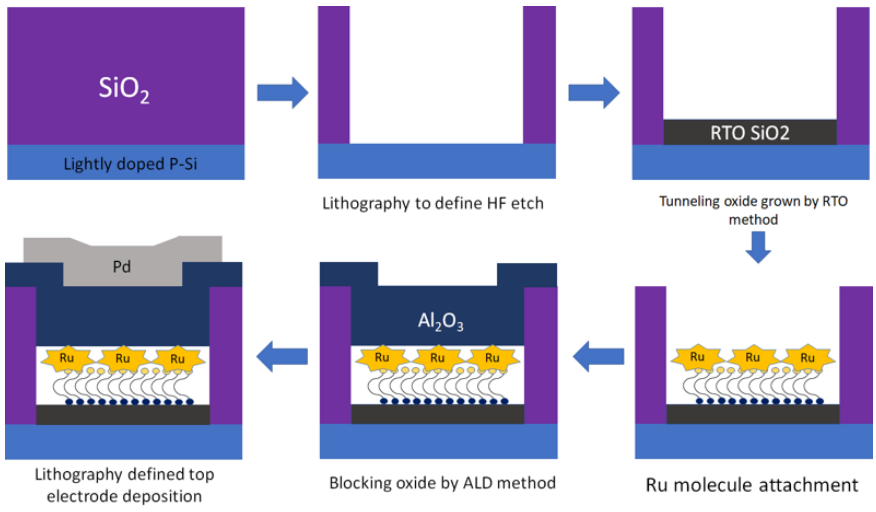

Figure 11 Capacitor memory device fabrication flow

2.4 Fabrication of 2-D material based molecular memory

The attachment of redox-active molecules on 2-D materials is carried out by the replace the Sulfur atom or fill the Sulfur vacancy with thiol moiety on monolayer MoS_2 surface. The connection between molecule and MoS_2 is covalent bond. Figure 2.7 exhibits the illustration of replacement or fill process [90]. The characterization of molecule attachment on 2-D materials done by using XPS measurement, prior to the memory cell fabrication process, the processing steps are as follows:

(1) Stand RCA clean process is employed on Si wafer prior to fabrication process

(2) A 290 nm SiO_2 film is thermally grown on moderate-doped n-type (100) Si wafer substrates (~10^{17} cm^{-3} phosphorous doped) by dry oxidation in CMOS oxidation furnace. The 290nm SiO_2 is used for identifying the color of different layer number of MoS_2 under

optical microscopy.

(3) Monolayer MoS_2 flakes is prepared by Au-mediated mechanical exfoliation method and then transfer to SiO_2 substrate. (the method will be discussed in chapter 5)

(4) Monolayer MoS_2 is patterned photolithography method and then etched by Reactive-ion etching (RIE) in SF_6 plasma

(5) The drain and source electrode are deposited and patterned on MoS_2 by photolithography and E-beam evaporation, followed by the lift-off.

(6) The redox molecules solution is prepared by dissolving the molecules in toluene solvent. The attachment process of molecules on MoS_2 surface is realized by immersing the substrate in to molecular solution (0.1mMol) for several hours with 70 ℃ hotplate. The attachment process is performed in glovebox with N_2 environment.

(7) After the molecular film was formed, two cycles of 2 min sonication clean was applied to rinse the attached sample for removing physisorbed residuals on the surface with toluene solvent.

(8) The molecular attached samples will immediately load into the Atomic Layer Deposition (ALD) vacuum chamber right after the sonication clean for blocking oxide Al_2O_3. The ALD operation temperature is set to 100 ℃ in case of the instability of organic molecule, with H_2O and TMA as precursors.

(9) Finally, Pt is deposited and patterned on the top of the devices as the top gate by photolithography and E-beam evaporation, followed by the lift-off process.

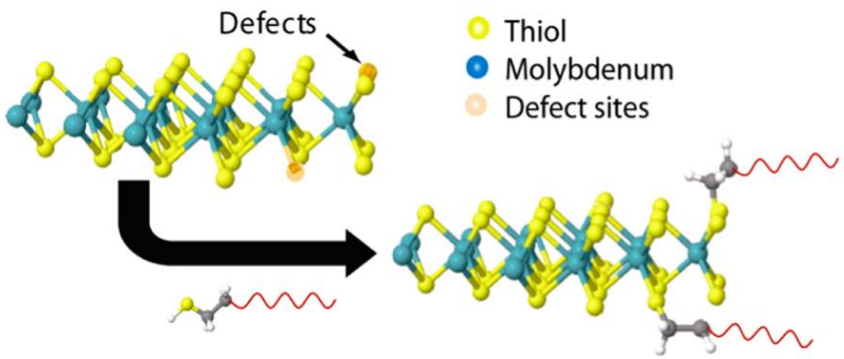

Figure 12 Illustration of attachment process on MoS_2[90]

The samples for XPS measurements are prepared by attach the redox molecule to large area MoS_2 sample deposited by Chemical vapor deposition (CVD) method. The attaching method and recipe is same with method described above.

2.4 Physical and electrical characterization

To confirm the molecule attachment process, XPS measurements were done by using a Kratos Axis Ultra instrument equipped with monochromatized Al Kα photons. We can demonstrate the molecule attachment by detecting specific element peaks, the coverage of molecule film could also be roughly estimated by the XPS measurement result. AFM images were obtained using Bruker Dimension FastScan in semi-contact mode to investigate the sample surface morphology. The surface roughness is greatly decided by the molecular size and hardness.

To study the memory device characteristics, electrical characteristics were measured in a dark environment with a commercial probe station. Bias was applied between the metal

gate and the silicon substrate during all the electrical measurements.

The memory performance of the capacitor structure molecular memory devices can be investigated by the measuring of the flat-band voltage curve under different bias sweeping conditions. A series of capacitance-voltage measurement at various frequencies were applied by using Agilent E4980A LCR meter to determine the retention attribute. Pulse response sensitivity measurements were implemented with an Agilent 4156 Semiconductor Parameter Analyzer. A Hewlett Packard 33120A waveform generator was applied to measure the Program/Erase endurance by produce designated voltage pulses.

Cyclic voltammetry (CV) measurements were performed using a Solartron Modulab potentiostat to verify the memory application potential of molecule. The electrolyte was 0.1 mol/L tetrabutylammonium hexafluorophosphate in anhydrous acetonitrile and was deoxygenated with dry N_2 prior to use. A three-electrode cell configuration was used with the Ru molecule clicked onto native oxide/Si as the working (area = 0.32 cm^2). The cell is completed with a platinum wire counter electrode, and a silver quasi-reference (AgQRE) electrode. The sweep rate was 10 mV/s.

Chapter 3 Redox-active Molecular Memory Based on Si

3.1 Introduction

The CMOS scaling according the Moore's law to realize faster central processing unit (CPU) is reaching the fundamental and physical limits induced by large heat production and short-channel effect as the technology node down to several times of atomic size. However, the scaling of semiconductor flash memory is far behind CPU device scaling. The EOT of the gate stack in semiconductor flash memory is still more than 10 nm while the EOT of CMOSFET with an equivalent EOT at 0.8 nm in 2001 [91]. The work hour of mobile devices and memory cell size scaling could be significantly increase if the scale of EOT of memory gate stack. Many materials have been proposed for improve this property.

Molecular electronics technology is getting more and more attention since 1970s due to the inherent scalability and intrinsic properties of molecule [92-93]. Molecular memory devices are considered as promising emerging memory candidates due to the potential for further cell scaling and improvement of reliability [94]. In a redox-active molecular flash memory cell, the redox-active molecules have distinct oxidation and reduction states accessible at different supplied voltage, which enables stable binary or multiple states for charge storage like that of traditional charge trapping materials [95]. Compared to polysilicon and Si_3N_4 charge trapping layer, redox-active molecule has the advantage of intrinsic molecular scalability at the nanoscale, multiple bits and tunable electronic

properties to achieve ultrahigh storage density. In addition, redox molecules can be tuned to attach onto different kinds of semiconductor materials [96] and form self-assembled few-layer or monolayer structures with low-cost processes, usually a solution-based process, which provides a great advantage for promising commercial memory application in the future.

The excellent retention property of the redox-active molecules based on Si structure has been demonstrated with enduring more than 10^{12} program/erase (P/E) cycles [97]. The excellent performance in reliability is naturally derived from the intrinsic reduction and oxidation states stability of redox molecule materials. Redox-active molecular memory devices usually fabricated by forming a self-assembled monolayer (SAM) or multi-layer film on various kinds of material surfaces. This process, known as attachment, is very cheap and simple achieved. Besides advantage of cheap cost fabrication process, molecular memory can work with few electrons at the molecular level, which stand for the potential for extremely low pow consumption and ultrahigh storage density. To commercialize a real molecular electronic product consist of understanding multiple comprehensive mechanism of the electrical of molecule materials both in macroscopic scales and atomic scales, interface morphologies and precise atomic level manipulation. Great efforts have been devoted on improving memory storage density, multibit data storage and the P/E speed improvement of molecular memories based on organic molecules, electrets, conjugated polymers and ferroelectric molecule materials [98-107]

For redox-active molecular memory devices, applying an oxidation voltage will cause the electron loss in redox molecules; on the other hand, electrons will be driven back to

molecules under a reduction voltage bias, typically this process is very fast and lead to a very fast P/E operation speed. In addition, the intrinsic scalability of molecular level and nature-derived valence states for stable charge storage states make the redox molecule very attractive for high density, long-retention non-volatile data storage applications. [97,104,108]

Another attractive advantage of molecular electronics is due to some redox-active molecules are compatible with present CMOS integration process. In this chapter, we present our work on characterization and optimization of redox-active molecules attached on Si/SiO_2 surfaces, and experimentally judge the memory performance of Ru redox molecular non-volatile memory. The results demonstrate the molecular flash memory is promising for low power consumption, high reliability and high density memory application due to their good retention and fast P/E speed at low P/E voltages. A distinguished charge storage efficiency was exhibited with 5.2 V memory window shown under $\pm$ 9 V sweeping gate voltage. The degradation anticipation estimated by the measured data indicated that 72% of the initial memory window will remain after 10 years.

3.2 Experimental details

In our work, we have developed and optimized a Si based molecular integration method to exploit the intrinsic redox properties and investigate the memory performance by measuring capacitor structure molecular memory. the memory devices based on Ru molecules exhibit nonvolatile flash like behaviors. The capacitor structure memory device exhibits a very large memory window of 5.2 V, fast response at a 10^{-5} s short P/E pulse, a

long retention time estimated as at least 10 years, and negligible degradation after P/E cycles up to 10^5. These properties are superior to other demonstrated molecular memory works [109, 110].

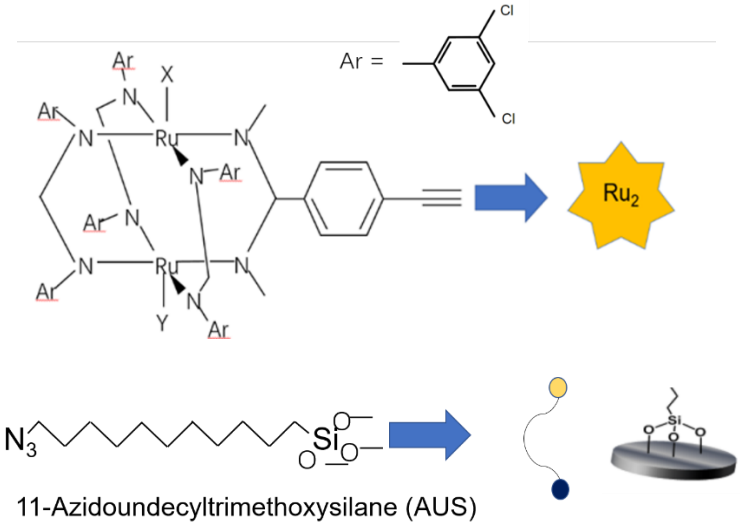

Figure 13 The molecule structure of Redox-active Ru molecule and the aliphatic AUS

we have fabricated memory cells with a metal-Al_2O_3-Ru_2-SiO_2-Silicon (MAROS) structure with a Ru molecule SAM on SiO_2. Figure 3.1 shows the structure of the synthesized Ru redox molecule with the chemical formula: $C_{50}H_{32}N_8Cl_{13}Ru_2$ and the linkage molecule 11-Azidoundecyltrimethoxysilane (AUS). The connection between each part is covalent bond.

The metal-oxide-semiconductor (MOS) capacitor structure, applied in our Flash-based memory devices was fabricated and used for the attachment of the redox-active Ru

molecules as the charge storage layer which is the most important fabrication procedure. The Ru_2 molecule is attached onto the device substrates by 'click' chemistry with a linker molecule which has been reported by Pookpanratana et al. [111].

Firstly, stand RCA clean process is employed on Si wafer prior to fabrication process. A 290 nm SiO_2 film is thermally grown on low-doped p-type (100) Si wafer substrates (~10^{16} cm^{-3} Boron doped) by dry oxidation in CMOS oxidation furnace followed by the definition of square shaped active window areas (100 μm × 100 μm) by photolithography and wet etch process.

The tunneling oxide (~2 nm) is grow by rapid thermal oxidation (RTO) instantly at 840 ℃ for 2 min 30s.

Synthesis work of the Ru redox molecules is performed by our collaborator Prof. Tong Ren. The Ru redox molecules solution is prepared by dissolving the molecules in dichloromethane (DCM) solvent. The molecular film is realized by self-assembling process on window areas by 'click' chemical reaction. AUS linkage material is first attached by immersing the substrate into AUS solution with 95 ℃ hotplate for 2-3 hours with a loose cover. The liquid evaporation helps the attachment process. After that, mix the Ru molecule solution (0.1 mmol/L) and other proper solution which helps the attachment process evenly and drop them into Sodium L-ascorbate solution slow and evenly, then immerse the AUS covered substrate into the container covered with loose lid. The Ru molecule will be attached on substrate after several hours in room temperature. All attachment operation is conducted in a glovebox with N_2 environment. After the molecular film was formed, sonication clean was applied to rinse the attached sample for removing physisorbed

residuals on the surface with DCM and IPA solvent.

The attached samples were separated into two groups: one group for attachment characterization like X-ray photoelectron spectroscopy (XPS) and Atomic Force Microscope (AFM); the other group is for molecular memory device fabrications. This group of samples will immediately load into the Atomic Layer Deposition (ALD) vacuum chamber right after the sonication clean for blocking oxide Al_2O_3. The ALD operation temperature is set to 100 ℃ in case of the instability of organic molecule, with H_2O and TMA as precursors.

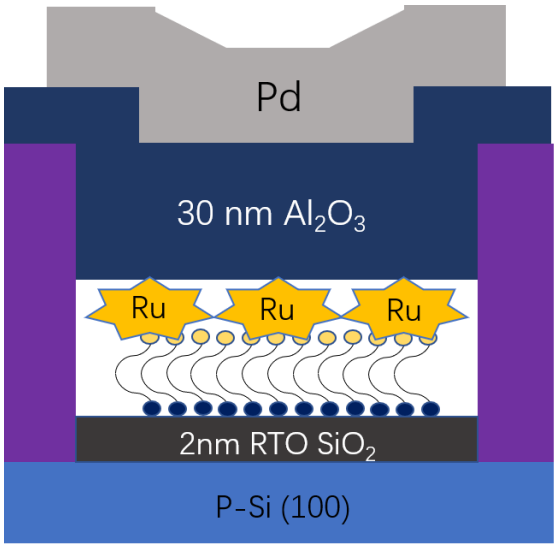

Figure 14 Schematic of the MAROS capacitor structure

As the final step, a layer of 105 nm Pd was deposited and patterned on the top of the devices as the top gate by photolithography and E-beam evaporation, followed by the lift-

off process. The schematic of MAROS capacitor structure is displayed in Figure 3.2. To make sure the origin of memory effect of capacitor redox molecular memory. We also fabricated two control sample structures for comparison, one of them is no molecule on tunneling oxide, the other is only with AUS linkage molecule.

3.3 Physical and electrical measurement for molecule attachment

In order to investigate the quality and density of molecule attachment, we applied Cyclic voltammetry (CyV) measurement to some after-attach device substrates. Cyclic voltammetry (CV) measurements were performed using a Solartron Modulab potentiostat to verify the memory application potential of molecule. The electrolyte was 0.1 mol/L tetrabutylammonium hexafluorophosphate in anhydrous acetonitrile and was deoxygenated with dry N_2 prior to use. A three-electrode cell configuration was used with the Ru_2 molecule clicked onto native oxide/Si as the working (area = 0.32 cm). The cell is completed with a platinum wire counter electrode, and a silver quasi-reference (AgQRE) electrode. Figure 3.3 shows the CyV data of the electrolyte-molecule-oxide-Si (EMOS) structure with Ru molecular SAM on substrate at 10 mV/s sweep rate. The peaks at negative gate voltage (VG) are for oxidation process and the peaks at positive VG are for reduction process, respectively. While the oxidation (or reduction) voltage is applied, the electrons are lost from (or driven back to) the molecular layer. The CyV measurements of the attached Ru molecule on SiO_2/Si substrates (as the working electrode) demonstrate that the Ru molecule is electrochemically active. Upon sweeping the potential between 0V and 1.0V (with respect to the AgQRE), a reduction-oxidation (redox) pair is observed after

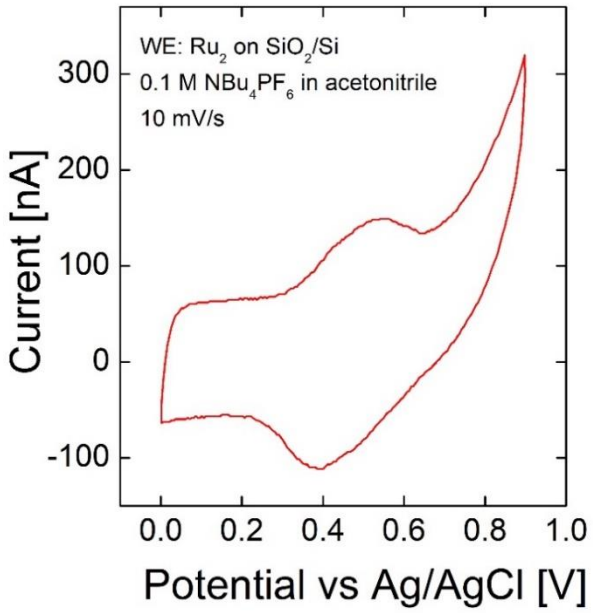

Figure 15 CyV of the EMOS capaciptor at 10mV/s sweep rate.

multiple cycles. The cathodic peak center is about 0.5V, while the anodic peak center is about 0.39 V. When compared to the same Ru molecule in solution, this redox feature is consistent with the reversible oxidation of the diruthenium core going from Ru_2(III, II) to Ru_2(III, III). Therefore, the Ru2 molecules are robustly integrated to the SiO2/Si substrate and they are still electrochemically active, which is promising for solid state molecular memory applications. The surface coverage density of Ru molecule can be roughly estimated form the oxidation peak line [112], the value is calculated to be 2×10^{12} cm^{-2} on SiO_2 surface.

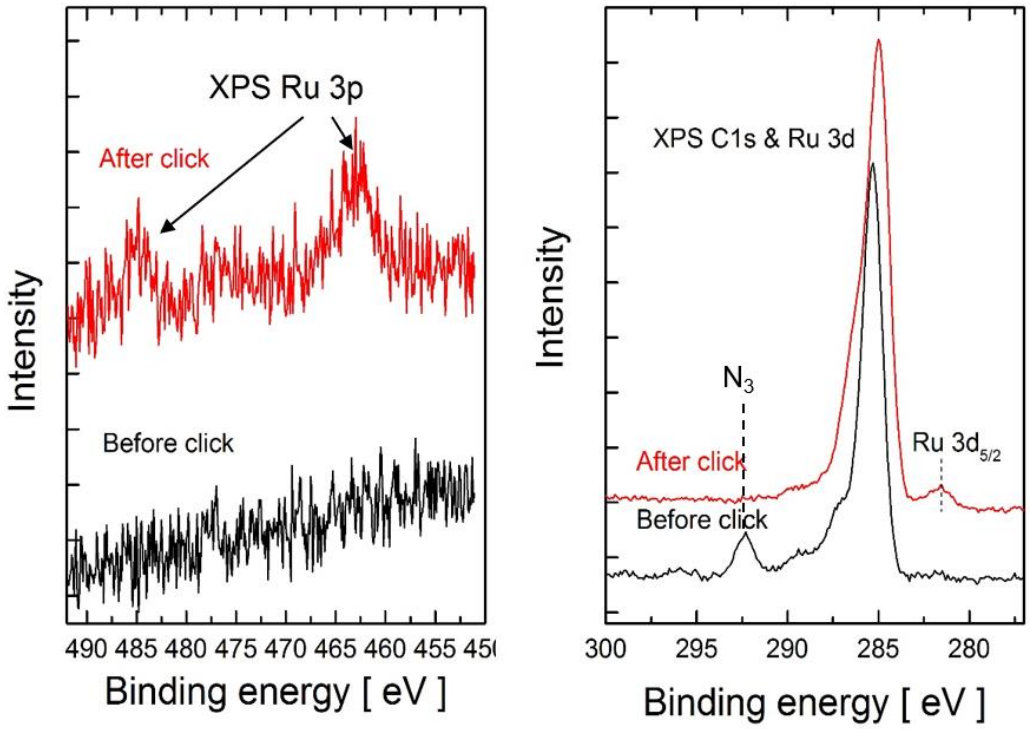

Figure 16 XPS measurement of (left) samples with Ru molecule attached on SiO_2 surface, and(right) sample before "click" reaction.

To directly confirm the chemical attachment information of the Ru_2 molecular SAM, XPS measurement were applied to the samples with Ru_2-containing sample and the AUS linker Figure 3.4 presents the XPS spectra gathered from the Ru_2-containing sample ("after click") and the AUS linker ("before click"). Ru $3d_{5/2}$ and Ru 3p peaks can be detected in the spectra of the Ru_2 SAM sample in contrast to the AUS linker surface, peak for N_3 moieties in AUS linkage cannot be find after "click" due to click reaction open the N_3 ring and form covalent bond with Ru molecule, which indicates that the Ru_2 molecule has been

attached on the SiO_2 surface successfully. The coverage density of Ru molecules on the SiO_2/Si substrate is estimated as 0.3 molecule per nm^2 by the calculation of the Ru 3d and Si 2p XPS spectral lines with Si substrate as the reference [113].

The surfaces morphology was investigated by AFM in semi-contact mode. The AFM image of bare Si substrate (left), Si substrate with azidoundecyltrimethoxysilane (AUS) linkage molecule (middle) and Ru_2 molecular SAM on Si substrate (right) are shown in Figure 3.5. The data revealed relatively smooth film surfaces and homogeneous monolayers. The root-mean-square (rms) roughness, R_{rms} increased after the molecule attachment process. The R_{rms} of the bare substrate, AUS layer, and the final diruthenium layer for a 1μm × 1μm scan area were found to be ≈0.16nm, 0.31nm and 0.64nm, respectively.

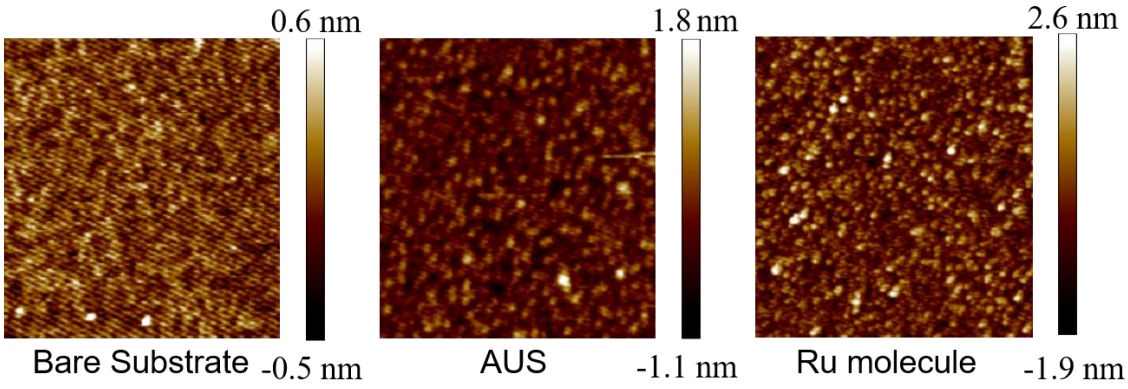

Figure 17 AFM image of (left)Bare Si, (middle)substrate with AUS and (right)Ru molecular SAM on Substrate

3.4 Molecular memory characterization

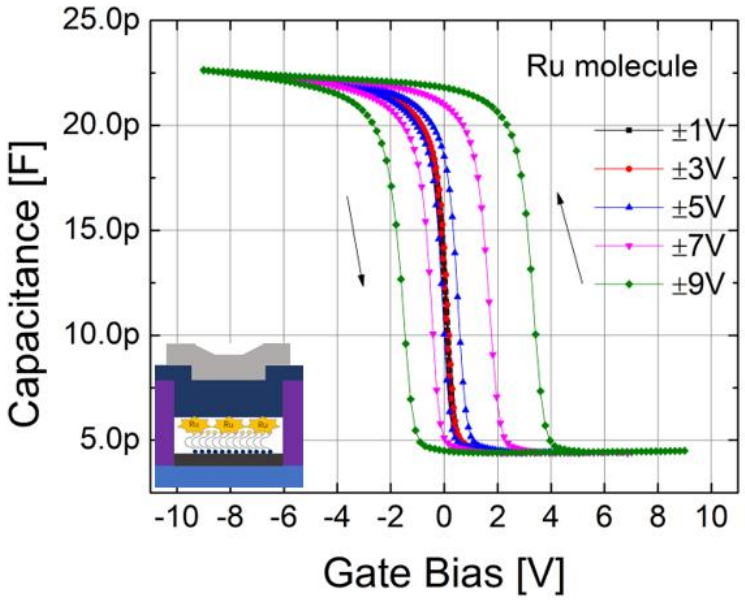

Figure 18 C-V measurements of memory devices with Ru attached structure

In memory operations, electrical bias should be applied to the gate electrode and thus induce the movement of charges between the semiconductor substrate and charge storage layer. Memory window in capacitor structure memory can be defined as the change of flat band voltage between forward and backward voltage sweeping. The memory window performance of the Ru_2 molecular memory devices and control samples is characterized by capacitance-voltage (C-V) hysteresis at 1 MHz, with multiple voltage sweeping range. As the result shown in Figure 3.6, the Ru_2 molecular memory window can be defined as the shift of the flat-band voltage ($\triangle V_{FB}$) from oxidation states to reduction states is about 5.2 V at an applied sweeping gate voltage between 9 V and -9 V at 1.0 MHz. The hysteresis

loop in C-V measurement is due to the charge stored in the Ru_2 molecule SAM: electrons tunnel out of the molecules to Si at negative V_G (oxidation) and tunnel back into the molecules at positive V_G (reduction). The density of the trapped charges per unit area (N_t) can be roughly estimated by using the following formula:

$$N_t = C_{ox}\Delta V_{FB}/qA,$$

where C_{ox} represents the capacitance at the accumulation region, $\triangle V_{FB}$ of the shift in the flat-band voltage, A of the effective device area, and q of the elementary charge. The density of the trapped charges in Ru_2 molecular memory devices at a sweeping voltage with ± 9 V, 1 MHz is calculated as 7.3×10^{12} cm^{-2}, which means about 0.25 electron could be stored in every Ru molecule.

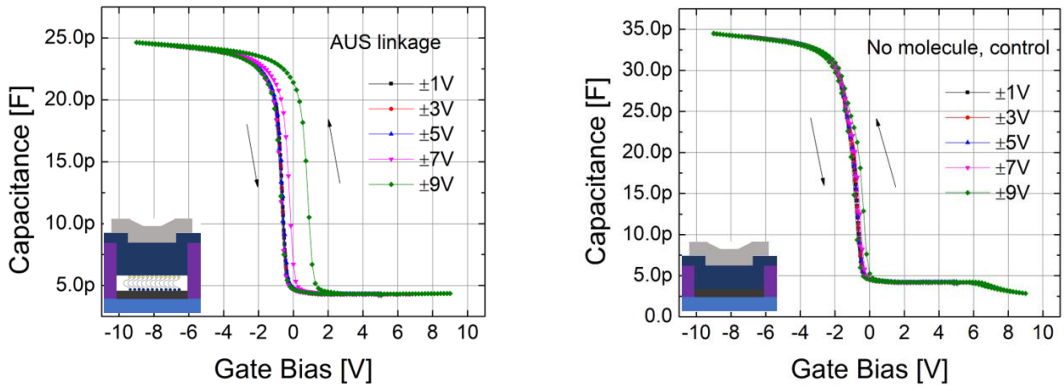

Figure 19 C-V measurements of memory devices with (left) only AUS linkage and (right) with no molecule

For comparison, the sample with AUS linkage molecule but no Ru_2 molecules has a much smaller program $\triangle V_{FB}$ and almost no erase $\triangle V_{FB}$ and the sample with no molecule showed even smaller $\triangle V_{FB}$ (Figure 3.7). We define positive (or negative) $\triangle V_{FB}$ with positive (or negative) V_G as programming (or erasing) operation, corresponding to electron get (or loss) in Ru_2 molecule, corresponding to reduction (or oxidation) of the molecules, respectively. The interface next to Al_2O_3 usually have some trap states and thus lead to charge storage, inducing a small $\triangle V_{FB}$ also. As the result shown in Figure 3.8, the $\triangle V_{FB}$ of the samples without molecule is smaller than that of Ru_2 molecular samples after the same voltage pulse, indicating that the electron storage effect is mainly from the Ru_2 molecules. The hole injection starts to show observable $\triangle V_{FB}$ at lower than -8 V gate voltage, while the ≈ 6 V gate voltage is required for electron injection to show a clear $\triangle V_{FB}$. This slight difference of $\triangle V_{FB}$ at low gate voltage is partially due to the more preferred of electron storage than electron at the Ru/Al_2O_3 interface, which will be discussed in following paragraph. While increases P/E voltage bias, the ferrocene molecular memory shows larger $\triangle V_{FB}$, indicating the charges are injected and mainly stored in the redox centers of Ru molecule.

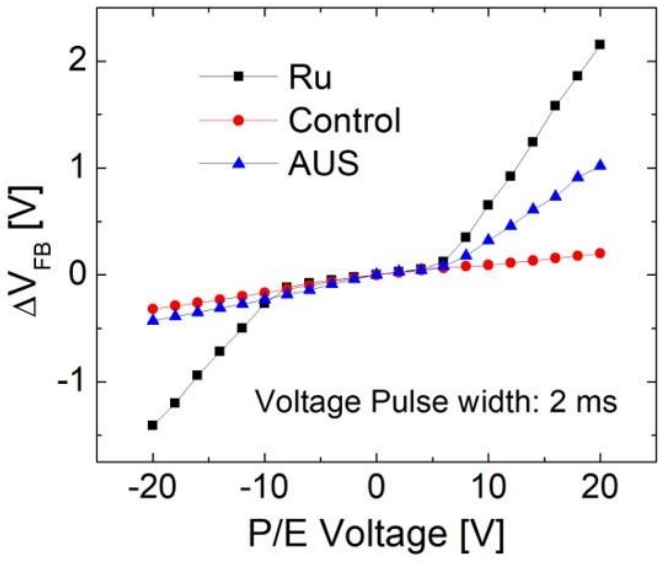

Figure 20 $\triangle V_{FB}$ of these 3 structures as a function of P/E voltage with pulse width= 2ms

Figure 3.9 exhibits the P/E speed characteristics of Ru molecular memory devices. Pulses of ±10V with different widths were applied to determine the response speed of the P/E operations. Ru molecule memory device shows a fast switch speed in both programing and erasing actions. From the high-frequency (1 MHz) C-V curves in figure 15, even with a pulse width as small as 10^{-5} s, Ru memory devices still have a response and show $\triangle V_{FB}$ at 0.15V (program) and 0.09V (erase), respectively. We notice that the distribution of $\triangle V_{FB}$ during the erase operation is relatively less compared to $\triangle V_{FB}$ under the same voltage amplitude program operation. And this suggests that the programming response is faster than erasing response in our Ru_2 molecule memory devices although the difference is not big in this Ru_2 molecular memory. This response different phenomena could be due to the difference in the density of traps for electrons and holes within the storage layer and the

relative energetic positions of the molecular orbitals with respect to the band edges of the inorganic layers. Figure 3.10 shows the band diagram alignment of the Ru molecular memory structure. The highest occupied molecular orbital (HOMO)/ lowest unoccupied molecular orbital (LUMO) for Ru molecule are measured by Prof. Tong Ren [114], the provider of molecule. The levels of HOMO and LOMO is -5.83 eV and -4.48 eV, respectively. The charge neutrality level (CNL) of Al_2O_3 deposited by ALD method is at -5.2 eV, which can be roughly considered as a local Fermi level of the interface states. For electron injection, the extra energy for electrons to get injected into ferrocene LUMO is $E_{LUMO} - E_C$ = -0.33 eV, where E_C is the level of Si conduction band bottom. The injected electrons will be relaxed into interface states surrounding the CNL due to the lower energy level. At the same time, the extra energy for holes to be injected into ferrocene HOMO is $E_V - E_{HOMO}$ = 0.55 eV, where is the level of Si valance band top. Therefore, electron injection is preferable than hole injection.

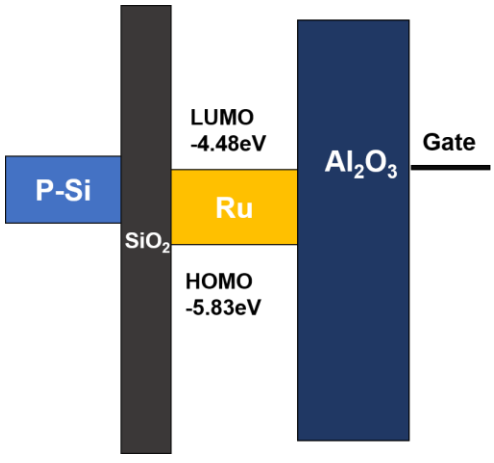

Figure 21 Schematic band diagram of Ru molecular memory structure

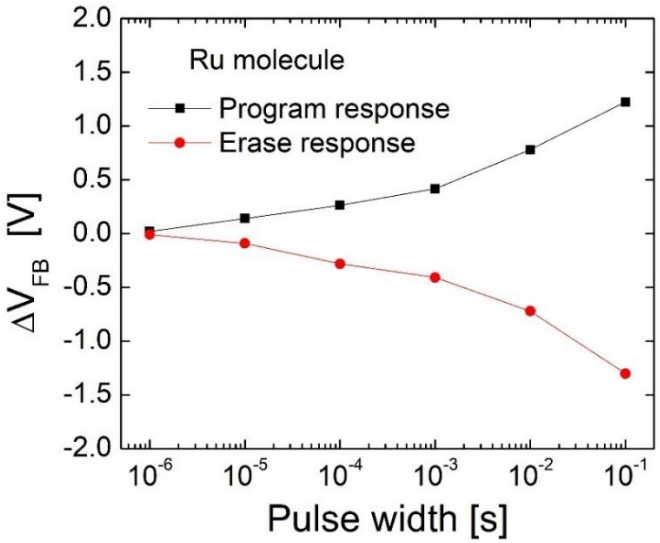

Figure 22 Response speed characteristic of Ru molecular memory device.

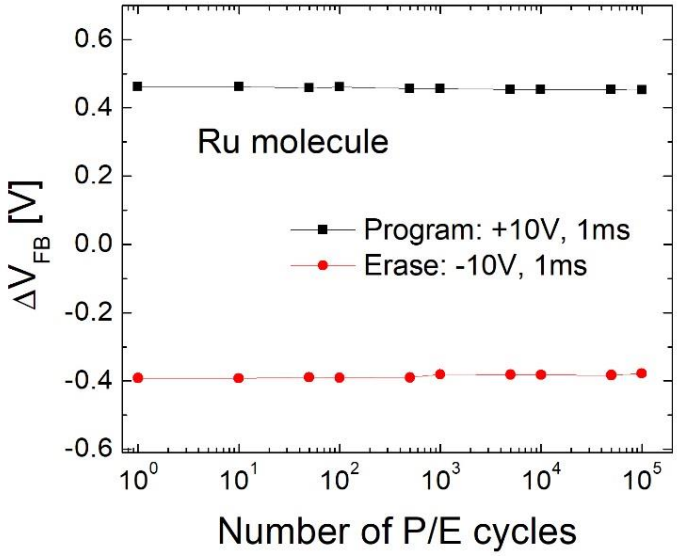

Figure 23 Endurance characteristics of Ru molecular memory devices under P/E pulse at V_G= ±10 V with 1 ms pulse width

Figure 3.11 displays the endurance characteristics of Ru molecule memory devices, a Program/Erase voltage of ±10 V with 1ms width at room temperature was applied to top gate. Change of V_{FB} after 10, 100,1000, 10000 and 100000 P/E cycles are record. The degradation of $\triangle V_{FB}$ is only about 8% when compare with the initial value 0.45 V (programing $\triangle V_{FB}$) and 0.37V (erasing $\triangle V_{FB}$) after 100,000 cycles. This memory sample will not fail after even a large number of erase and rewrite cycles indicating high reliability and stable switching endurance property [115]. The excellent endurance characteristic shows that the device fabrication procedures protect the Ru molecule very well.

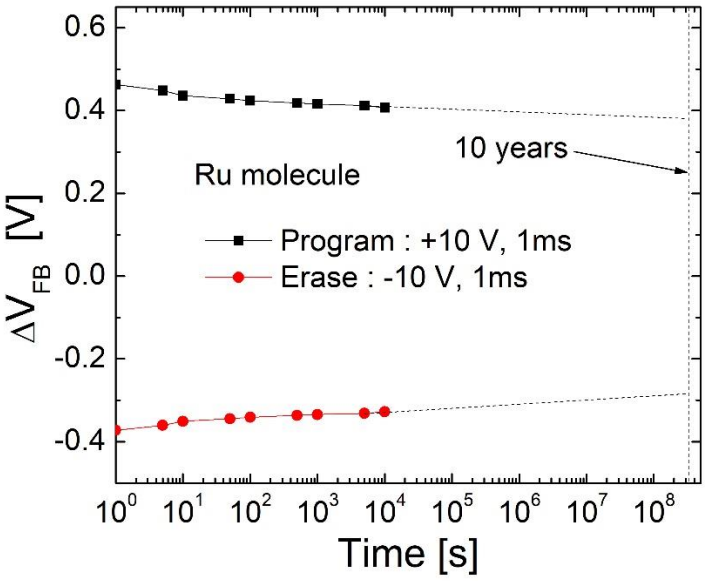

Figure 24 Retention Characteristic of Ru molecular memory at room temperature

The electrons loss from the charge storage layer typically means the likelihood of failure in information storage. To determine if the memory devices are suitable for long term data storage, retention performance is a very important standard. As the final part of the memory device characteristics, the retention property of Ru_2 molecular memory was investigated at room temperature by applying the gate voltage of ±10 V for 1 ms as the initials program/erase state respectively, shown in Figure 3.12. It showed 0.05 V (program) and 0.04 V (erase) $\triangle V_{FB}$ shrinks after 10^4s compared to its initial value. By extrapolating the data with the tendency line both on the program state and erase state, we can anticipate the remnant memory window after 10 years will be about 72% of the initial V_{FB} shift which proves that the charge loss from Ru_2 molecular SAM is competent for nonvolatile memory industry. The good retention property is mainly due to the AUS linkage molecule and good quality tunneling layer SiO_2 [111]. The obtained retention property appears encouraging, considering that this Ru_2 molecular memory structure is only the prototype of the kinds of Ru molecule series. With the methods of a thorough engineering of each part and modifying the ligands of molecules, great improvement can be anticipated. Retention characteristic can be related to many factors such as the nature of tunneling barrier and the charge trap property. We can propose that both the intrinsic property of Ru_2 molecules and the intercalated AUS layer between the tunneling SiO_2 and Ru_2 molecular SAM contributes contribute to the charge retention. The AUS layer can be considered as a spatial insulator barrier and its relative permittivity was estimated to 3 from previous report [110], which helps prevent the charge tunneling back to Si. At the same time, the AUS layer likely creates

an extra obstacle barrier for the charges switching between the Ru_2 molecules and the Si substrate which leads a relatively slow Program/Erase speed.

3.5 Summary

In summary, we have fabricated redox molecular capacitor structure based on Si with Ru molecule film which is sandwiched by the blocking oxide and tunneling oxide for non-volatile memory application. The molecular attachment process on Si has been developed and optimize with the demonstration by XPS, AFM and Cyv measurement. The memory devices based on diruthenium molecules exhibit nonvolatile flash like behaviors and exhibit very good program and erase characteristics comparing with conventional flash memory. Due to the high surface coverage of charge-storage Ru_2 molecule on SiO_2, great number of charges can be stored in this Ru molecular monolayer, leading to a large memory window in high frequency C-V measurements at 5.2 V with -9 V to +9 V sweeping range. The endurance of MAROS structure devices can endure at least 10^5 P/E cycles with negligible memory window degradation which is better that of the conventional floating-gate memory. All the characteristics above already hit the state-of-the-art of flash memory. Moreover, the charge stored in molecular layer is discrete, the charge will not migration in molecular layer and charge on one bit's storage center will not transfer to an adjacent bit cell, which suitable for a simple 3-D NAND structure. These properties experimentally demonstrate the potential of Ru molecular structure for future memory industry.

Chapter 4 Process Variation Control

Process variation is the one of the naturally occurring variation in the devices. (surface profile, dielectric quality, dimension and so on). All manufacturing and measurement processes exhibit variation. For example, when we measure sample data on the output of a process, such as critical dimensions, oxide thickness, or resistivity, we observe that all the values are not the exactly same. The process variation could be an important problem for the uniformity of redox-active molecular memory devices as the variation may affect the final performance of devices significantly. Moreover, with the further scaling down, the device will be even more sensitive to the process variation. Variation that is characterized by a stable and consistent pattern of variation over time. By well process variation control, the variation will be random in nature and will be exhibited by a uniform fluctuation about a constant level. Process variation control is an effective way to improve the device performance.

4.1 molecular attachment control

The molecular attachment and forming uniform film on substrate are the essential steps in molecular memory fabrication. The concept of controlled variation is important in determining if a molecular attachment process is stable. A process is considered as stable if it runs in a consistent and predictable trend. This means that the average process output is quite same and the variability is controlled. If the variation is uncontrolled, the quality,

coverage and other properties of attached molecular film will be irregular and unpredictable. The first set of parameters we want to control the molecular attachment process. As we discussed in the chapter 2, The attachment of redox-active molecules on Si/SiO_2 surfaces was fulfilled by self-assembled monolayers (SAMs) or few layers film on Si/SiO_2 surfaces. However, this process is sensitive to the solution concentration and temperature.

For temperature factor, it will affect the attachment speed by both reaction speed and evaporation of solution. After try and compare the result with several combination of solution concentrations, hotplate temperature and process duration time, we find that ~2 hours under 95 ℃ and 0.1 mmol/L solution concentration will be the best recipe to get high quality AUS linkage and control the uniformity of AUS linkage. The quality of AUS linkage molecule is controlled by the vendor, Sigma-Aldrich company, we buy this kind of chemical reagent in on batch reduce the variation.

By the same method, we also find the best attachment recipes for other molecules applied in our work. As the evaporation of liquid also helps the process during some attachment process, we use the same liquid volume and monitor the solution level every 15 min to keep the times for liquid all evaporated are similar. With the well-control in molecular attachment process, the variation is small enough to accept.

4.2 Dielectric layer control

The quality and uniformity and thickness of dielectric layer (tunneling oxide and blocking oxide) play an important role to improve the molecular memory performance. For

example, retention, program/erase (P/E) speed and endurance characteristics will be affected a lot by the thickness and quality of tunneling oxide. In our fabrication process, the tunneling oxide is grow by the rapid thermal oxidation (RTO) method. The temperature transition rates in RTO method is much faster than conventional furnace process. A precise temperature and oxidation time control is very important for RTO method oxide uniformity. The availability of many parameter that control RTO process make it a complex process. 100% accurate thickness and thickness distribution is not practicable.

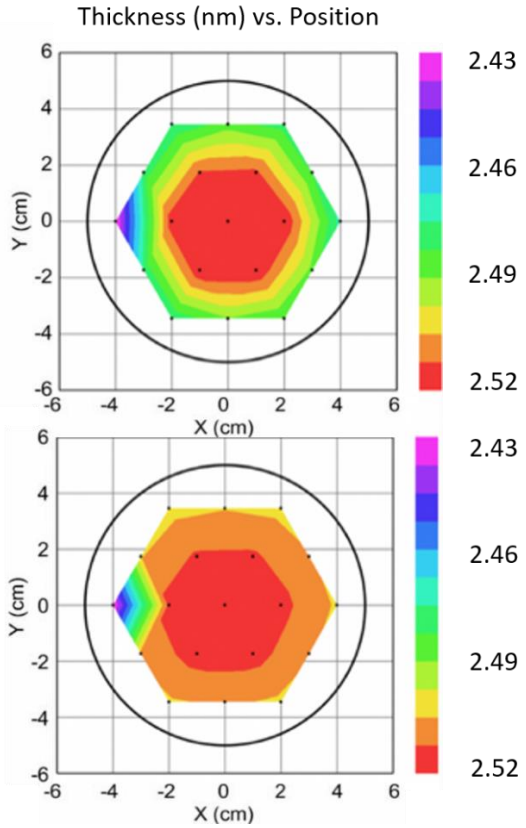

Figure 25 distribution of RTO oxide thickness

Figure 4.1 shows the two cycles of 2.5 nm RTO process depart with 2 hours. We can easily find there is variation of oxide thickness between each RTO cycle and different position in same wafer. The RTO oxide thickness in center position is thicker than edge position and the difference can be 0.1 nm. To minimize the variation produced by RTO machine itself, we do calibration run prior every time we use RTO machine and do empirical adjust to achieve the precise oxide thickness we want. To avoid the variation of oxide growth rate in different position, we fabricate our device only with the cutting pieces from center position. The thickness distribution is measured by ellipsometry method.

In summary, we try to make the device precisely follow our design. However, the process variation is inevitable in fabrication procedures. They may come from the intrinsic operation of process or outside environment parameters. The molecular attachment process control is the first problem we confronted. We optimized the attachment recipe and uniform the evaporation rate by real time monitoring. The tunneling oxide grown by RTO method. Thickness variation is caused by different machine condition and due to the location on wafer, calibration test cycle is applied prior to the real fabrication step for minimizing the variation. We only use the center part of the wafer after RTO process, to make sure the tunneling thickness difference between each memory device is enough small.

Chapter 5 Redox-Active Molecular Memory on Two-Dimensional Materials

5.1 Introduction

Two-Dimensional (2-D) materials, such as graphene, single layers of molybdenum disulfide (MoS_2) or boron nitride (BN) are considered as the thinnest electronic materials. Due to these materials are only one layer thick in vertical direction, they are typically considered as the ultimate limit of vertical scaling. 2-D materials can be employed for a wide range of application in nano-scale technology due to their excellent physical and electrical properties [116-127]. 2-D transition metal dichalcogenides (TMDCs) are the thinnest channel candidates with optimized gate control for metal oxide semiconductor field-effect transistor (MOSFET) because graphene is semimetal and BN usually consider as a dielectric material [128-133].

MOSFET based on MoS_2 is fabricated and demonstrated with gate control effect by B. Radisavljevic et al [134]. Scotch tape-based mechanical exfoliate is the most common method to prepare monolayer MoS_2 in lab. They prepared MoS_2 monolayers with this method and then transferred to degenerately doped silicon substrates covered with 270nm SiO_2. After that they proceed atomic layer deposition (ALD) of 30 nm HfO_2 as a high-k gate dielectric for the local top gate and mobility booster to realize the full potential of the single-layer MoS2. The resulting structure, composed of two field-effect transistors

connected in series, is shown in Figure 5.1. I_{ds}–V_{TG} curve recorded for a bias voltage ranging from 10 mV to 500 mV. Measurements are performed at room temperature with the back gate grounded. Top gate width was chosen as 4 mm; top gate length was 500nm. The device can be completely turned off by changing the top gate bias from –2 to –4 V. For V_d= 10 mV, the I_{on}/I_{off} ratio is $1\times\ 10^6$. For V_{ds} = 500 mV, the I_{on}/I_{off} ratio is 1×10^8 in the measured range while the subthreshold swing S= 74 mV/Vs. Top and bottom gate leakage is negligible. They also achieve the ohmic contact by applying Au electrode.

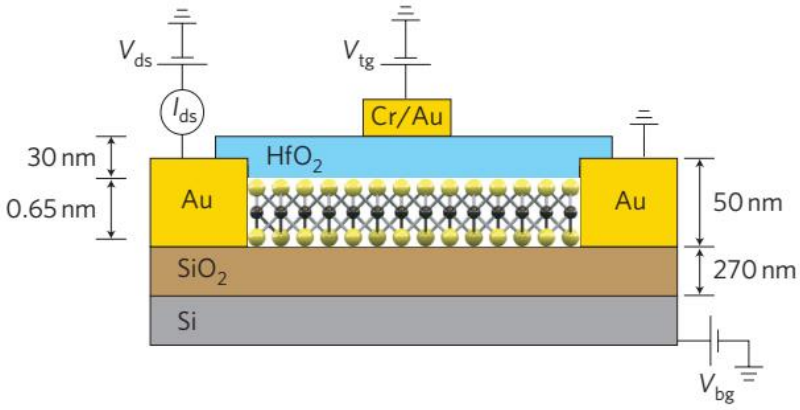

Figure 26 Schematic view of MoS_2 monolayer transistor

If the transistor based on monolayer MoS_2 channel could be realized, people can obviously fabricate flash-like memory structure with monolayer MoS_2 Channel. The non-volatile memory cells based on MoS2/Graphene heterostructures was reported by Simone Bertolazzi et al [135]. Their work started with growing graphene by chemical vapor deposition (CVD) method. Then, the graphene transferred onto silicon substrate with 270

nm SiO_2 layer. Graphene is patterned into stripes and contacted with metal leads. They prepare the monolayer MoS_2 by exfoliation method and transfer onto another SiO_2/Si substrate. Individual layers are distinguished by using optical microscope and transferred on top of the graphene stripes that form the source and drain electrodes in direct contact with monolayer MoS_2. A 6 nm thick HfO_2 film grown using atomic layer deposition (ALD) is acting as the tunneling oxide layer. Multilayer graphene flakes with the thickness of 1.5 nm are transferred onto the tunneling oxide and positioned above the MoS_2 flakes. The memory structure is end up with the floating gate is capped by a 30 nm thick HfO2 layer followed by the deposition of the control gate. Figure 5.2 shows the 3-D schematic view of memory device based on monolayer MoS_2.

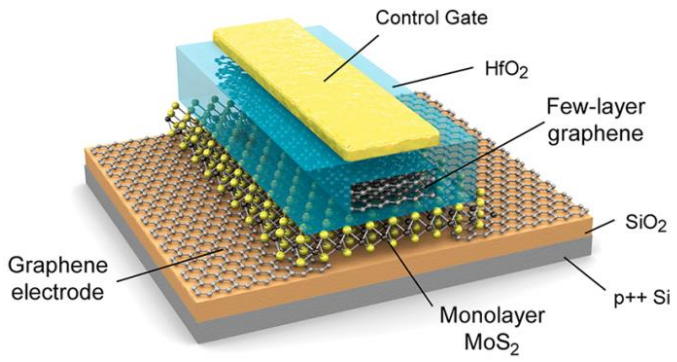

Figure 27 schematic view of memory device based on monolayer MoS_2

As their report, A memory window over 8V is observed. The on/off ratio of their MoS2 based memory device is more than 10^4, the retained charge will be about 30% to the initial number estimated from the 10^4 s retention measurement. The total 2-D materials memory

device is demonstrated in this report.

The exfoliation method for monolayer TMDC preparation is depend on the layers in TMDC bulk are held together by van der Waals forces, so that cleave them to the limit of monolayer is easy. Although the scotch-tape based exfoliation method is simple and cheap cost, the flake size and monolayer TMDC yield is poor. Some modifications during exfoliation process to improve exfoliation quality have been proposed and reported [136 - 140]. The Au-mediated exfoliation considered as an effective way to improve the quality of mechanical exfoliation TMDC materials have been reported by Ali Javey et al [141]. The Au-mediated exfoliation is start with a 100-150 nm gold deposition onto bulk MX_2 (M = Mo or W; X = S or Se) crystals by evaporator method. The gold atoms bond with the chalcogen atoms of the topmost layer of MX2. The interaction of the topmost layer with the evaporated gold is stronger than the interactions of that same layer with the bottom layers of MX_2. This enables selective peel-off of the top layer using a thermal release tape which is later stuck onto the target substrate. After that they release thermal tape by put it on a hot plate (≈130 °C) and the substrate is treated with a mild O_2 plasma to remove the tape residue from the surface. The O_2 plasma power and etching time are kept low to ensure that the gold is not etched away, thereby exposing the underlying monolayer MX_2. The gold film is then etched by wet etching method, which does not etch the TMDC flakes. The large-area monolayers of TMDC will be obtained after acetone and IPA rinse clean. The size and yield of exfoliated monolayer MoS_2 increase significantly by using this Au-mediated exfoliation method. Figure 5.3 displays the histogram of flake area for the improvement of Au-exfoliated MoS_2 [141].

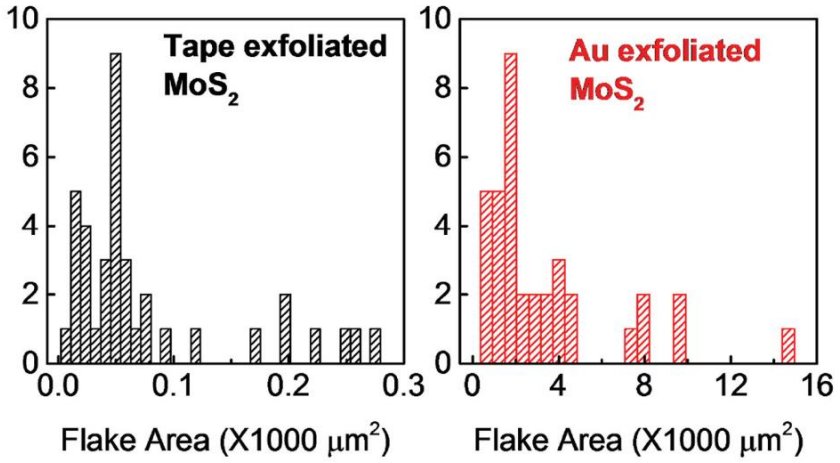

Figure 28 Histogram of flake areas for tape-exfoliated vs. Au-exfoliated MoS_2

5.2 Experiment details

In our work, we have developed and optimized a monolayer MoS_2 based molecular integration method to exploit the intrinsic redox properties and investigate the memory performance by measuring transistor structure molecular memory. the memory devices based on 11-(Ferrocenyl)undecanethiol molecule (Fe molecule) exhibit nonvolatile flash like behaviors. The memory device based on Fe molecule exhibits a memory window of ~2 V, retention property of the Fe molecular memory also be obtained, and negligible degradation after P/E cycles up to 10^5.

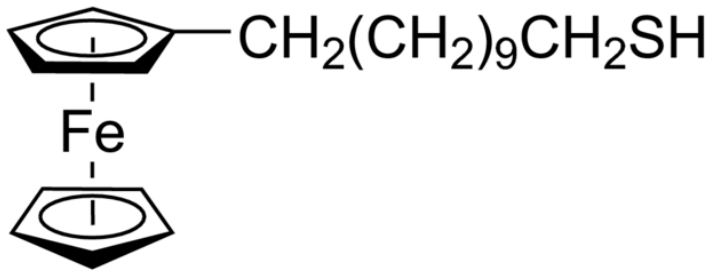

Figure 29 molecule structure of 11-(Ferrocenyl)undecanethiol

We have fabricated memory cells with Fe molecule/MoS_2 gate stacks structure. Figure 5.4 illustrate the structure of the Fe molecule with the chemical formula: $C_{21}H_{32}FeS$, this redox-active Fe molecule is bought frim Sigma Aldrich company. The connection between MoS_2 and Fe molecule is covalent bond.

The metal-oxide-semiconductor (MOS) field-effect transistor structure, applied in our Flash-based memory devices was fabricated with the redox-active Fe molecule as the charge storage layer. Preparation of Monolayer MoS_2 and Fe molecule attachment on MoS_2 surface are the most important fabrication process steps. Our work is start with a 290 nm SiO_2 film thermally grown on moderate-doped n-type (100) Si wafer substrates (~10^{17} cm^{-3} phosphorous doped) by dry oxidation in CMOS oxidation furnace. The 290nm SiO_2 is used for identifying the color of different layer number of MoS_2 under optical microscopy and will be the target substrate for exfoliated MoS_2 monolayer. Monolayer MoS_2 flakes is prepared by Au-mediated mechanical exfoliation method [141].

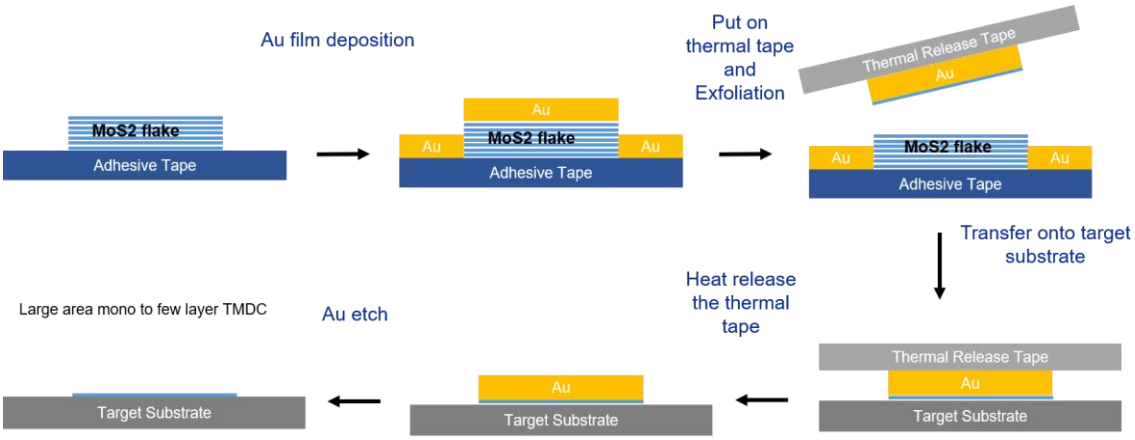

Figure 30 schematic illustration of the Au exfoliation process.

The detailed process flow is illustrated in Figure 5.5. 100 nm Gold is evaporated onto preliminary tape exfoliated MoS_2 pieces. The gold atoms bond with the chalcogen atoms of the topmost layer of MoS_2. The interaction of the topmost layer with the evaporated gold is stronger than the Van der Waals force interactions of that same layer with the bottom layers of MoS_2. This enables selective peel-off of the topmost layer using a thermal release tape which is later stuck onto the desired target substrate (SiO_2/Si). The thermal tape is then released on a hot plate (~130 °C) by several minutes. After that the substrate is treated with a mild O_2 plasma to remove the tape residue from the surface. The O_2 plasma power and etching time should not be high in order to protect the Au film, thereby exposing the underlying monolayer MoS_2. The gold film is then etched using Gold etchant, which does not harm to the MoS_2 flakes. The exfoliate MoS_2 flakes will be cleaned by Acetone and IPA rinse to remove residues adhere on the MoS_2 surface and obtain the large-area monolayers. Microscope image of exfoliated monolayer MoS2 on 290 nm SiO2/Si substrate, lithography patterned MoS_2 sample and MoS_2 sample with evaporated

electrode are displayed in Figure 5.6.

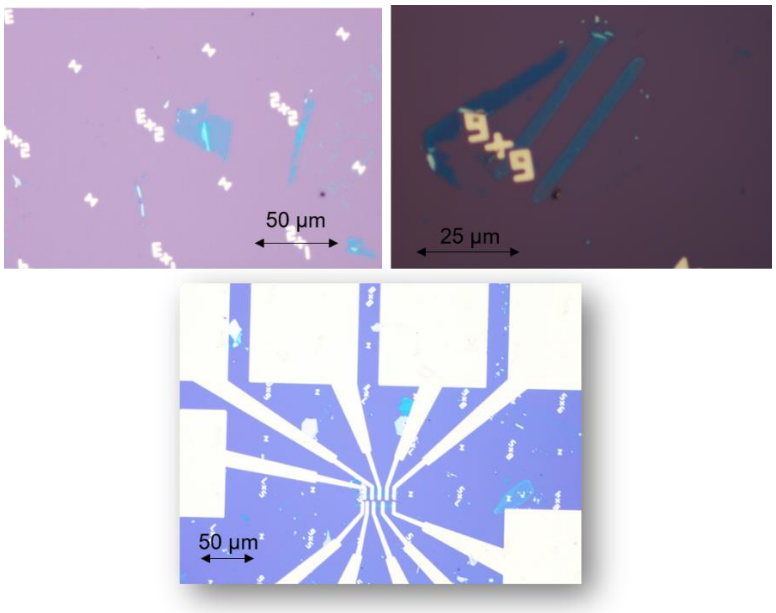

Figure 31 Optical microscope images of (left) a large monolayer MoS_2, (right) patterned MoS_2 stripe and (bottom)MoS_2 with electrode

Monolayer MoS_2 is patterned photolithography method and then etched by Reactive-ion etching (RIE) in O_2 plasma as the width of monolayer MoS2 channel is 4 μm. The drain and source electrode 35nm Ti/Au are deposited and patterned on MoS_2 by photolithography and E-beam evaporation, followed by the lift-off. The redox 11-(Ferrocenyl)undecanethiol molecules solution is prepared by dissolving the molecules in toluene solvent, the concentration is 0.1mmol/L. The attachment process of molecules on MoS_2 surface is realized by immersing the substrate in to molecular solution for 3 hours with 70 ℃ hotplate.

The attachment process is performed in glovebox with N_2 environment. After the molecular film was formed, two cycles of 2 min sonication clean was applied to rinse the attached sample for removing physisorbed residuals on the surface with toluene solvent. The molecular attached samples will immediately load into the Atomic Layer Deposition (ALD) vacuum chamber right after the sonication clean for blocking oxide 30 nm Al_2O_3. The ALD operation temperature is set to 100 ℃ in case of the instability of organic molecule, with H_2O and TMA as precursors. Finally, a layer of 105 nm Pt is deposited and patterned on the top of the devices as the top gate by photolithography and E-beam evaporation, followed by the lift-off process. We also fabricated the transistor structure with out 11-(Ferrocenyl)undecanethiol attachment process as the control sample for comparison.

5.3 Exfoliated MoS_2 and molecule attachment characterization

Multiple processes have been applied all through the Au-mediated exfoliated MoS_2 flakes, including the scotch tape exfoliation, metal evaporation, thermal tape sticking, Au etching and solvent cleaning. Careful characterization should be applied to monitoring the quality and layer of exfoliated MoS_2 flakes. Raman spectra measurement is applied to characterize the Au-exfoliated MoS_2 flakes. Figure 5.7 shows that the Raman spectra of Au-mediated exfoliated MoS_2 with different layer number (preliminary judged by the optical microscope). As the result, the Raman spectra for Au-mediated exfoliation method monolayer or few layers MoS_2 are identical to those prepared with other method. No new feature or peak position can be found in Raman spectra measurement. The peak position of different layer MoS_2 is nothing different with other report, which demonstrate the flakes

are not strained. The layer number of MoS_2 flakes can be identified by Raman peak positioning, the Raman mapping measurement has been performed and the data is shown in Figure 5.8.

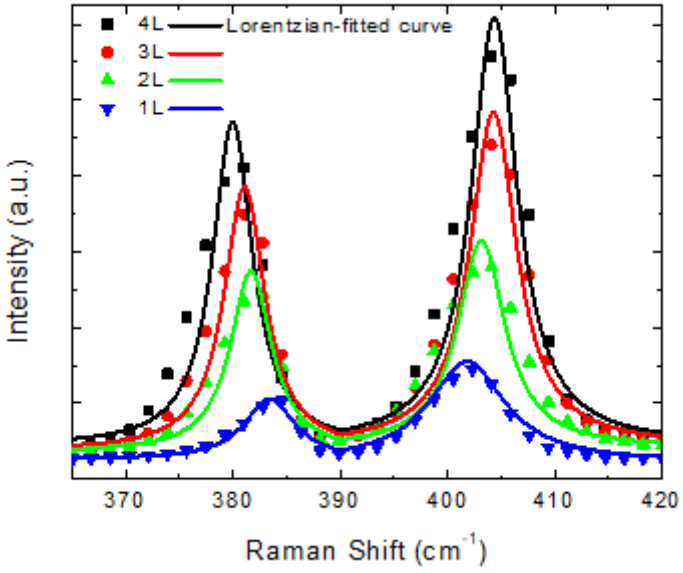

Figure 32 Raman spectra measurement on MoS_2 samples with different layer number

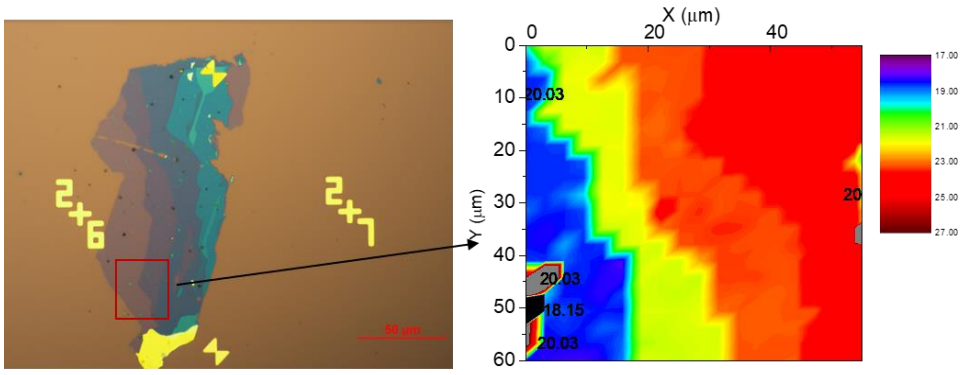

Figure 33 Microscope image of MoS_2 flake contain different layer number and corresponding Raman peak mapping, the color reflects the peak position difference.

In order to monitor the quality of 11-(Ferrocenyl)undecanethiol molecular attachment, XPS measurements were applied on the samples with 11-(Ferrocenyl)undecanethiol film on the MoS_2 surface. To avoid the small sample size, the samples for XPS measurement is made by attaching the 11-(Ferrocenyl)undecanethiol on CVD method MoS_2 film with quartz substrate. As shown in Figure 5.9, Fe 2p peaks can be find easily after the attachment process, while there is no Fe signal before the attachment. The result of XPS measurement demonstrate that the attachment on MoS_2 film is successful and will not be removed by sonication clean. Due to the signal of Fe 2p is so strong, the attached 11-(Ferrocenyl)undecanethiol molecular film is judged as multi-layer.

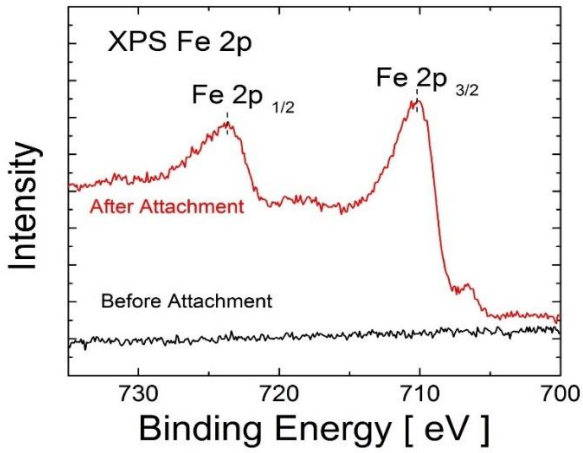

Figure 34 XPS of the samples with 11-(Ferrocenyl)undecanethiol attached on MoS_2 and Bare MoS_2 before attachment

5.4 Characterization of molecular memory on monolayer MoS_2

The redox-active molecular memory with transistor structure will allow us to use regular electronics characterization metrologies to determine the memory performance of 11-(Ferrocenyl)undecanethiol molecular memory based on monolayer MoS_2. In our work we demonstrate a redox molecular memory with monolayer MoS_2, shows a flash-like memory behavior. The schematic of a 11-(Ferrocenyl)undecanethiol molecular memory cell is shown is Figure 5.10. Molecular film is formed on MoS_2 surface with low cost and total solution process approach. Although the memory characteristics performance is not so good in 11-(Ferrocenyl)undecanethiol molecular memory, it can be improved by further engineering and optimization.

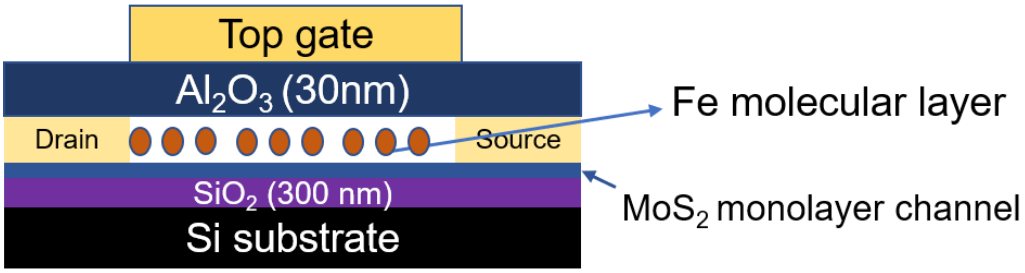

Figure 35 schematic of a MoS_2 based Fe molecular memory cell based on monolayer MoS_2 channel

We have characterized the Au exfoliated method and molecule attachment process by Raman spectra and XPS measurements, showing that the quality of MoS_2 flake is good and 11-(Ferrocenyl)undecanethiol was successfully attached on MoS_2 surfaces. Due to the Schottky contacts between the S/D electrodes and Au-exfoliated monolayer MoS_2, we assume the 11-(Ferrocenyl)undecanethiol molecular devices in Schottky-barrier n-type MOSFET characteristics. Figure 5.11 shows the output characteristics of the molecular FET structure in linear scale. The result show source-drain current versus source-drain voltage (I_{DS}-V_{DS}) curves is quite smooth and well saturated. The contact resistance between monolayer MoS_2 channel and Ti/Au electrode is small enough to affect the FET performance. Overall the molecular memory device functions as a conventional MOSFET.

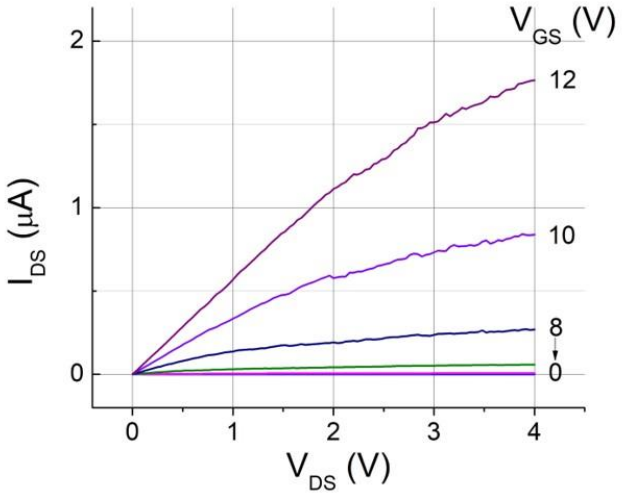

Figure 36 Output characteristic of MoS_2 based Fe molecular memory with V_{GS} varies from 0V to 12V, with step of 1V.

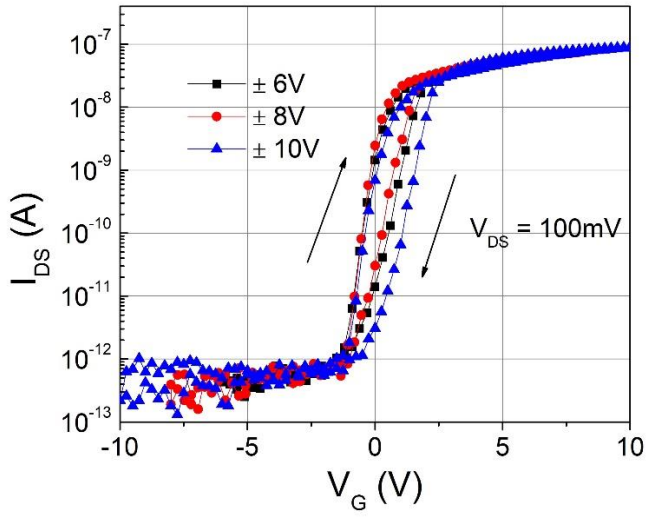

Figure 37 Transfer characteristics of MoS_2 based Fe molecular memory with V_{DS} =100 mV

The transfer characteristics source-drain current vs. gate voltage (I_{DS}-V_{GS}) of the redox molecular memory are displayed in Figure 5.12. From the curve, hysteresis loops are observable at different gate voltage, indicating the charging and discharging occur in the charge storage layers in molecular memory cells, the memory window of the device is showing ~2 V with ±10 V gate voltage sweep range. In contrast, the structure with on redox molecular film shows negligible memory window with the same characterization condition.

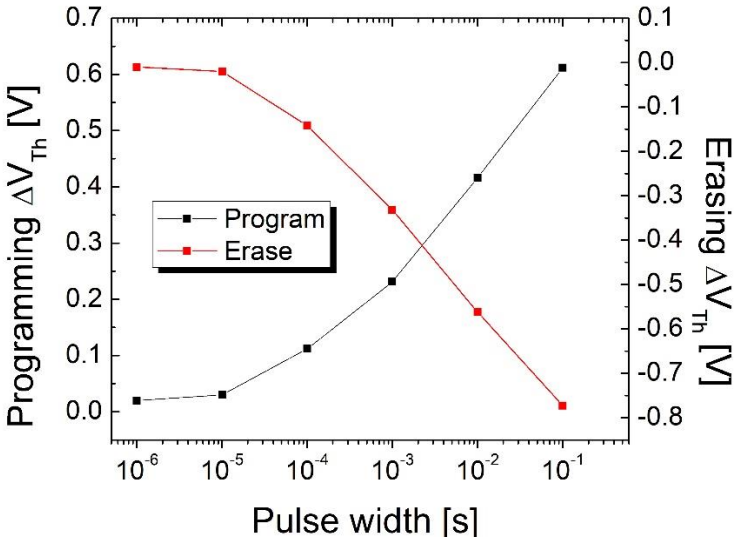

Figure 38 P/E switch characterization of MoS_2 based Fe molecular memory

The programing and erasing response speed of MoS_2 based Fe molecular memory memory devices were investigated by observing the threshold voltage change $\triangle V_{Th}$ with different P/E pulse width under ±10 V top gate voltage bias. The P/E operations were performed by applying gate voltage rectangular pulses while the source and drain

electrodes were both grounded. The response speed characteristic is shown in Figure 5.13. The change of threshold voltage mainly due to the stored charge in redox center of Fe molecular film. When applying a positive gate voltage, the electrons will transfer from the MoS_2 monolayer and get stored in Fe molecule redox center and cause the reduction which could be considered as programming operations and result in a positive V_{Th} change. In contrast the application of a negative gate voltage will drive back the stored electrons to the MoS_2 channel, and cause a negative shift of the V_{Th}, which can be defined as erasing operations. This molecular memory shows fast P/E speed derives from the intrinsic fast charging and discharging of Fe molecule, the device shows an observable $\triangle V_{Th}$ when applying a +10V, 100 μs programming gate voltage pulse. The erasing operation threshold voltage shift $\triangle V_{Th}$ with a -10 V, 100 μs is even greater than the one in programming operation. The faster speed in erasing compared with programming can be attribute to the charging at the interface trap states between monolayer MoS_2 and Fe redox molecule. The presence of these states might due to the natural property of the Fe molecule and monolayer MoS_2, or surface defects introduced by Au-mediated exfoliation method and other fabrication steps [142].

The retention characteristics of MoS_2 based Fe molecular memory are measured in room temperature, the results are illustrated in Figure 5.14. The initial program/erase states are defined with ±10 V, 2 ms gate voltage pulse, respectively. The initial threshold voltage shift ($\triangle V_{Th}$) are 0.25 V for program state and -0.36 V for erase state. Overall, the device shows moderate retention characteristics as $\triangle V_{Th}$ had a slight degradation during the measure time of 10^4 s and by extrapolating the tendency line form the experimental data

we estimate the memory window will totally lose after 10^7 s for both states. The result of retention property is due to there is no extra intercalate dielectric layer between the monolayer MoS_2 channel and Fe redox molecule. The redox center which considered as the charge storage site is insulated with MoS_2 channel only by the redox molecule moieties although intrinsic redox behavior of Fe molecule will provide relative robust charge storage states. Another assumption for the retention performance is that part of the injected charge stored in the traps located at Fe molecule/MoS_2 interface. The charge stored in interface trap stats is easy to vertical migration and this leads to a memory window loss in early stage.

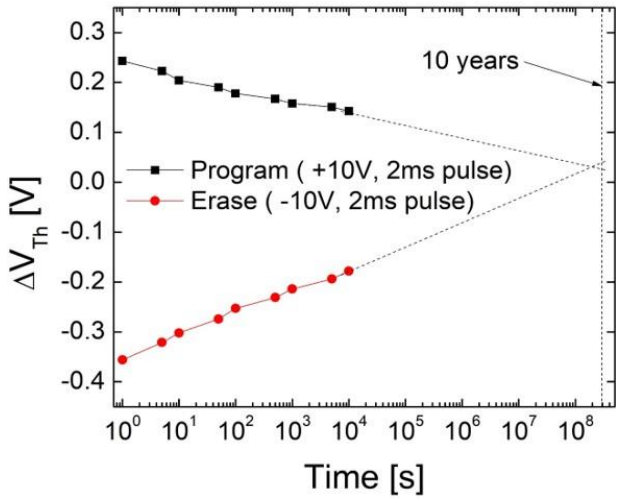

Figure 39 Retention characterization of MoS_2 based Fe molecular memory

The endurance characteristic of the MoS_2 based Fe molecular memory were characterized by applying a Program/Erase voltage of ±10 V with 2ms width at room temperature was applied to top gate(Figure 5.16). Change of V_{FB} after certain numbers of P/E cycles are record. The degradation of $\triangle V_{FB}$ negligible when compare with the initial value of program state and erase state after 10,000 cycles, this performance already satisfied the current demand of flash memory application. This memory sample will not fail after even a large number of erase and rewrite cycles indicating high reliablility and stable switching endurance property. The good endurance characteristic is derived from the stable valence state of redox center due to the intrinsic redox property of 11-(Ferrocenyl)undecanethiol. Overall the performance of MoS_2 based Fe molecular memory is good, but further optimization is still needed to benefit the retention and P/E speed properties.

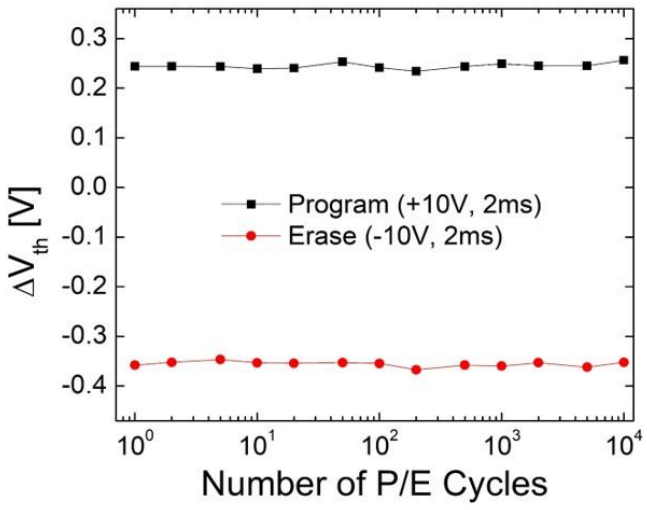

Figure 40 Endurance property of MoS_2 based Fe molecular memory

As the previous discussion, the result of retention property is due to no extra intercalate dielectric layer between the monolayer MoS_2 channel and Fe redox molecule. In order to improve the memory performance of MoS_2 based Fe molecular memory. But the 11-(Ferrocenyl)undecanethiol cannot be attached on common dielectric surfaces like Al_2O_3. Monolayer hexagonal boron nitride (h-BN) have the similar crystal structure with graphene and a 5.9 eV bandgap consider as a good 2-D insulator. Due to the wide bandgap monolayer h-BN can be used as a passivation layer or tunneling barrier layer to improve other 2-D materials especially for monolayer TMDCs [143]. By using h-BN, we may optimize the previous molecular memory structure by introducing MoS_2/h-BN/MoS_2 sandwich structure. The monolayer MoS_2 can be better protected by encapsulated with h-BN, and the topmost MoS_2 is acting as the surface for molecular attachment. The h-BN layer will act as the tunneling barrier layer and help to keep the stored charge for a longer period.

5.5 Summary

In this chapter, we have discussed the development of 2-D materials devices and our work on 2-D material based redox molecular memory. The monolayer MoS_2 is prepared by Au-mediated exfoliation method and characterized with optical microscope and Raman spectra measurement. The redox molecular memory devices with 11-(Ferrocenyl)undecanethiol based on MoS_2 channel are fabricated and measured. The redox molecular memory devices based on MoS_2 exhibit memory effect and good endurance property, but the retention characteristic is not so good. Negligible degradation after 10^4

P/E cycles and slight charge loss over 10^4 s are observed. The performance of retention property should attribute to lack of enough dielectric barrier to keep the stored charge. Structure optimization method has been proposed by introducing the MoS_2/h-BN/MoS_2 stack where h-BN layer act as the tunneling barrier layer.

Chapter 6 Conclusion and Future Work

6.1 Conclusion

In this work, our research is focused on novel non-volatile memory containing redox molecule. The memory cell is fabricated with bottom-up approaches combining with molecular attachment process. The detailed fabrication processes have been explained. The optimization of some fabrication steps was also explored and discussed. The performance of memory characteristics have been analyzed and proposed further improve method. The major efforts of this dissertation are summarized as follows:

(1) Molecular attachment on Si and monolayer MoS_2 have been studied and characterized with CyV, XPS and AFM measurement. The molecular films have been demonstrated with good uniformity and quality. Au-mediated exfoliation method have been performed in preparation of large area MoS_2 for memory cell fabrication.

(2) Redox molecular memory on Si have been fabricated and studied for high-performance non-volatile memory applications. The Si based molecular memory has been demonstrated good P/E speed and excellent retention characteristics. The good performance and low-cost fabrication process make it very attractive for long retention non-volatile memory applications.

(3) Redox molecular memory on monolayer MoS_2 have been fabricated. The memory performances have been characterized and analyzed. The retention property is not so good due to thin tunneling barrier. We proposed new idea to improve the performance of

monolayer MoS_2 based molecular memory.

6.2 Future work

There are some areas we still need to further study and improve upon our recent work. First, we will keep on exploring new molecules with different metal redox center and different chemical structure as new materials is key factor for future development of non-volatile memory. In addition, Further optimization of molecular attachment recipe and device structure are also effective approaches in performance improvement. We will try to improve the retention performance of MoS_2 based molecular memory by using h-BN as tunneling barrier layer. Third, we will study the integration of the molecular memory cells with logic circuit.

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Biography

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