GALLIUM OXIDE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR ANALYTICAL MODELING AND POWER TRANSISTOR DESIGN TRADES

by

Neil Austin Moser

A Dissertation
Submitted to the
Graduate Faculty
of
George Mason University
in Partial Fulfillment of
The Requirements for the Degree
of
Doctor of Philosophy
Electrical and Computer Engineering

Committee:

_____	Dr. Nathalia Peixoto, Dissertation Director
_____	Dr. Qiliang Li, Committee Member
_____	Dr. Yuri Mishin, Committee Member
_____	Dr. Gregg Jessen, Committee Member
_____	Dr. Monson Hayes, Department Chair
_____	Dr. Kenneth S. Ball, Dean, Volgenau School of Engineering
Date:_____	Fall Semester 2017 George Mason University Fairfax, VA

Gallium Oxide Metal Oxide Semiconductor Field Effect Transistor Analytical Modeling and Power Transistor Design Trades

A Dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy at George Mason University

by

Neil Austin Moser
Master of Science
George Mason University, 2013
Bachelor of Science
University of Michigan-Ann Arbor, 2002

Director: Nathalia Peixoto, Professor
Department of Electrical and Computer Engineering

Fall Semester 2017
George Mason University
Fairfax, VA

DEDICATION

This is dedicated to my father, Gary Moser, who started me on the path to being an academic before I even really knew what that was and still encourages me to not be ignorant about anything to this day.

ACKNOWLEDGEMENTS

I would like to thank my wife, Morgan, and daughter, Schaefer, for putting up with me "working" on this for quite a long time. Also, I would like to thank my committee, especially Gregg Jessen who helped me find this exciting research and shepherded me the whole way and Nathalia Peixoto who put up with a lot of dead ends and redirections in topic along the way. I would like to thank everyone on the Air Force Research Laboratory gallium oxide and lab teams who loaned me a few of their exciting projects and helped me with everything from test equipment training to stepper lithography exposures to editing of journal papers. I would also like to acknowledge the SMART scholarship for service program which funded the last three years of schooling toward this final goal.

TABLE OF CONTENTS

LIST OF TABLES

Table **Page**

LIST OF FIGURES

Figure **Page**

LIST OF EQUATIONS

Equation **Page**

LIST OF AUTHOR PUBLICATIONS

Large portions of the work presented in this dissertation were published by the author in the following peer reviewed journals and conference proceedings.

[1] N. A. Moser, J. P. McCandless, A. Crespo, K. D. Leedy, A. J. Green, E. R. Heller, K. D. Chabak, N. Peixoto, and G. H. Jessen, "High pulsed current density β-Ga_2O_3 MOSFETs verified by an analytical model corrected for interface charge," Appl. Phys. Lett., vol. 110, no. 143505, pp. 1–5, 2017.

[2] N. Moser, J. Mccandless, A. Crespo, K. Leedy, A. Green, A. Neal, S. Mou, E. Ahmadi, J. Speck, K. Chabak, N. Peixoto, and G. Jessen, "Ge-doped β-Ga_2O_3 MOSFETs," IEEE Electron Device Lett., vol. 38, no. 6, pp. 775-778, 2017.

[3] N. A. Moser, K. D. Chabak, A. J. Green, D. E. Walker, S. E. Tetlak, E. Heller, A. Crespo, R. C. Fitch, J. Mccandless, K. D. Leedy, M. Baldini, G. Wagner, G. D. Via, J. D. Blevins, and G. Jessen, "Device Development of Gallium Oxide MOSFETs Grown by MOVPE on Native Substrates for High-Voltage Applications," in CS Mantech Digest, 2017, no. 14.4, pp. 1–4.

[4] N. A. Moser, A. Crespo, S. E. Tetlak, A. J. Green, K. D. Chabak, and G. H. Jessen, "Investigation of thermal effects in β-Ga_2O_3," in 2016 74th Annual Device Research Conference (DRC), 2016, pp. 1–2.

[5] K. D. Chabak, N. Moser, A. J. Green, D. E. Walkerjr, S. E. Tetlak, E. Heller, R. Fitch, J. P. Mccandless, K. Leedy, M. Baldini, G. Wagner, X. Li, G. Jessen, "Enhancement-mode Ga_2O_3 wrap-gate fin field-effect transistors on native (100) β-Ga_2O_3 substrate with high breakdown voltage," vol. 109, no. 213501, pp. 2–5, 2016.

[6] A. J. Green, K. D. Chabak, M. Baldini, N. Moser, R. C. Gilbert, R. Fitch, G. Wagner, Z. Galazka, J. Mccandless, A. Crespo, K. Leedy, and G. H. Jessen, "β-Ga_2O_3 MOSFETs for Radio Frequency Operation," IEEE Electron Device Lett., vol. 38, no. 6, pp. 790-793, 2017.

[7] K. D. Leedy, K. D. Chabak, V. Vasilyev, D. C. Look, J. J. Boeckl, J. L. Brown, E. Tetlak, A. J. Green, N. A. Moser, A. Crespo, D. B. Thomson, R. C. Fitch, P. Jonathan, G. H. Jessen, "Highly conductive homoepitaxial Si-doped Ga2O3 films on (010) β-Ga2O3 by pulsed laser deposition," Appl. Phys. Lett., vol. 111, no. 012103, pp. 1–4, 2017.

[8] G. Jessen, K. Chabak, A. Green, J. McCandless, S. Tetlak, K. Leedy, R. Fitch, S. Mou, E. Heller, S. Badescu, A. Crespo, and N. Moser, “Toward realization of Ga_2O_3 for power electronics applications,” in 2017 75th Annual Device Research Conference (DRC), 2017, pp. 1–2.

[9] K. Chabak, A. Green, N. Moser, S. Tetlak, J. McCandless, K. Leedy, R. Fitch, A. Crespo, and G. Jessen, “Gate-recessed, laterally-scaled β-Ga_2O_3 MOSFETs with high-voltage enhancement-mode operation,” in 2017 75th Annual Device Research Conference (DRC), 2017, pp. 1–2.

LIST OF ABBREVIATIONS AND SYMBOLS

Baliga's conduction loss Figure of Merit ..... BFOM
Contact Resistance ..... R_C
Direct Current ..... DC
Electron Charge ..... q
Field Effect Transistor ..... FET
Gallium Arsenide ..... GaAs
Gallium Nitride ..... GaN
Gallium Oxide ..... Ga_2O_3
Gate Turn-off Thyristor ..... GTO
Halide Vapor Phase Epitaxy ..... HVPE
Heterojunction Field Effect Transistor ..... HFET
High Electron Mobility Transistor ..... HEMT
Insulated Gate Bipolar Transistor ..... IGBT
Johnson's Figure of Merit ..... JFOM
Low Pressure Chemical Vapor Deposition ..... LPCVD
Maximum Saturated Drain Current ..... IMAX
Metal Oxide Semiconductor Field Effect Transistor ..... MOSFET
Metalorganic Vapor Phase Epitaxy ..... MOVPE
Modulation Doped Field Effect Transistor ..... MODFET
Molecular Beam Epitaxy ..... MBE
On Resistance ..... R_{ON}
Pulsed Laser Deposition ..... PLD
Radio frequency ..... RF
Relative Dielectric Constant ..... ε_r
Saturated Drain Current at Zero Gate Voltage ..... I_{DSS}
Scanning Electron Microscopy ..... SEM
Schottky Barrier Diode ..... SBD
Sheet Resistance ..... R_{SH}
Silicon Carbide ..... SiC
Transfer Length Method ..... TLM
Transmission Electron Microscopy ..... TEM
Transparent Conductive Oxide ..... TCO
Two dimensional electron gas 2DEG
Van der Pauw ..... VDP

ABSTRACT

GALLIUM OXIDE METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR ANALYTICAL MODELING AND POWER TRANSISTOR DESIGN TRADES

Neil Austin Moser, Ph.D.

George Mason University, 2017

Dissertation Director: Dr. Nathalia Peixoto

Gallium oxide has recently emerged as a promising semiconductor material for high voltage switch applications owing to its ultra-wide band gap of ~4.8 eV and the corresponding expected critical field strength of ~8MV/cm. β-Ga_2O_3, which is the most stable polymorph, also has the advantage of melt grown, defect free, large diameter native substrates which are traditionally much more cost effective than vapor phase substrates such as those for incumbent power switching materials like gallium nitride and silicon carbide. Using these substrates, researchers have already developed high quality homoepitaxial channel layers with n-type doping concentrations ranging from 10^{16} to $>10^{20}$ cm^{-3} using group IV materials as dopants. Further, several groups have fabricated metal semiconductor and metal oxide semiconductor field effect transistors (MESFET and MOSFET) using these channel layers with excellent current control and high breakdown voltages.

In this work, we utilize silicon MOSFET theory to develop a simple analytical model for the state-of-the-art depletion mode β-Ga_2O_3 MOSFET. The model is verified for devices with varying doping concentration and channel thickness and is also investigated for gate oxide changes and operating temperature. Implications for device development toward low loss power switches and radio frequency (RF) devices are provided using the model formulation. Limitations of the simple model and potential future additions toward a comprehensive compact model as the gallium oxide material system matures are also investigated. Finally, future β-Ga_2O_3 device developments are anticipated, and it is shown how the model can be used to expedite the development of these devices.

1. POWER SEMICONDUCTOR INTRODUCTION

Gallium oxide (Ga_2O_3) has rapidly emerged in the past decade as a semiconductor with material properties far exceeding silicon, and even greater than silicon carbide (SiC) and gallium nitride (GaN), for many power semiconductor and possibly high power radio frequency (RF) switch applications. While silicon has been the dominant semiconductor in both digital and analog transistor applications since the start of the information age, its limitations become apparent when operating in high voltage, high current, high power, and high temperature environments allowing for other semiconductor materials such as SiC and GaN to find a niche and dominate large market segments relatively untouched by silicon and its in-place foundry infrastructure. Transistor devices using gallium oxide have promising potential to offer even more capability at lower cost within these markets; thus, the transistor device community is rapidly evaluating and maturing gallium oxide technology. This dissertation specifically lays the groundwork to determine the applicability of silicon metal oxide semiconductor field effect transistor (MOSFET) theory and associated analytical modeling to gallium oxide field effect transistors (FETs). This is an essential first step in analyzing whether the desirable properties of gallium oxide can be understood and realized in real device applications. Additionally, after a simple theory is developed and verified through experiments on fabricated devices, numerous device design trades are presented that will shape the future of gallium oxide

transistor development and help determine if its potential material advantages can be realized in devices needed for new or improved applications.

To aid the discussion in future chapters, the rest of Chapter 1 describes the wide bandgap semiconductor market in general by laying out specific qualities of a semiconductor with advantages for this market and describing some performance requirements and market applications for power semiconductor and power RF devices.

Wide Bandgap Semiconductor Materials

While silicon is certainly not absent from the power semiconductor and analog RF markets, it is often advantageous to use other semiconductors, in this case Ga_2O_3, with material properties that are more suitable than silicon for designing power and RF semiconductor devices. Better semiconductor materials allow designers to reduce the size and/or complexity of their designs or even exploit new market segments where silicon is not suitable at all. The material-based origins of power semiconductor properties in Ga_2O_3 will be evident in Chapter 2 and 3, but here we lay out the basic advantages of Ga_2O_3 and other wide bandgap semiconductors.

As mentioned above, Ga_2O_3 and other wide bandgap semiconductors provide advantages over Silicon when used to create several semiconductor devices including transistors and diodes that operate in high voltage, high current, high power, or high temperature environments. The property that differentiates these materials from other semiconductors is a large difference in energy potential between the top of the valence band and the bottom of the conduction band commonly referred to as a wide or ultra-wide bandgap. Ga_2O_3 has a bandgap of ~4.8 eV which is much larger than Silicon's

bandgap of ~1.1 eV and even significantly larger than the bandgap of other power semiconductor materials like GaN (~3.4 eV) and SiC (~3.3 eV). The origin of this large bandgap is explained further in Chapter 2, but put simply, it is related to the strong ionic bonds between the gallium and oxygen atoms of the crystal lattice in gallium oxide which increases the energy required to ionize an electron from the crystal lattice (the valence band) and allow it to move freely about the lattice (the conduction band). This single property leads to two other desirable properties that are the basis for the advantages of using gallium oxide in device designs over silicon and other wide bandgap semiconductors.

First, the wide bandgap leads to a reduced intrinsic carrier concentration. The intrinsic carrier concentration can be estimated from quantum statistical mechanics as shown in Equation 1 [1]. From this equation, it is evident that an exponential decrease occurs in the intrinsic carrier concentration as the materials bandgap becomes wider (E_G becomes larger) at a given temperature. Additionally, the intrinsic carrier concentration will remain lower at higher temperature (as T increases) for devices with a wider bandgap.

Equation 1 Intrinsic Carrier Concentration. N_X is the conduction (C) or valence (V) band effective density of states, E_G is the material bandgap, k is Boltzmann's constant, and T is the temperature in Kelvin.

$$n_i = \sqrt{N_C N_V}\exp\left(\frac{-E_G}{2kT}\right)$$

This is shown graphically in Figure 1 using estimates for the temperature dependent bandgap (Equation 2), and the temperature dependent density of states in the valence and conduction bands (Equation 3) based on the material parameters of the listed power

semiconductors that will be further analyzed in Chapter 2. The intrinsic carrier concentration determines the ability to modulate the device using externally applied potentials. When the intrinsic carrier concentration approaches the value of the conduction band density of states, the material ceases to operate as a semiconductor. Thus, a low intrinsic carrier concentration improves the semiconducting property at high temperature.

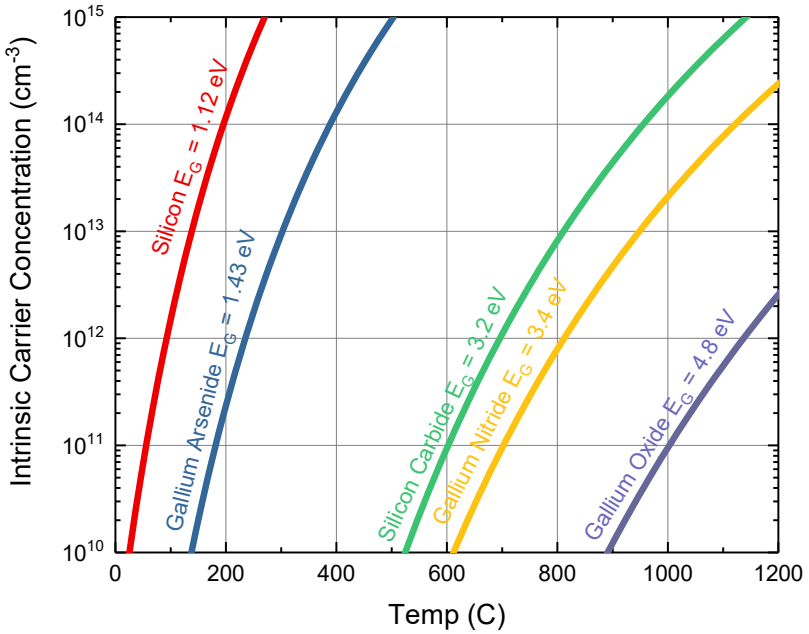


Figure 1 Intrinsic carrier concentration versus temperature for several important semiconductors. The dependence on the material bandgap is evident (increasing bandgap from left to right).

Equation 2 Temperature dependent bandgap. *T* is the temperature in Kelvin, *β* and *α* are empirical fitting parameters, and *$E_G(T=0)$* is the bandgap at a temperature of 0 K.

$$E_G = E_G(T=0) - \frac{\alpha T^2}{(T+\beta)}$$

Equation 3 Temperature dependent density of states in the valence or conduction band. *k* is Boltzmann's constant, *T* is temperature in Kelvin, *h* is Planck's constant, and *m is the effective mass of electrons (holes) in the conduction (valence) band.**

$$N_X = 2\left(\frac{2\pi m_x^* kT}{h^2}\right)^{3/2}$$

The second desirable property rising from a wide bandgap, namely a high critical field strength, E_C, is less formalized in theory, but is empirically evident in Figure 2. As the bandgap becomes wider, carriers are less likely to achieve the energy necessary to contribute to conduction when impacted by other free carriers with high kinetic energy. This leads to a lower probability of impact ionization and a reduced possibility of device failure (i.e. loss of semiconducting property at high field) from this mechanism. Impact ionization is not the only mechanism leading to failures at high field; however, as seen in Figure 2 empirically a wider bandgap does equate to a higher critical field strength. Debate remains, however, over the methods to construct empirical fits. As can be seen in Figure 3 using data and methods from [2], limited data for devices with high critical fields can lead to imprecision in assessing the critical field based on the bandgap alone. From all empirical indications, however, gallium oxide should have a higher critical field strength than other wide bandgap semiconductors with the possible exception of diamond and aluminum nitride. Additionally, preliminary full band Monte Carlo (FBMC) simulations of β-Ga_2O_3 (specifics of the β-polymorph will be described in Chapter 2)

considering impact ionization through electron-electron interactions (EEI) predicted a critical field higher than the 8 MV/cm predicted empirically [3]. This study ignored important possibilities that affect the breakdown such as band-to-band tunneling, but nevertheless, represents another data point showing the high breakdown field predicted for Ga_2O_3. The critical field strength and implications will be further analyzed in chapter 2.

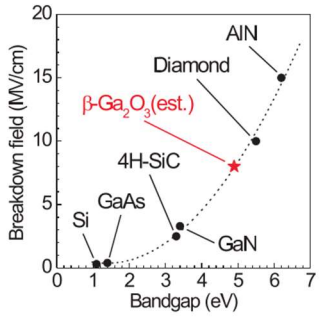


Figure 2 Empirical relationship between bandgap and critical field strength. The dotted line is drawn by eye. Reprinted from[4], with the permission of AIP Publishing. Only diamond and aluminum nitride (AlN) breakdown fields are greater than that of gallium oxide.

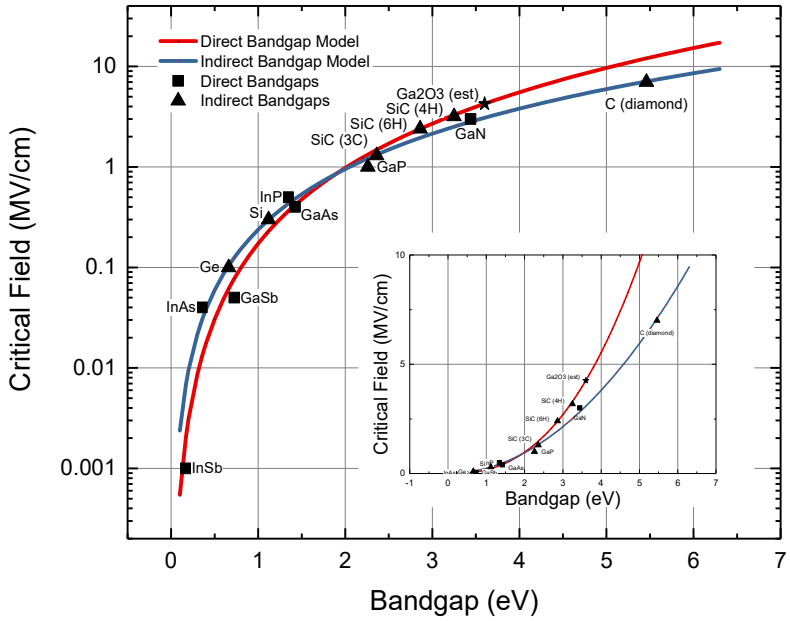


Figure 3 Critical field versus bandgap modeled empirically as in [2]. Measured values are included for direct (squares) and indirect (triangles) bandgap semiconductors. An estimate of the critical field of gallium oxide is also shown with a star. The inset shows a linear scale plot of the same highlighting the exponential nature of the empirical fit which can lead to large discrepancy in the estimates as the field strength increases.

Power Applications and Figures of Merit

Power semiconductor devices can be defined as any discrete or integrated device delivering more than 1 Watt to an electrical load, but often the definition is widened to include devices operating at any voltage >30 V [5]. The power semiconductor market includes these devices and the packaging and infrastructure required for them. This market was valued in 2015 at over $34B [6]. These numbers include wide bandgap semiconductor devices and silicon power devices as well as necessary passive devices used in applications ranging from wireless cell phone systems and laptop computers to magnetic levitation (Maglev) trains and power grid transmission [5]. The portion of this market dedicated to radio frequency (RF) power semiconductors, a $10B portion, is estimated to grow to >$31B alone by 2022 [7]. Growth in these markets is often related

to system integration of high power components with other electronic components such as memory and logic circuits [6]. Integrated systems require increases in the efficiency of the power semiconductor components to achieve relevance in the market. Additionally, efficiency is a must for smart grid and clean energy technologies or their advantages can be dulled. Finally, the military needs more efficient systems to reduce cost and increase range and lifetimes.

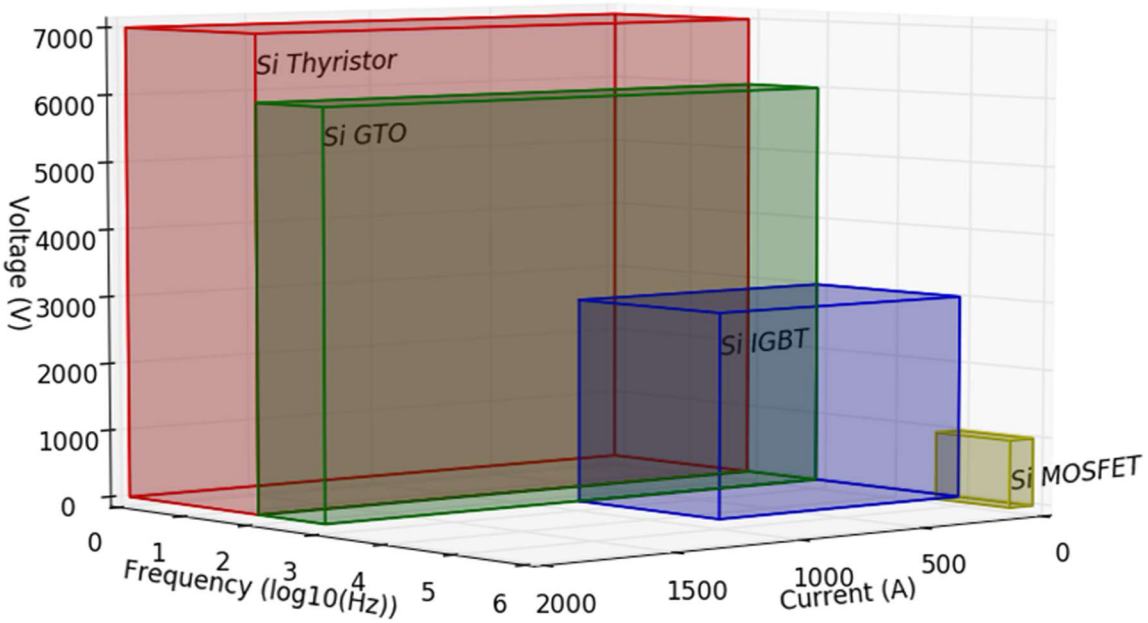


Figure 4 Silicon power devices, the thyristor, the gated thyristor (GTO), the insulated gate bipolar transistor (IGBT), and the metal oxide semiconductor field effect transistor (MOSFET, showing on the three axes the maximum operating voltage, current, and frequency that each type of device can achieve. Adapted from https://en.wikipedia.org/wiki/Power_semiconductor_device.

To quickly illustrate the advantages that can be gained through new power semiconductor devices, we present the silicon power semiconductor devices in Figure 4 with their maximum operating current, voltage, and frequency. Expanding the rectangular

box along the *y* (frequency) or *z* (voltage) axis, as has been done by introducing different silicon technologies seen in Figure 4, can offer advantages in size or efficiency of a component. For instance, increasing the operating frequency of a power converter reduces the size of the passive components-which reduce in proportion to the wavelength (Equation 4)-needed in the power conversion circuitry. This reduces the size of the power converter and can even allow the passives to be integrated on the same chip. Similarly, increasing the operating voltage can reduce the resistive losses or the size and weight of the cables required to operate a system at a given power level. For example, a 500 W device powered through a 1 meter cable with a resistivity of 10 Ω-m and surface area of 1 m^2 would have cable losses of 250 W and 10 W when operating at 100 V and 500 V, respectively using Equation 5. This advantage is evident in the United States power grid which uses high voltage lines for long distance transfer to reduce losses. For data centers and supercomputers, this problem is further exacerbated by the heat dissipated by the cables, making it more cost effective to operate facilities at high voltage to reduce environmental control costs. Alternatively, according to Equation 5, the surface area, *A*, of the cable could be increased to reduce the resistivity, but this cannot be done arbitrarily because of surface effects and is not realistic-especially for military and space applications-because size and weight of cables will also dramatically increase.

Equation 4 Wavelength of a sinusoidal waveform traveling at velocity, *v*, with frequency, *f*. For any electromagnetic radiation *v*=*c* where *c* is the speed of light.

$$\lambda = \frac{v}{f}$$

Equation 5 Power equation showing the power dropped over a resistive load such as a cable. *I* is the current flowing through the load, *R* is the total resistance, ρ is the resistivity of the material, *l* is the length of the material, and *A* is the cross sectional surface area of the material.

$$P_{loss} = I^2R = I^2\rho\frac{l}{A}$$

The specific advantage of expanding the rectangular box in Figure 4 in the x direction is to increase the power delivered to the load once voltage is already at a limit and to increase the current handling capability of the device should a failure mode occur. As such current is usually scaled last by increasing the area as will be discussed further below; however, it becomes an important factor for manufacturability if the area cannot arbitrarily be increased to the level of current required for a given application. This issue and more specifics of existing power semiconductor device technologies will be described at the end of Chapter 3, and we will revisit Figure 4 in Chapter 8 to describe some potential market directions for Ga_2O_3. For now, we describe the specifications used to assess direct current (DC) and RF power semiconductor devices, and we reduce these specifications to some key figures of merit for the assessment of different semiconductors for power semiconductor applications. We use these figures of merit throughout to describe the potential of Ga_2O_3 as a power semiconductor and to determine progress in the development of Ga_2O_3 devices.

Equation 6 Power dissipation of a DC or RF switching device. I_{rms} is the root-mean-square current, R_{ON} is the on-resistance, C_{IN} is the input capacitance, V_G is the applied gate voltage, f is the operating frequency, and A is the device area. $R_{ON,sp}$ and $C_{IN,sp}$ are the specific on-resistance and input capacitance respectively. From [8].

$$P_{loss} = I_{rms}^2 R_{ON} + C_{IN} V_G^2 f = \underbrace{I_{rms}^2 \frac{R_{ON,sp}}{A}}_{Conduction\ loss} + \underbrace{C_{IN,sp} A V_G^2 f}_{Dynamic\ Switching\ loss}$$

Efficiency is of utmost importance for power semiconductor devices whether operating at high frequency or in direct current (DC) mode. As such, other than biasing information and current and voltage ratings, power semiconductor device specifications include some form of power dissipation information. For high frequency devices, this is likely to be in the form of drain efficiency or other types of power efficiency [9], [10], and for low frequency or DC switch devices this is often in the form of on-resistance [11], [12]. The power dissipation of a switching device can be easily found as described by Baliga [8] and shown in Equation 6. The first term accounts for the conduction losses, and the second term accounts for the charging and discharging of the input capacitor. For low frequency switching, the DC conduction loss dominates, and the second term in Equation 6 is often ignored. As the switching frequency increases, the dynamic losses become significant or even dominant and both terms should be used. Thus as Baliga noted for DC or low frequency switches the specific on resistance, $R_{ON,sp}$, should be minimized and for high frequency operation the $R_{ON,sp}$-$C_{IN,sp}$ product should be minimized [8]. Because of this, specifications for power semiconductor devices often contain some form of $R_{ON,sp}$ or the on-resistance, R_{ON}, and the switching capacitances, the gate charge required to turn the device on, Q_G, or both [9]–[13].

Being in the development stage of Ga_2O_3, it is beneficial to have a way to assess the material properties of Ga_2O_3 versus other power semiconductor materials without creating finally optimized devices. To do exactly this, Baliga assumes an ideal abrupt one-dimensional semiconductor junction and uses the depletion approximation to determine a figure of merit that can be calculated using material properties of different semiconductors to assess their viability in high frequency and DC switch technologies given equally optimized device structures [8]. Baliga's figure of merit is shown in Equation 9 for DC and RF power switching devices, and an example of the simplified junction and calculations used are shown in Figure 5 and Equation 7 and Equation 8, respectively. A higher figure of merit indicates reduced power loss in the power semiconductor when used as a DC or RF switch.

Equation 7 The specific on resistance of an arbitrary semiconductor material at a given breakdown voltage. E_C, the critical field strength; μ, the effective mobility of the minority carriers; and ϵ_S, the dielectric constant are the material parameters. V_B is the breakdown voltage, W_B is the maximum depletion width, N_B is the maximum doping concentration, q is the electron charge, l is the length of the resistive layer, and σ is the conductance of the material [8].

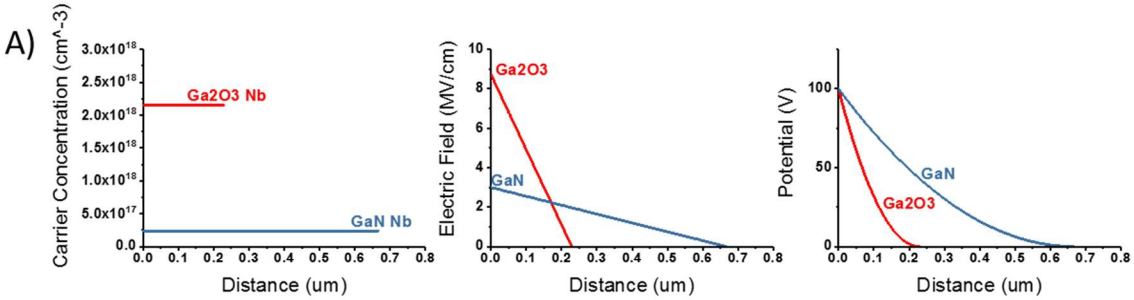
$$R_{ON,sp} = \frac{1}{\sigma} l = \frac{1}{N_B q \mu} W_B = \frac{4V_B^2}{\epsilon_s E_C^3 \mu}$$

Equation 8 The specific input capacitance of an arbitrary semiconductor material at a given breakdown voltage. E_C, the critical field strength and ϵ_S, the dielectric constant are the material parameters. V_B is the breakdown voltage, W_D is the gate depletion width, N_B is the maximum doping concentration, q is the electron charge, and V_G is the applied gate voltage [8].

$$C_{IN,sp} = \frac{\epsilon_s}{W_D} = \frac{\epsilon_s E_C}{2V_G} = \sqrt{\frac{N_B q \epsilon_s}{2V_G}} = \frac{\epsilon_s E_C}{2\sqrt{V_G V_B}}$$

Equation 9 Baliga's figure of merit for high-frequency switches calculated from an arbitrary semiconductor material at a given breakdown voltage. The Baliga's figure of merit for DC switches is also highlighted. E_C, the critical field strength; μ, the effective mobility of the minority carriers; and ϵ_S, the dielectric constant are the material parameters. V_B is the breakdown voltage, V_G is the gate voltage, and $R_{ON,sp}$ and $C_{IN,sp}$ are the specific on resistance and specific input capacitance, respectively [8].

$$BHFFOM = \frac{1}{R_{ON,sp}C_{IN,sp}} = \underbrace{\frac{\epsilon_s E_C^3 \mu}{4V_B^2}}_{BFOM\ for\ DC} \cdot \frac{2\sqrt{V_G V_B}}{\epsilon_s E_C} = \frac{E_C^2 \mu V_G^{0.5}}{2V_B^{1.5}}$$



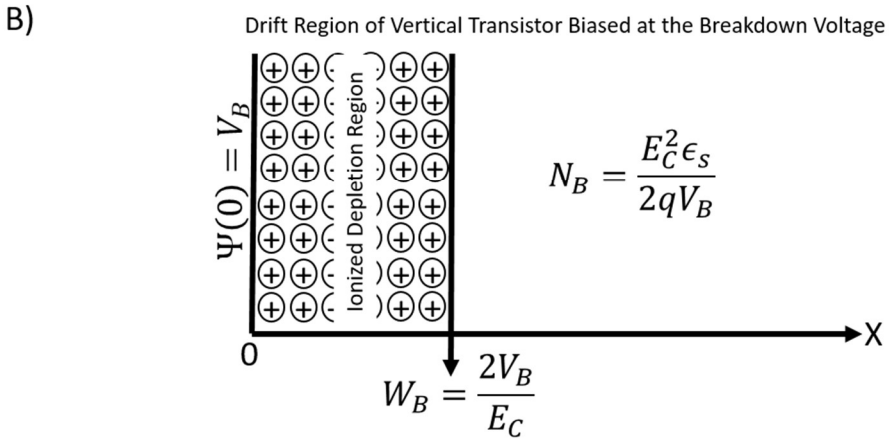


Figure 5 (A) Solution to Poisson's equation for a GaN and Ga_2O_3 vertical junction as shown in (B) with a breakdown voltage of 100 V. The high critical field of Ga_2O_3 allows for a higher doping concentration and a shorter depletion distance leading to lower conduction loss for an ideal switch in the Ga_2O_3 material system as described by Baliga [8]. N_B is the maximum doping concentration for the drift region, V_B is the breakdown voltage (chosen as 100 V), W_B is the width of the depletion region, E_C is the critical field strength of the material, ϵ_S the dielectric constant of the material, $\Psi(0)$ the potential at the surface, and q the electron charge.

While the BFOM does an excellent job in comparing different material systems for high frequency and DC switch losses, it does not assess the frequency range of RF power devices. RF power devices have another important specification which involves the ability to deliver power to a load at a given frequency. This can be described by a power-frequency product which describes the amount of power that can be delivered at a given frequency for a given device. To assess the potential power-frequency product of materials without developing optimized devices, Johnson noted that the maximum frequency of operation that a device can obtain is related to the maximum velocity of electrons in the material, v_{sat}, and the minimum gate length as in ref [14]. He also noted that the minimum gate length, L_{Gmin}, is obtained when the lateral field along the gate length is equal to the critical field, E_C as in Equation 10. Finally, manipulating these equations, he obtained the Johnson's figure of merit (JFOM) (Equation 11) which describes the power-frequency product of a given semiconductor material from its material properties only [14]. We note that the JFOM has units of voltage multiplied by frequency, ignoring current. In the calculation, it has been assumed that current is only limited by the area of the device and can thus be equalized for the different semiconductors by increasing or decreasing the total area.

Equation 10 Transition frequency of an arbitrary field effect transistor. τ is the gate transit time, v_{sat} is the saturation velocity, L_{Gmin} is the minimum gate length, E_C is the critical electric field strength of the material, and V_B is a given breakdown voltage.

$$f_T = \frac{1}{2\pi\tau} = \frac{v_{sat}}{2\pi L_{Gmin}} = \frac{E_C v_{sat}}{2\pi V_B}$$

Equation 11 Johnson's figure of merit for an arbitrary semiconductor material with material parameters, E_C, the critical field strength and v_{sat}, the saturation velocity. The figure of merit represents the transition frequency, f_T, breakdown voltage, V_B, product, and it can be used to assess the maximum electrical power that can be delivered to a load at a given frequency in the material system.

$$JFOM = f_T V_B = \frac{E_C v_{sat}}{2\pi}$$

The Johnson and Baliga figures of merit have many limitations as will become evident in the discussion of specific device technologies in Chapter 3, but during the initial development of a new semiconductor, they are important to assess the material properties against other competing technologies in the field. This comparison will be done at the end of Chapter 2, but first we need to understand the material properties of Ga_2O_3.

Dissertation Layout

The rest of this dissertation is laid out as follows. Chapter 2 provides further materials background needed to understand the material advantages offered by gallium oxide and compares the material properties of gallium oxide to other important power semiconductors. Chapter 3 reviews wide bandgap semiconductor devices specifically focusing on existing research using gallium oxide field effect transistors. Chapter 4 provides a brief background of semiconductor device modeling and introduces a simple model based on semiconductor device theory for gallium oxide field effect transistors. Chapter 5 provides details on fabrication and testing of gallium oxide MOSFETs used to verify the analytical model developed in Chapter 4. Chapter 6 further analyzes the applicability of the device model including limitations of extending the model due to

immaturity of the material infrastructure for gallium oxide and analysis of model implications for device design trades. Chapter 7 presents future development possibilities for gallium oxide devices. Chapter 8 concludes the dissertation with a summary of the gallium oxide research performed and general progress for this material system.

2. GALLIUM OXIDE MATERIAL BACKGROUND

The potential of gallium oxide as a new material for the power semiconductor and RF switching markets begins with its unique material properties. In this chapter, we describe the crystal structure of gallium oxide and describe some of the implications of that structure as compared to other power semiconductor materials. We describe some state of the art results from the literature on the growth and doping of gallium oxide needed for electron devices, and we conclude with a comparison of the material properties of gallium oxide compared to other wide bandgap semiconductor materials.

Gallium Oxide Polymorphs

Gallium oxide which forms in the ionic compound, Ga_2O_3, was first noted in the literature in 1875 when the compounds of gallium were briefly mentioned by Lecoq de Boisbaudran as part of an investigation into the newly discovered element gallium [15]. Other than additional material studies, in the twentieth century Ga_2O_3 was investigated for applications ranging from MASER materials to transparent conductive coatings to electroluminescence devices [16]. Currently, Ga_2O_3 is still being evaluated in gas sensors particularly for high temperature oxygen sensing [17] and electro-optical devices such as solar-blind photodiodes [18]. Only recently, has Ga_2O_3 been sought for power semiconductor devices-with perhaps the first mention of this possibility from the Tokyo Institute of Technology's paper in 2006 [19]-which makes it essentially a newcomer to

this research area. It is this potential for power semiconductors and the entirely new possibility of RF switching that are the focus of this dissertation.

Ga_2O_3 is often placed in the category of transparent conductive oxides (TCOs) along with the oxides of Zn or oxides of the metal combinations of Ga, In, and Zn (i.e. InGaZnO or IGZO) because of its similar transparency and wide bandgap. These materials are closely related to transparent conductive oxides such as tin-doped indium oxide (ITO) which are commonly used as front contacts in displays, touch screens, and solar cells [20]; however, the IGZO family has the added semiconducting property that allows conductivity to be controlled at room temperature through applied potentials. Because of this conductivity control, ZnO and IGZO are being developed for improved display technology over the incumbent amorphous-Si transparent thin film transistors (TTFT) and for making completely transparent displays a reality. Ga_2O_3, however, is not desired for display technology because it is an insulator in amorphous form unlike ZnO and IGZO which can be used like TCOs in the more cost effectively deposited polycrystalline or amorphous forms with the added benefit of full transistor function. Ga_2O_3 is only useful, therefore, in the more expensive crystalline form. Thus, Ga_2O_3 has been ignored for display technology and has only recently emerged as potential material for electro-optic, gas sensing, and of course, power semiconductor devices.

Five different crystal polymorphs of Ga_2O_3 have been investigated in the literature [21]. β-Ga_2O_3 is the primary polymorph that will be considered in this work because it is the most stable and is the most likely polymorph to see widespread use in future power semiconductor and RF switch devices. α-Ga_2O_3 has been identified as

having a potentially wider bandgap than the β polymorph [22]; however, this polymorph is unstable and converts to β-Ga_2O_3 at the high temperatures required for material growth. While they have been identified, γ-Ga_2O_3, δ-Ga_2O_3, and ε-Ga_2O_3 are also metastable [23]. Even though some effort has been made to grow material using ε-Ga_2O_3 [24][25] for its high crystal symmetry and potential advantages in nitride hetero-epitaxy, α-Ga_2O_3 [26][27] for its wider bandgap, and γ-Ga_2O_3 [28]for spintronic applications at room temperature, interest in these polymorphs is very limited for semiconductor devices which require stability at various temperatures during material growth and fabrication processes as will be discussed later. Figure 6 shows results of a 1952 study on the transformations of the different polymorphs of Ga_2O_3 with the β-Ga_2O_3 polymorph being the most stable [23]. A more recent version from 2013 is presented in [29] and shown in Figure 7 which removes δ-Ga_2O_3 from the polymorphs (now believed to be nanocrystalline ε-Ga_2O_3 and not its own unique polymorph) and adds the transition polymorph κ-Ga_2O_3. Additionally, Table 1 summarizes the different polymorphs including crystal structure and bandgap if it has been determined. Table 2 shows the crystal structures of some other important materials that may compete with or be used with Ga_2O_3. In both tables, the lattice constants and number of symmetry operators for the crystal structure are shown. The lattice constants can be used to indicate the lattice match with Ga_2O_3, and the symmetry operators indicate the simplicity of the crystal for physics based modeling. Both of these will be discussed further below.

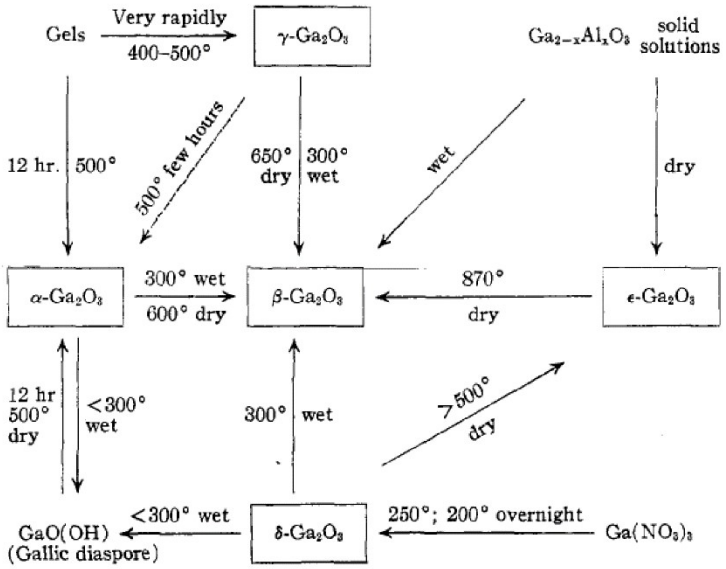


Figure 6 Transformation relationships of Ga_2O_3 and its hydrates. Reprinted with permission from [23]. Copyright 1952 American Chemical Society.

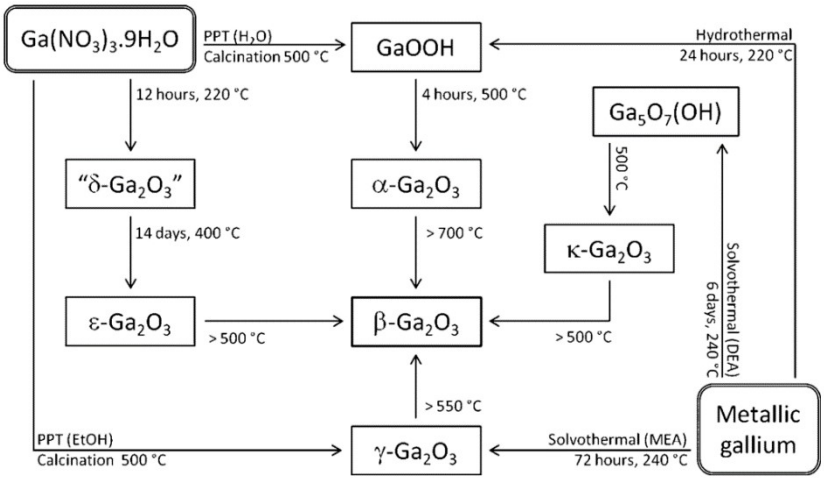


Figure 7 Summary of the synthesis and interconversion of the polymorphs of Ga_2O_3 and related phases. Note that "δ-Ga_2O_3 " is a nanocrystalline form of ε-Ga_2O_3 and κ-Ga_2O_3 is a transient phase, not isolated as a phase-pure sample. PPT=precipitate, DEA=diethanolamine and MEA=monoethanolamine. Reprinted with permission from [29] copyright John Wiley and Sons.

Table 1 Sumary of the different crystal polymorphs of Ga_2O_3 and their known material properties.

Polymorph	Crystal Structure (symmetry operators)	Known Properties
α-Ga_2O_3	Trigonal-Corundum (6) [30]	E_G= ~5.0-5.3 eV [22][31]
β-Ga_2O_3	Monoclinic (8) [32]	E_G= 4.6-4.9 eV
γ-Ga_2O_3	Cubic-Defective Spinel (192)[29]	
δ-Ga_2O_3	Bixbyite (no longer unique polymorph)	
ε-Ga_2O_3	Hexagonal (12) [29]	E_G=4.9 eV [25]
κ-Ga_2O_3	Hexagonal (12) [29]	

Table 2 Basic crystal structures of important power semiconductor materials.

Material	Crystal Structure (symmetry operators)	Lattice constants (@300K)
4H SiC [33]	Hexagonal (12)	a=0.31 nm, c=1.0 nm
6H SiC [33]	Hexagonal (12)	a=0.31 nm, c=1.51 nm
Si [1]	Diamond Cubic (192)	a=0.54 nm
GaN [34]	Hexagonal – Wurtzite (12)	a=0.33 nm, c=0.52 nm
AlN [34]	Hexagonal – Wurtzite (12)	a=0.31 nm, c=0.50 nm
GaAs [35]	Zinc Blende Cubic (96)	a=0.57
Diamond [36]	Diamond Cubic	a=0.36

β-Ga_2O_3 Material Properties

Since it is the most stable form and native substrates can be produced efficiently, β-Ga_2O_3 has been the primary focus of materials research and devices aimed at creating market share in the power semiconductor and RF switching market, as such, this particular polymorph will be the focus of this dissertation. The specifics of the crystal structure of β-Ga_2O_3 are under evaluation to determine material, electrical, and transport

properties needed for incorporation into power semiconductor and RF switching models. The results, so far, are summarized in this section.

The unit cell of β-Ga_2O_3 was first reported in 1957 by Kohn, Katz, and Broder [37], and it has been only slightly refined since then to the accepted base centered monoclinic crystal structure with a= 1.22 nm, b= 0.30 nm, c= 0.58 nm, and β= 103.8 degrees. X-ray diffraction crystallography was used by Geller in 1960 [38] and again with increased precision by Ahman, Svensson, and Albertsson in 1996 [32] to determine the specific crystal structure of β-Ga_2O_3 which belongs to space group *C2/m* with 8 symmetry operators. The unit cell shown in Figure 8 has four formula units. Ga^{3+} is found in both octahedral (6 neighboring oxygen atoms, i.e. 6-fold) and tetrahedral (4 neighboring oxygen atoms, i.e. 4-fold) coordination in the crystal lattice which becomes important in the discussion of doping later in this chapter and in Chapter 3. The oxygen atoms appear in three inequivalent sites; however, this information is thus far less critical to determining the material properties compared to the gallium coordination.

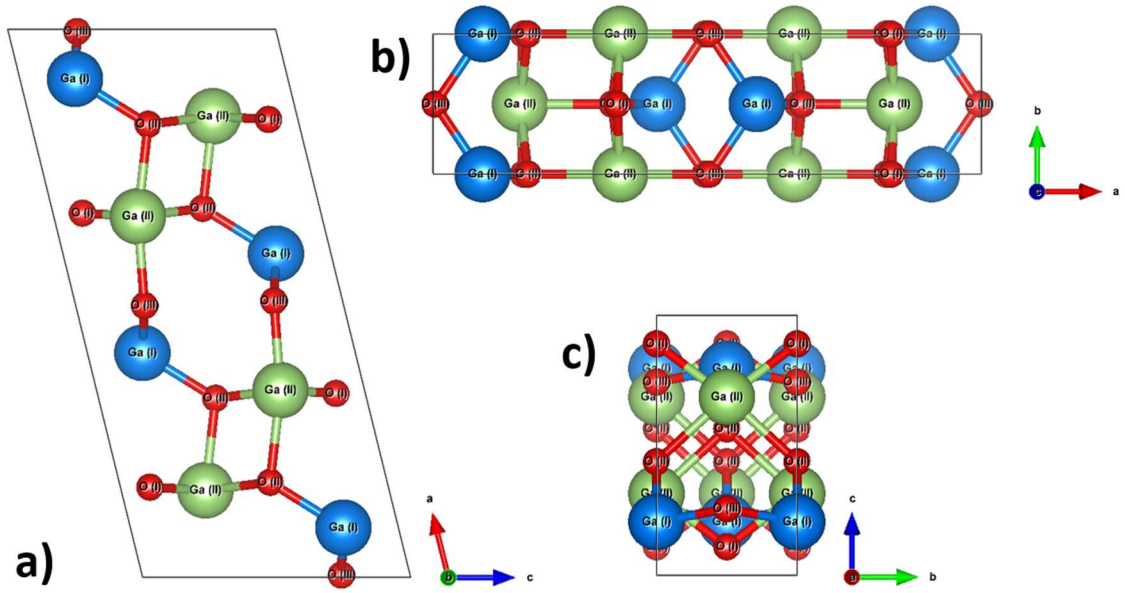


Figure 8 Beta Gallium Oxide unit cell. a) b-plane surface. b) c-plane surface. c) a-plane surface. Graphic was created from [32] using the VESTA program [39]. 4-fold coordinated (blue) and 6-fold coordinated (green) Gallium atoms are shown in different color for clarity. Atoms are sized by atomic radius.

Immaturity in single crystal and thin film preparation, difficulty in using accepted measurement techniques due to the wide bandgap, and the complexity of the crystal structure delayed information on the electronic structure of β-Ga_2O_3 until only recently [40]. In 2006, all electron density functional theory (DFT) in the framework of the linear combination of atomic orbitals was used to calculate a bandgap of 4.69 eV and 4.66 eV for direct and indirect bandgaps of zero pressure bulk β-Ga_2O_3, respectively [22]. An electron effective mass, m_e^*/m_0, of 0.342 was also reported [22]. These early bandgap values were markedly lower than experimental values obtained from single crystal thin films of 4.9 eV and 4.85 eV for direct and indirect bandgaps, respectively, obtained by angular resolved photoemission spectroscopy [41]. A lower electron effective mass, m_e^*/m_0, of 0.28 was also reported [41]. It is clear in [42] where a bandgap of 4.65 eV and

4.7 eV where measured for un-doped and Sn-doped β-Ga_2O_3 single crystals, respectively, that different modeling methods, layer thicknesses, and doping levels can yield slightly different results related to the electronic structure. Thus, in the rest of this work, we use an estimated value of 4.80 eV for the bandgap and 0.28 for the electron effective mass which are generally accepted values used currently in the community [16]. Important aspects of the energy bands from experiment and hybrid functional DFT including the direct and indirect bandgap are shown in Figure 9. It can also be seen in Figure 9 that the valence band is nearly flat leading to a very high effective mass of holes, m_h^*/m_0 = ~40, as described in ref [43]. This limits the potential for p-type conduction in β-Ga_2O_3 which clearly limits the potential for complementary devices; however, the same authors predicted a much lower hole mass, m_h^*/m_0 = ~0.40 in a different direction which has not yet been further analyzed.

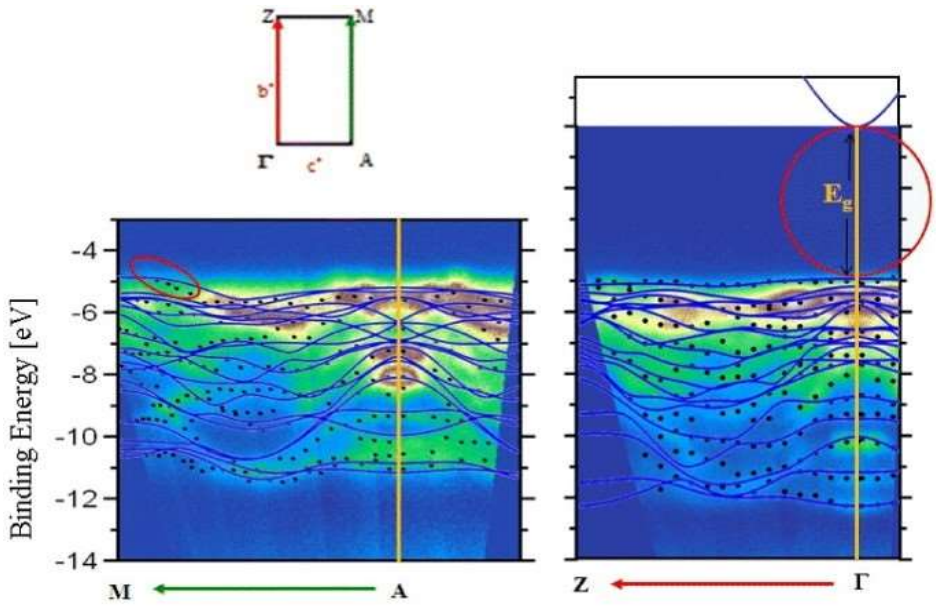


Figure 9 Top: BZ directions for Ga_2O_3 parallel to the cleavage plane. Bottom: experimental band structure of β-Ga_2O_3 along the A–M (left) and Γ–Z (b∗) (right) directions of the BZ. The experimental bands derived from a fitting procedure to the spectra are shown by black dots. Calculated band structures based on density functional theory using a hybrid functional are shown as blue lines on the experimental band structure for comparison. The red marked areas highlight the regions of the direct and indirect gaps. Reproduced from [41] under IOPScience open access Creative Commons policy https://creativecommons.org/licenses/by/3.0/. Available through open access at http://iopscience.iop.org/article/10.1088/1367-2630/13/8/085014/meta.

The monoclinic crystal structure of β-Ga_2O_3 also leads to difficulty in physics based modeling of thermal and transport properties. Low symmetry materials like β-Ga_2O_3 have a large Brillouin zone, low degeneracy of phonon modes and associated electron-phonon interaction (EPI) elements, and dependence on crystal orientation for dielectric tensor and long range EPI [44] which makes first-principles calculations complex. The thermal conductivity of β-Ga_2O_3 is accepted to be both poor compared to GaN (~110 W/mK [2]) or SiC (~700 W/mK [2]) and anisotropic with room temperature values of ~21.0 W/m·K in the [010] direction and ~13 W/m·K in the [100] direction obtained from first principles calculations [45]. Using the time domain thermal

reflectance (TDTR) method the values at room temperature were verified to be ~27.0 W/m·K and ~10.9 W/m·K in the [010] and [100] directions, respectively [46]. The measured and calculated thermal conductivities show a 1/T dependence at high temperature indicating phonon dominated thermal transport as shown in Figure 10. This remains the case until the doping level reaches values >10^{19} cm^{-3} when mobile electron thermal transport may become a factor [46]. In the devices investigated here, the thermal conductivity is important at temperatures above room temperature, and below doping levels of 10^{19} cm^{-3} therefore additional operating domains will not be further discussed.

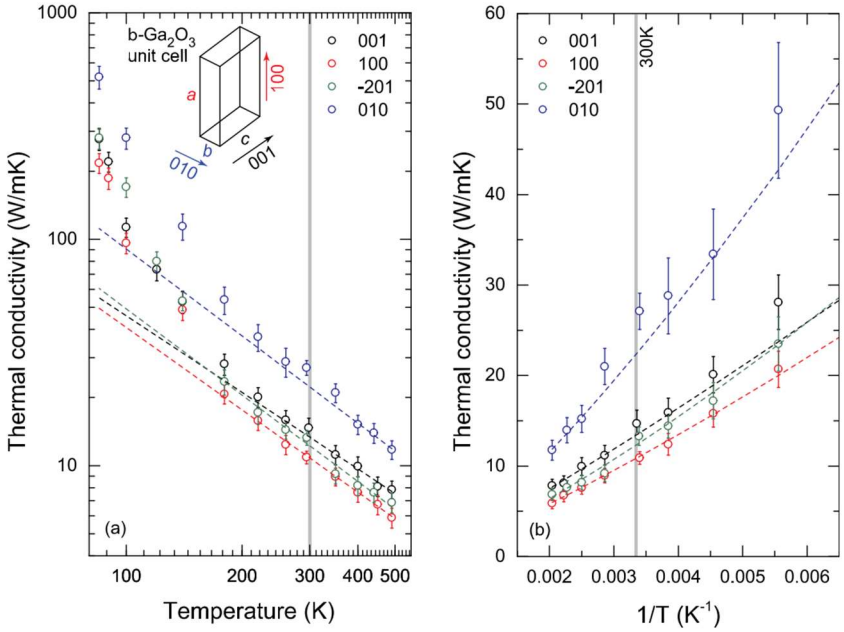


Figure 10 Temperature-dependent thermal conductivity of β-Ga_2O_3 measured along different crystal directions by the time domain thermal reflectance (TDTR) approach. In (a), the thermal conductivity and temperature are in the log scale. The inset shows a schematic of the unit cell of the β-Ga_2O_3 crystal. The thermal conductivity is larger along directions of smaller lattice constant: The rough lattice constant ratios are c~2b and a~4b. The dashed lines show $1/T^m$ fits that capture the high-temperature behavior of the thermal conductivity. The vertical dashed line separates the high-temperature behavior from the lower-temperature deviation to the fits. (b) Shows a linear plot of thermal conductivity against 1/T to highlight the dependence on temperature and the high-temperature $1/T^m$ fits more clearly. Reprinted from [46], with the permission of AIP Publishing.

Low field bulk mobility was originally extrapolated from Sn-doped molecular beam epitaxy (MBE) material to be as high as 300 $cm^2/V{\cdot}s$ at room temperature for very low doping levels [47]. Ghosh and Singisetti used an *ab initio* study to calculate EPI values for the 30 phonon modes resulting from the large primitive cell in β-Ga_2O_3. They concluded that the polar optical (PO) phonon mode dominated the low field mobility at room temperature leading to a value of 115 $cm^2/V{\cdot}s$ for $1.1x10^{17}$ cm^{-3} modeled carrier concentration [48]. Even more recently, empirical data and a relaxation time approximation of the Boltzmann transport equation have been used to predict a value of 110-150 $cm^2/V{\cdot}s$ at room temperature [49]. In [49], the authors credit a much stronger EPI for polar-optical (PO) phonons (i.e. Fröhlich coupling constant) in β-Ga_2O_3 for the much lower bulk mobility when compared to GaN (~1500 $cm^2/V{\cdot}s$) which has similar effective mass. As shown in Figure 11, the authors predict a critical doping concentration level, N_{cr}, where ionized impurity begins to dominate PO phonon interaction to be around $2.8x10^{18}$ cm^{-3} [49]. The modeled values agree well with an experimentally measured highest room temperature mobility of 153 $cm^2/V{\cdot}s$ [50] for UID bulk single crystals with $(\bar{2}01)$ surface plane. The temperature dependent mobility predicted from several important scattering mechanisms is shown in Figure 12, and as with thermal conductivity, the low temperature mobility is not a large concern for the devices reported in this work which operate at or above room temperature. Originally, large anisotropy in the transport characteristics of β-Ga_2O_3 were reported experimentally with an order of magnitude difference in mobility between the **b** and **c** lattice directions [51]; however, more recent experimental data indicates errors in this result [52] [53]. The transport properties of β-

Ga_2O_3 are now believed to be nearly isotropic which agrees with the parabolic (spherical at the bottom) conduction band minimum and extracted electron effective masses presented previously [54].

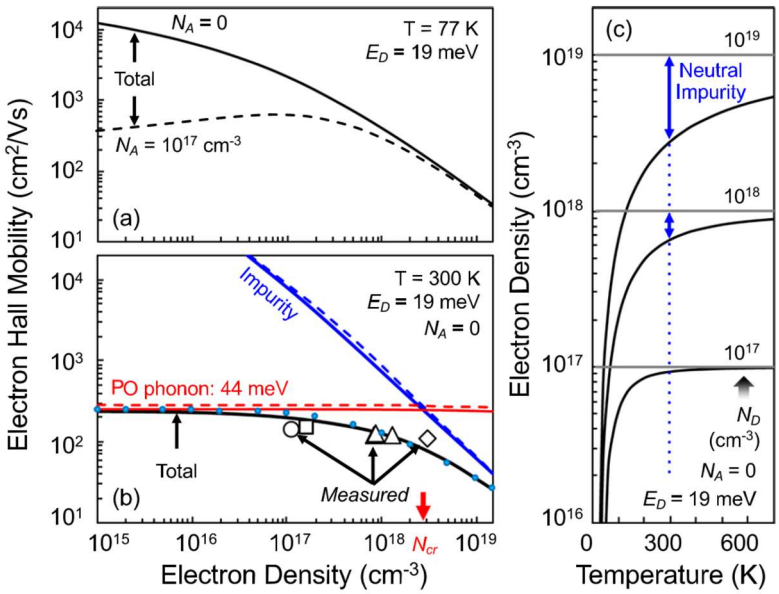


Figure 11 Electron mobilities as a function of donor concentration at (a) 77K and (b) 300 K. The symbols show experimental results from different groups: circle[55], triangle [56], square [50], and diamond [57]. (c) Electron density as a function of temperature with different donor concentrations. Reprinted from [49] with permission from AIP publishing.

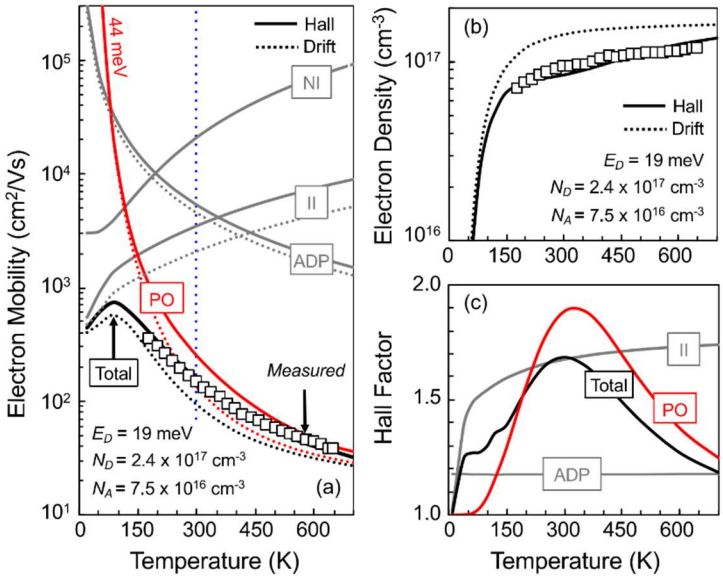


Figure 12 Temperature-dependent (a) electron mobility, (b) electron density, and (c) Hall factors in β–Ga_2O_3. The solid and dashed lines in (a) and (b) indicate Hall and drift electron mobilities (densities), respectively. The open squares indicate experimental results obtained using Hall-effect measurements. Reprinted from [49] with the permission of AIP publishing.

High field transport has not been largely evaluated because of difficulty in simulation with the low symmetry crystal; however, recent results from full band Monte Carlo simulations indicate a saturation velocity of around 2.0x10^7 cm/s at a field of 200 kV/cm [58]. In our group using similar methods, initial unpublished estimates shown in Figure 13 indicate a saturation velocity of ~1.1x10^7 cm/s for moderately doped β-Ga_2O_3 also occurring around 200 kV/cm. Experimental values of the saturation velocity are also difficult to obtain as will be discussed in Chapter 7.

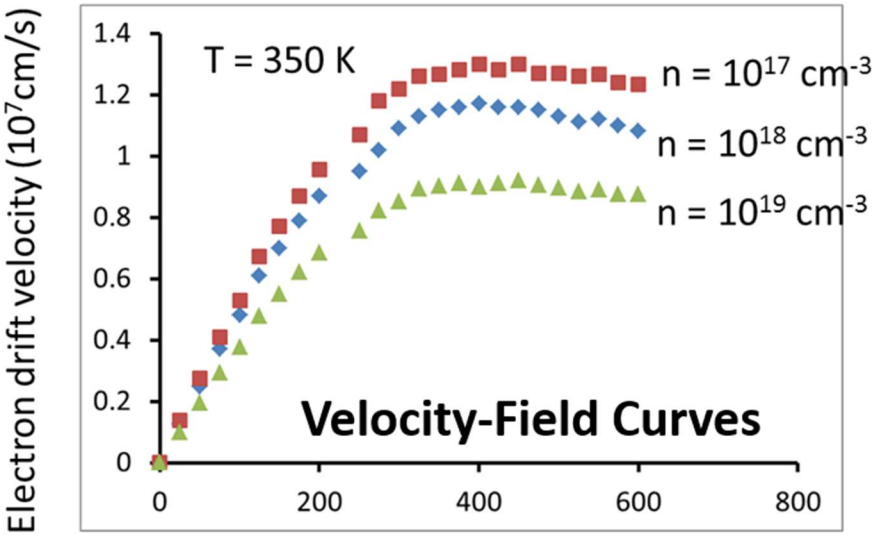


Figure 13 Full band Monte Carlo simulation of the high field transport properties of β-Ga_2O_3. The simulations include all phonon modes and charged impurity scattering. Results are unpublished. The horizontal scale is the field in kV/cm. Courtesy of S. Badescu. Contact: catalin.badescu.1@us.af.mil

Substrate Growth

The advantage of choosing β-Ga_2O_3 over the other polymorphs of Ga_2O_3 primarily lies in the ability to produce low defect density native substrates through simple, inexpensive melt growth techniques. This also provides significant advantages over other power semiconductors (GaN, SiC, and diamond) which cannot be grown efficiently in bulk, and thus, lack inexpensive defect free native substrates. In fact, β-Ga_2O_3 is the only semiconductor with a bandgap greater than 3 eV that can be grown efficiently from the melt. Minimizing defects in power semiconductor and RF switch materials is important because the devices often require large areas for high voltage, high current, or high power operation. Native substrates avoid defects related to lattice mismatch between different substrate and epitaxial materials leading to significant

advantages in performance and device yield. Additionally, vertical devices require high quality substrates as part of the conduction path vertically through the device. For β-Ga_2O_3, several melt growth techniques have been demonstrated including the edge-defined, film fed growth method (EFG) [59]; floating zone (FZ) method [53]; and the Czochralski (CZ) method [60] each of which can be used to produce large single crystal substrates from molten Ga_2O_3 (~1820 ºC [60]). Substrate growth is summarized in Figure 14.

Despite the tremendous promise of defect free, native substrates from melt growth, many engineering challenges still exist with each of these methods. The CZ method is currently limited by the high melting point of β-Ga_2O_3 which can affect the iridium crucible used in this method and the ability to achieve large diameter substrates. Additionally, the growth direction for all methods can be affected by (100) and (001) cleavage planes associated with the O(III) and O(I) bonds in the crystal lattice, respectively (see Figure 8) [53]. Finally, the EFG method, which may be the least limited by high temperature and growth direction, has an inherent limit to the thickness of the substrate that can be grown. Each of these issues is currently under investigation as the desire for β-Ga_2O_3 native substrates grows.

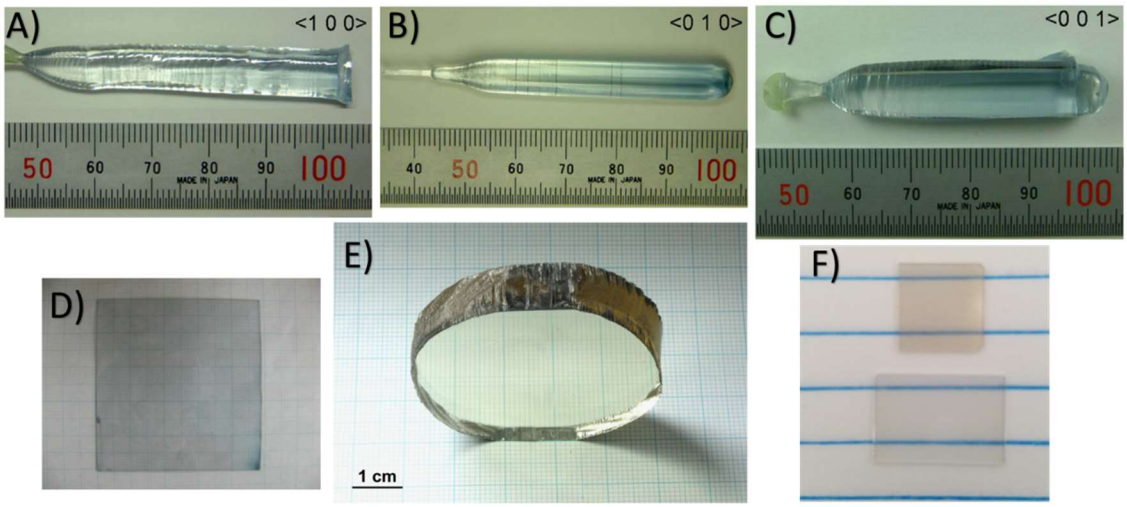


Figure 14 A pictorial summary of substrate growth of β-Ga_2O_3. A), B), and C) are single crystal boules as grown by the floating zone (FZ) method along the crystallographic axis <100>, <010>, and <001>, respectively. Used with permission from [53]. Copyright 2004 by Elsevier. D) β-Ga_2O_3 wafer substrate grown by the edge-defined film fed growth (EFG) method after polishing (48x50x0:5 mm^3). Used with permission from [59]. E) Two inch diameter and 1 cm thick β-Ga_2O_3 crystal slab prepared from the bulk crystal doped with Mg grown by the Czochralski (CZ) method. Used with permission from [60]. Copyright 2014 by Elsevier. F) 10 x 10 mm^2 CZ grown semi-insulating (top) and 10 x 15 mm^2 EFG grown unintentionally-doped (bottom) single crystal substrate samples processed in this work. (The top sample also has epitaxial layers grown by MOVPE.)

While the potential to produce large (so far up to 4") substrates exists [61], only the EFG method has been used to produce β-Ga_2O_3 for commercial use. These substrates were originally intended for the light emitting diode (LED) market because of their transparency into the UV range, and the primary surface plane is thus $(\bar{2}01)$ because of its superior lattice match to GaN which was intended to be heterogeneously integrated for the LED market. For homoepitaxial growth, $(\bar{2}01)$ is inferior to (010) or (100) because epitaxial growth rates are very slow using metal organic vapor phase epitaxy (MOVPE) or molecular beam epitaxy (MBE) on that plane; therefore, substrates for power semiconductor and RF switching transistor development are often on the (010) or (100) oriented surface. This and the research nature of other growth methods (CZ and FZ) leads

to only small sample sizes being available for investigation into power and RF switch transistors. In our lab, substrates are purchased with sizes of 10 mm x 15 mm with (010) surface or obtained through collaborations with 10 mm x 10 mm (100) surface. With only these small substrate sizes available, the ability to perform well controlled experimentation on various fabrication techniques is limited.

For RF switch and power semiconductor lateral devices such as those described later in Chapter 4, besides a low defect native substrate, it is important to have an insulating substrate that minimizes off-state leakage current, I_{OFF}. For β-Ga_2O_3, Mg [60] or Fe [62] can be added during the melt growth as compensating deep level traps to create semi-insulating substrates for lateral device fabrication. For vertical devices on the other hand, conductive substrates are often needed. In this case, it has been shown that β-Ga_2O_3 substrate doping can be controlled using either Sn [63] or Si [64]. Finally, it should be noted that β-Ga_2O_3 unintentionally doped (UID) substrates have a carrier concentration in the high 10^{16} cm^{-3} [65] related to unintentional Si-doping during the melt growth [43].

Ga_2O_3 Epitaxy

Epitaxial layers of Ga_2O_3 have been grown using a variety of different techniques including MOVPE [66], MBE [47], low pressure chemical vapor deposition (LPCVD) [67], hydride or halide vapor phase epitaxy (HVPE) [26][68], pulsed laser deposition (PLD) [69], atomic layer deposition (ALD) [70],and ultrasonic mist chemical vapor deposition (mist-CVD) [31]. Homoepitaxial layers of β-Ga_2O_3 used in our lab have been grown by MOVPE, MBE, LPCVD, or PLD, so we will focus on maturity, advantages, and disadvantages of these four methods.

MBE is a commonly used, primarily experimental growth technique that has nearly atomistic control of crystalline interfaces. MBE is performed at ultra-high vacuum [71] allowing direct incorporation of constituent atoms to a nearly atomically clean crystal surface through impingement of beams of atoms or molecules [72]. A typical MBE growth chamber is pictured in Figure 15; each constituent atom is maintained in a separate growth effusion cell with flow controlled by a mechanical shutter. MBE is a relatively slow growth method and is thus not easily scaled to production levels. The equipment used also limits both the size of the sample because of beam uniformity and the species available using a particular growth chamber because of cross contamination concerns [72].

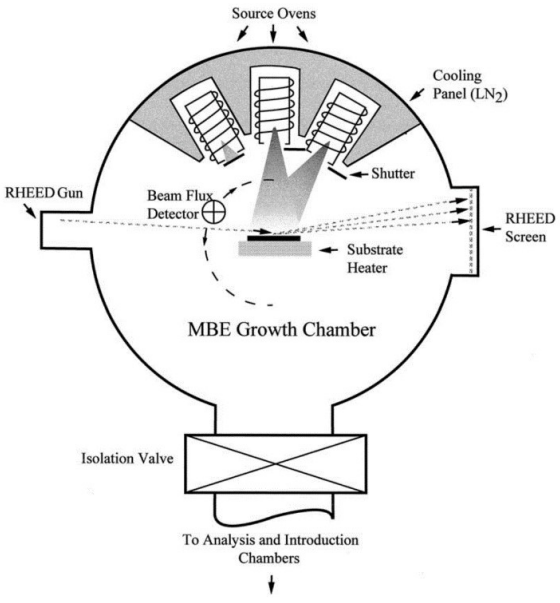


Figure 15 Top view of a simple MBE chamber showing the essential growth sources, shutters, beam flux detector and the reflection high energy electron diffraction (RHEED) system for monitoring structure during growth. Reprinted from [72], with permission from Elsevier.

MBE growth of heteroepitaxial and homoepitaxial β-Ga_2O_3 has been performed to obtain UID and Si- [73], Sn- [47], or Ge-doped [74] n-type layers. The growth conditions are similar for all of these dopant species with doping level controlled by varying the dopant cell temperatures. Substrate temperature is usually maintained from 600-800 ºC with the Ga beam equivalent pressure, usually ~$1.1x10^{-7}$ Torr, optimized for growth rate and crystal quality. High quality n-type films have been grown for device channels with mobility values >100 $cm^2/(V·s)$ using MBE [47]. Highly resistive UID layers grown by MBE have also been used in an implant doping process to obtain device channels [75]. The growth rate using MBE has been shown to vary from ~10 nm/h to 125 nm/h for the (100) and (010) growth planes, respectively [47]. This is the primary reason MBE growth has been largely on the (010) surface. Uniformity of the MBE growth-related to the proximity of the ozone (oxygen) source-across even small sample sizes also needs to be improved.

MOVPE, which is very similar to metal-organic chemical vapor deposition (MOCVD), is a commonly used, potentially commercial scale growth technique that provides very good crystal uniformity while maintaining reasonable growth rates. As such it is the primary production method for GaN and gallium arsenide [71]. MOVPE growth utilizes a chemical reaction at the growth surface and requires only a moderate vacuum compared to MBE. MOVPE layer control is traditionally not as precise as MBE. The MOVPE equipment is considered to be more configurable for increasing wafer size, and since layer growth is controlled by a chemical reaction, species contamination is less likely.

MOVPE has been used to grow hetero- and homoepitaxial layers of n-type (Si or Sn-doped) or UID β-Ga_2O_3 with high quality for device channel layers or diodes [76]. Original growth methods using trimethylgallium (TMGa) as Ga precursor and water (H_2O) as oxygen source [66] have been adapted to a standard process using the reaction of triethylgallium (TEGa) as Ga precursor and molecular oxygen (O_2) as oxygen source [77]. Recent homoepitaxial layers are grown at chamber temperature and pressure of 850 ºC and 5 mbar (3.75 Torr), respectively, and have been doped using tetraethyltin (TeSn) and tetraethylorthosilicate (TeOS) over a wide doping range as measured by secondary ion mass spectroscopy (SIMS) and shown in Figure 16 [76]. The Highest quality films had a growth rate of around 120 nm/h and had only a 20% decrease in growth rate from the (010) to (100) growth plane [76] as opposed to the order of magnitude difference (>90%) for MBE.

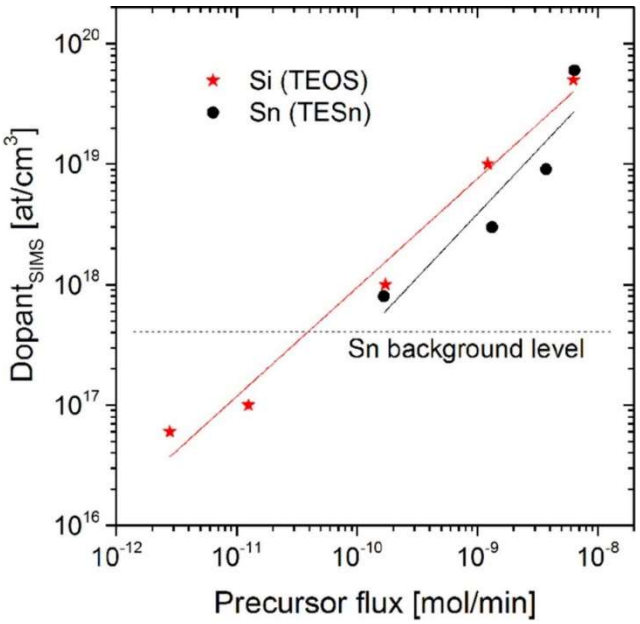


Figure 16 SIMS concentration of Si (red stars) and Sn (black circles) versus TEOS and TESn flux. The solid lines are the linear regression of the experimental data, the dashed one indicates the Sn background level due to memory effect. Reproduced from [76] under the Creative Commons Open Access use policy https://creativecommons.org/licenses/by/3.0/.

LPCVD is very similar to the MOVPE method, however, the reactor pressure is lowered to 0.01 to 1 Torr to decrease any unwanted gas phase reactions. While the use of LPCVD for β-Ga_2O_3 epitaxial growth is limited, a growth temperature range from 780 to 950 C using metallic gallium (Ga) and oxygen (O_2) as precursors has been investigated for homoepitaxy in ref [67]. In this work, the growth was as high as 1.3 μm/h; however, the surface morphology (a reported minimum of ~7 nm root mean square (RMS) roughness [67]) was not as good as MBE (0.7 nm RMS roughness [47]) or MOVPE (0.6 nm RMS roughness [76]) methods . The high growth rate and good layer uniformity is the expected advantage of the LPCVD method, and further investigation is underway. No information on dopant control has been published to date using this method.

PLD uses a high-powered laser to vaporize a material target creating a plasma plume which deposits a film on a temperature controlled substrate usually facing that target. The actual process and parameters used are quite complicated [71], but for understanding β-Ga_2O_3 growth, details of the process are not essential. While we have pursued PLD homoepitaxy in our lab, available publications using this growth method are limited to deposition of polycrystalline β-Ga_2O_3 thin films on sapphire substrates [78], [79]. The crystal grains in these thin films have a $(\bar{2}01)$ orientation, and Si concentration control from 10^{15} to 10^{20} cm^{-3} has been demonstrated by changing the wt. % of Si in the material target used [79]. The relatively low temperature (500 ºC) and reasonable pressure required (1 Pa or 7.5x10-3 Torr) make this technique viable for some in-process film growth methods (e.g. ohmic regrowth) [78].

Doping Ga_2O_3

In the previous two sections, we have detailed the growth of β-Ga_2O_3 using melt growth techniques for substrates and vapor phase techniques for epitaxial channel layers, and we have mentioned that several n-type dopants are available to be incorporated during these growth techniques. We note that ion implantation of silicon donors has also been performed [80], and here we provide some more material background on these dopants.

Group 4 elements, Si^{4+}, Ge^{4+}, and Sn^{4+}, can be substituted for Ga^{3+} atoms in the monoclinic crystal lattice to act as donors in an n-type β-Ga_2O_3 channel layer. No suitable acceptor atoms to create p-type β-Ga_2O_3 have been found to date. Although data is limited on comparison of the different donors in Ga_2O_3, the differences between the

substitution site, atomic radius, and activation energy of the available donors can play a large role in the density of crystal defects. This has implications for device performance related to the mobility and the amount of surface defects for interfaces between β-Ga_2O_3 and the other materials necessary to fabricate a semiconductor device. Since the best donor is far from being determined based on the material system immaturity, we provide a summary here of the studies so far related to the different potential donors to n-type β-Ga_2O_3.

Table 3 Summary of Ga_2O_3 donors with a comparison of lattice match to the substituted gallium atom.

Atom	4-fold Atomic Radius (pm) [64]	6-fold Atomic Radius (pm) [64]	Mismatch $\Delta R/R_{Ga}$ (%)	Activation Energy (meV)
Ga^{3+}	47	62		
Si^{4+}	26*	40	-40	31 [50]
Ge^{4+}	39*	53	-16	17.5 [81]
Sn^{4+}	55	69*	+14	60.0 [82]

*Preferred site for substitution according to [43] based on modeled formation energies. The mismatch is calculated for the preferred site.

Table 3 shows the atomic radius computed for different donors in the monoclinic β-Ga_2O_3 crystal lattice. Here, we can see that Sn and Ge are likely to cause a smaller disturbance in the crystal lattice. Ge and Si are more likely to substitute at the tetrahedral Ga site and Sn at the octahedral site, and it is unclear in doping experiments so far if any of the donors can substitute at both sites. Additionally, in [43] fluorine and chlorine are mentioned as potential n-type donors, which can affect device fabrication because both materials are typically used in dry etch processes. The activation energies listed in Table

3 are preliminary values obtained from a single or a few fabricated devices; however, the results indicate that donors can contribute electrons at room temperature. These activation energies often assume a large percentage of compensating acceptors in the charge neutrality equations (up to 61% in the case of Ge [81]) which according to [83] can cause reduced mobility compared to the intrinsic limits of gallium oxide based only on ionized impurity and phonon scattering. Further investigation is underway to analyze the best dopants as will be discussed later.

Materials Comparison

We conclude the materials section by comparing the β-Ga_2O_3 material properties discussed above with some other wide bandgap semiconductors of interest as shown in Table 4. All values used for β-Ga_2O_3 are described above with the exception of the relative static dielectric constant of ~10.2 [52], [84], and the critical field strength of 8 MV/cm which is empirically estimated from the bandgap as in ref [4], calculated in ref [16] from empirical equations, and shown in Figure 2. The material parameters of the other semiconductors are taken from the referenced source, and the figures of merit are calculated from those parameters as described in Chapter 1. It should be noted that there are some deviations in the literature for many of the material parameters; however, this does not affect the values enough to drastically skew the comparison between the various materials. It is obvious from Table 4 that, with the exception of thermal conductivity, β-Ga_2O_3 has advantages or at least similar properties to other competing technologies for wide bandgap devices, and unlike diamond or GaN, β-Ga_2O_3 has a simple melt grown native substrate. In the next chapter, we will investigate devices used to exploit these

material advantages using β-Ga_2O_3 and compare that with some of the device technologies available using other wide bandgap materials. This will provide further insight into achieving the material potential for each of the material systems in Table 4

Table 4 A summary of material parameters and figures of merit for various wide-bandgap semiconductors. Figures of merit are normalized to Silicon. All materials are n-type with the exception of diamond which has only demonstrated p-type devices.

	Si [85]	**GaAs** [85]	**GaN** [85]	**4H-SiC** [85]	**Diamond** [86]	**β-Ga_2O_3**
Bandgap, E_g (eV at 300K)	1.12	1.43	3.4	3.2	5.5	4.8
Relative dielectric constant, ε_r	11.9	13.0	9.5	10.0	5.5	10.2
Saturated drift velocity, v_{sat} (x10^7 cm/s)	1.0	1.0	2.5	2.0	1.1 [87]	1.1-2.0
Critical field, E_c, (MV/cm)	0.25	0.3	3.0	3.0-4.0	> 4.0	8.0 (est)
Thermal conductivity, λ, (W/m·K at 300K)	150	50	130	300-400	2090	10-27
Bulk mobility, μ (cm^2/V·s est. at 300 K)	1350	8500	1000	950	2000 [87]	150-300
Baliga's DC figure of merit, BFOM ($\mu\varepsilon E_c^3$)	1	12	1022	1022-2422	2804	3120-6242
Baliga's high frequency figure of merit, BHFFOM (μE_C^2)	1	9	107	101-180	379	114-228
Johnson's figure of merit, JFOM ($v_{sat}E_c$)	1	1.2	30	24-32	17.6	35-64

3. GALLIUM OXIDE DEVICES

In this chapter, we describe the development of gallium oxide electron devices including transistors and diodes. We focus on β-Ga_2O_3 transistors and their development toward high-voltage switching and high power RF switching applications. We also present some information on competing device technologies and associated advantages and disadvantages in using different material technologies. We conclude with a summary of state of the art results for β-Ga_2O_3 MOSFETs from the literature.

Early Development

As previously noted, only recently has β-Ga_2O_3 been mentioned for wide bandgap semiconductor electronic devices, and even as these applications begin to be developed, the material momentum is often fueled by other potential applications. As an extremely wide bandgap TCO, single crystal β-Ga_2O_3 substrates were first developed for potential optoelectronic applications that exploited the deep-UV transparency resulting from the materials ultra-wide bandgap [53], [69]. Substrate development continues to be fueled by the potential to grow GaN-based semiconductor blue light emitting diodes (LEDs) to realize a solid white light source, UV LEDs, and potentially laser diodes on the β-Ga_2O_3 substrates [59].

Other than some fringe research in nanowire devices [88], researchers from the Tokyo Institute of Technology developed the first Ga_2O_3 FET in 2006 from PLD

deposited heteroepitaxial Ga_2O_3 of unknown polycrystalline structure [89]. The 50-μm gate length, top down metal insulator semiconductor FET (MISFET) was primarily used to demonstrate control of the conductivity of Ga_2O_3 under an external electric field, but the results, presented in Figure 17, would kick off further exploration into the technologies considered herein.

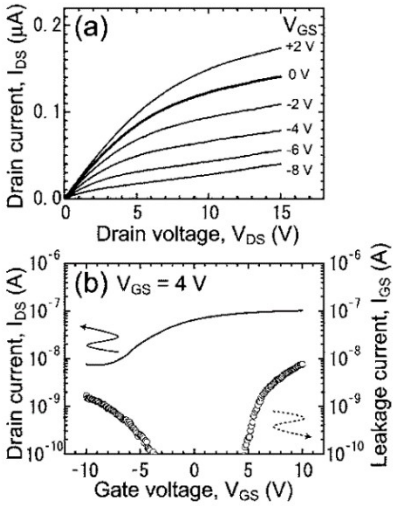


Figure 17 (a) Output and (b) transfer characteristics of FET using epitaxial tin-doped Ga_2O_3 film as a channel layer measured at room temperature. Reprinted from [89]**, with the permission of AIP Publishing. The device is the first ever Ga_2O_3 transistor.**

Other than a photodiode intended for solar-blind photodetector [18], Schottky barrier diodes (SBD) were first reported as characterization devices for CZ grown UID substrates in 2011 [52]. A calculated Schottky barrier height of ~1.1 V was obtained for a nickel contact on the (100) β-Ga_2O_3 surface. The authors noted the surprisingly good behavior of the un-optimized SBDs shown in Figure 18 and the resulting potential of β-Ga_2O_3 for other power semiconductor devices [52].

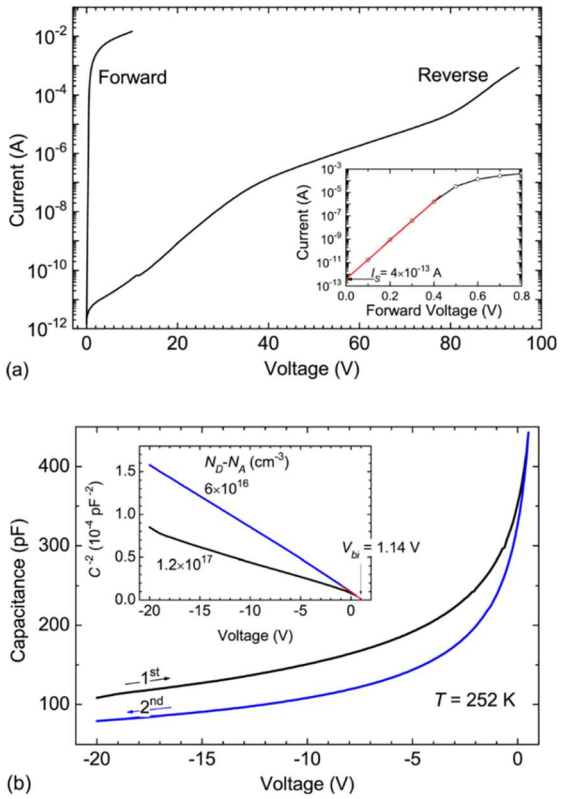


Figure 18 (Color online) I-V (a) and C-V (b) characteristics of a Ni Schottky contact (0.8mm diameter) of UID sample grown by the CZ method. Inset of (a): The extrapolated I-V curve in the low forward voltage range results in a saturation current I_S=4x10^{-13} A. Inset of (b): Extrapolation of the plot C^{-2} vs reverse voltage yields the built-in voltage V_{bi}=1.14 V. In (b) the black curve (1st) and the blue one (2nd) belong to the following experimental conditions: Sample cooled down from room temperature to about 250K with the reverse voltage (-20 V) on, then, the first C-V measurement was started with decreasing reverse voltage up to a forward voltage of 0.5V and finally, the second C-V measurement was done with increasing reverse voltage. Reprinted from [52], with the permission of AIP Publishing.

The current surge in research in β-Ga_2O_3 electronic devices followed the groundbreaking metal semiconductor FET (MESFET) results of the Japanese researchers Higashiwaki, Sasaki, Kuramata, Masui, and Yamakoshi in 2012 [4]. The device, fabricated on Sn-doped MBE homoepitaxy on (010) Fe-doped, FZ grown semi-insulating substrates and shown in Figure 19, achieved a current of 15 mA (~25 mA/mm) at gate

voltage, V_G = +2 V and perhaps more notably, a three terminal breakdown voltage, V_{BK} = 257 V, for a 20 µm source-drain (S-D) spacing [4]. Although, the device had a marginal on-off current ratio, I_{ON}/I_{OFF}~10^4, from gate leakage through the Schottky barrier at the gate and the actual breakdown field strength (~0.2 MV/cm) did not come near surpassing GaN or SiC, the early device result and the language of the authors had set the stage for investigation of β-Ga_2O_3 for the development of high voltage, high power electronic devices.

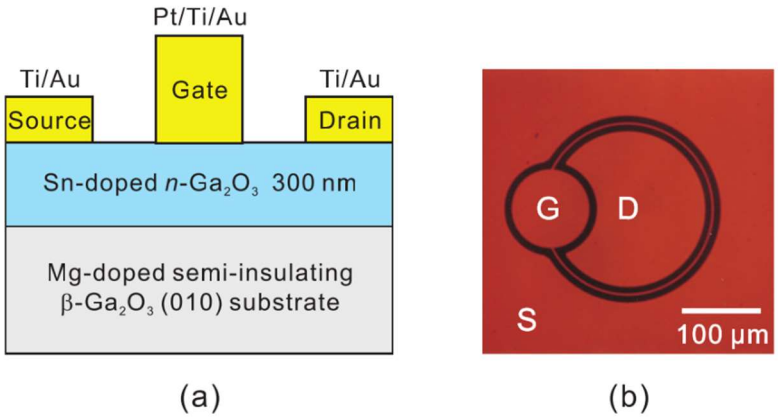


Figure 19 (a) Cross-sectional schematic illustration and (b) optical microscope micrograph of Ga_2O_3 MESFET. Reprinted from [4], with permission from AIP Publishing.

β-Ga_2O_3 MOSFETs

To improve the original MESFETs performance, the same group introduced the β-Ga_2O_3 depletion-mode MOSFET in 2013 using similar material [82]. The addition of a thin layer of aluminum oxide, Al_2O_3, as both a passivation layer and gate oxide significantly reduced gate leakage and improved the on-off current ratio by 6 orders of

magnitude to $I_{ON}/I_{OFF} \sim 10^{10}$ [82]. The device also had a reduced gate length, 2 μm, and improved ohmic contact linearity enabled by an Si-ion-implanted contact region, a 13 nm-deep reactive ion etch (RIE) of the surface, and a 470 ºC ohmic anneal [82]. The MOSFET has subsequently become the standard transistor fabricated using β-Ga_2O_3 substrates and n-type channel layers.

Although only a few β-Ga_2O_3 transistor results have been published, milestones for the technology have been rapidly achieved. Field-plate technology was implemented to achieve $V_{BK} > 750$ V on a lateral device which also utilized a previously developed Si-implant process [80] on highly resistive UID epitaxial layers grown by MBE [75]. The SiO_2 layer beneath the field plate in this device was also used to passivate the surface traps leading to reduced dispersion in the I-V characteristics of the device as shown in Figure 20, presenting an early potential mitigation to an issue that is still being investigated for GaN technologies. The original MOSFET was also used to demonstrate thermal stability by maintaining $I_{ON}/I_{OFF} > 10^4$ for an ambient temperature of 250 ºC as shown in Figure 21 [82].

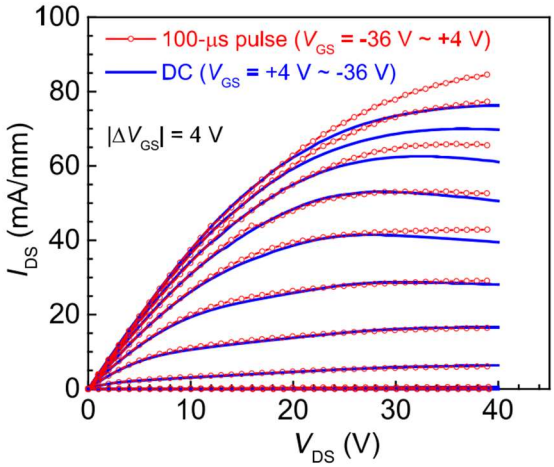


Figure 20 DC and pulsed I_{DS}-V_{DS} characteristics of the Ga_2O_3 FP-MOSFET showing non-dispersive behavior. The pulsed measurements were performed at an off-state quiescent bias condition of (V_{DQ}, V_{GQ}) = (40 V, −36 V) with a pulse width and period of 100 µs and 100 ms, respectively. Reprinted, with permission, from [75]. Copyright © 2016.

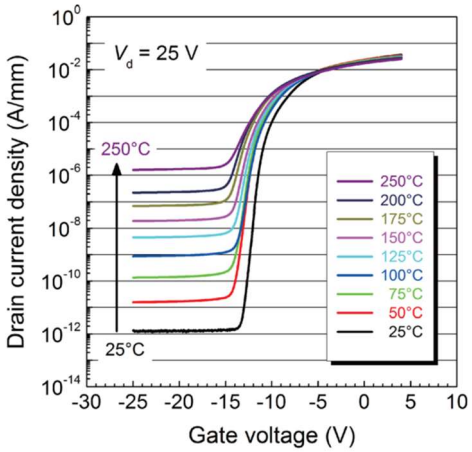


Figure 21 Transfer characteristics at V_d = 25 V of Ga_2O_3 MOSFET (L_g = 2 µm) as a function of operating temperature. Reprinted from [82], with the permission of AIP Publishing.

Other research groups have taken advantage of the strong (100) cleavage plane, to exfoliate nanomembrane devices for additional research [90], [91]. While these devices

have limited value for commercialization [90], they have been used to demonstrate high current density with maximum current values, I_{DMAX}, greater than 600 mA/mm using a 0.85 µm gate length self-aligned source and drain device [91].

In our group, a critical field strength E_C > 3.8 MV/cm was demonstrated on a β-Ga_2O_3 MOSFET with an MOVPE grown Sn-doped homoepitaxial channel [92]. The device shown in Figure 22 had a V_{BK} = 200 V on a much smaller gate-drain (G-D) spacing, 0.6 µm, than previously reported devices with similar or larger V_{BK} values. As shown in Table 4 this value exceeds the critical field strength of GaN and SiC and nearly exceeds that of diamond.

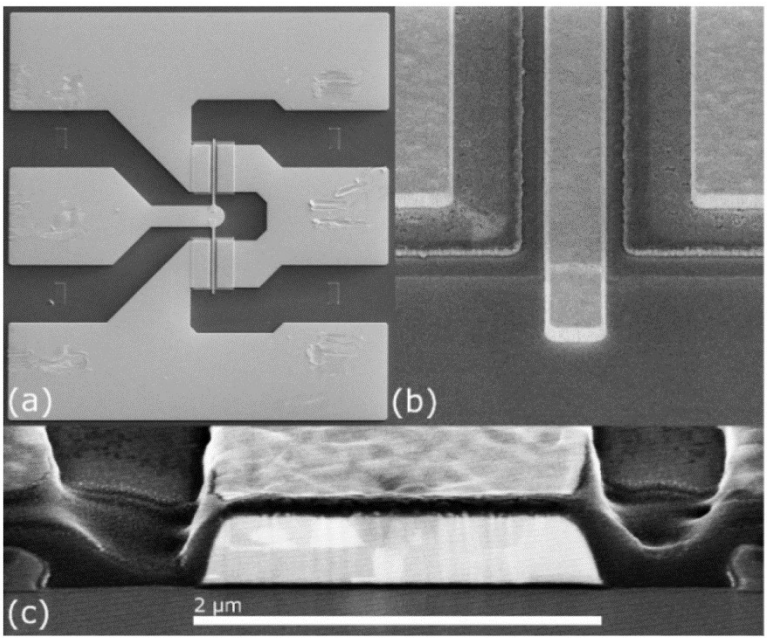


Figure 22 (a) Top-down SEM image of a high critical field lateral β-Ga_2O_3 MOSFET with L_G = 2 µm, L_{GS} = 0.8 µm, and L_{GD} = 0.6 µm. (b) Angled view SEM image of the gate finger. (c) Cross-sectional SEM view of the source drain space and gate finger. Reprinted, with permission, from [92]**. Copyright © 2016.**

Occurring over only a 4 year span the early and limited MOSFET results are impressive and have prompted a surge in β-Ga_2O_3 MOSFET research. As a result, research groups have also focused heavily on improved homoepitaxial material and improved metal-semiconductor and metal-oxide semiconductor interfaces. This research will be discussed next.

β-Ga_2O_3 Material Interfaces (MOSCAPs and SBDs)

Interfaces in the β-Ga_2O_3 material system including metal-semiconductor ohmic and Schottky contacts and metal-oxide-semiconductor capacitors (MOSCAP) must be characterized to provide physical understanding of proposed electronic devices. Like transistors, research into MOSCAP structures, ohmic contacts, and Schottky barrier diodes (SBD) has increased rapidly. Here we present some of the recent results.

Nickel (Ni), gold (Au), and platinum (Pt) SBDs have been produced on β-Ga_2O_3 material with several different crystal orientations and doping concentrations to study the Schottky barrier produced by placing the metal and semiconductor in direct contact. SBDs are important electronic devices themselves and also provide insight into the band structure of the metal-semiconductor contact created. Ni SBDs on a $(\bar{2}01)$ β-Ga_2O_3 UID (N_d = 1.2x10^{17} cm^{-3}) EFG grown substrate had a Schottky barrier height of 1.25 eV and an ideality factor of 1.01 [50]. Pt SBDs on a (010) β-Ga_2O_3 UID (N_d = 5x10^{16} cm^{-3}) FZ grown substrate had a Schottky barrier height of 1.3-1.5 eV and an ideality factor of 1.04-1.06 [93]. Finally, Au SBDs on a (100) cleaved β-Ga_2O_3 sample from a UID (N_d = 6x10^{16} cm^{-3}) CZ grown substrate had a Schottky barrier height of ~1.04 eV and an ideality factor of 1.02 [94]. Because of the unipolar nature of β-Ga_2O_3, SBDs are one of the primary

potential uses for power electronic devices, as such, many other materials have been evaluated for SBDs [95]. A review of all of these, however, is beyond the scope of this work.

Ohmic contact formation on β-Ga_2O_3 devices has primarily been focused on metal stacks with titanium metal (Ti) at the semiconductor surface [4], [80], [82]. Often researchers have employed an ohmic anneal (typically ~500 ºC) to obtain reasonable ohmic contacts [82]. Additionally, ion-implantation into the ohmic contact regions [80] and reactive ion etching has been performed to expose the degenerately doped implant to form a good ohmic contact [82]. Still, linearity of contacts can be difficult to obtain especially for lightly doped and UID material, and even when contacts have linear current-voltage (I-V) relationships, contact resistances can be large. This has led to investigation of alternative ohmic contacts such as indium tin oxide (ITO) which produced a reasonable ohmic contact resistance of ~20 Ω-mm even for a lightly doped (N_d = 2x10^{17} cm^{-3}) β-Ga_2O_3 substrate [96]. The linearity of the ITO ohmic contacts at different annealing temperatures is shown in Figure 23. Formation of good ohmic contacts is an ongoing research area, and it will be discussed for our devices in Chapter 6.

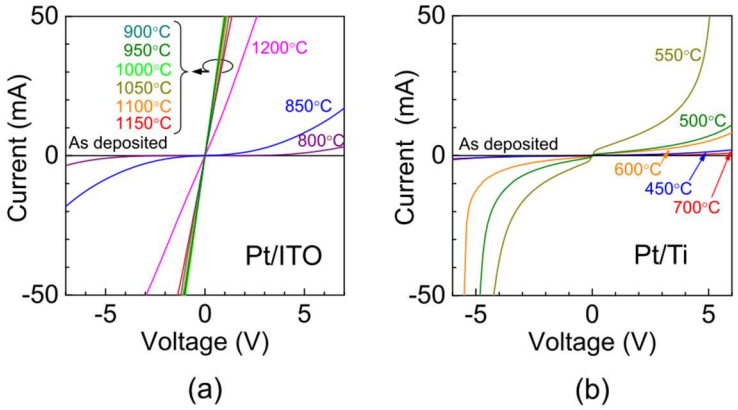
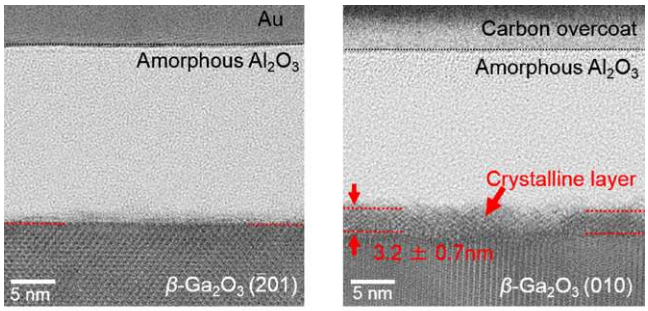


Figure 23 Typical I V characteristics of (a) Pt=ITO and (b) Pt=Ti electrodes annealed at various temperatures. Reprinted from [96]**, under the Creative Commons open access policy https://creativecommons.org/licenses/by/3.0/. Available online at http://iopscience.iop.org/article/10.7567//JJAP.55.1202B7.**

In addition to simple process control capacitance-voltage (C-V) structures on MOSFET samples which will be discussed extensively later, MOSCAP and MOS diode structures have been fabricated using silicon dioxide (SiO_2) and aluminum oxide (Al_2O_3) as oxide layer to characterize the important properties of the metal-oxide-semiconductor interface in β-Ga_2O_3 devices. For power MOSFET devices, the conduction band offset of these oxide layers compared to β-Ga_2O_3 is of primary importance to allow maximum forward bias without excessive gate leakage. For Al_2O_3, a conduction band offset of ~1.5 eV was measured on $(\bar{2}01)$ β-Ga_2O_3 using X-ray photoelectron spectroscopy (XPS) and MOS diode forward bias Fowler-Nordheim (F-N) tunneling currents [97]. For SiO_2, a much higher conduction band offset of ~3.63 eV was measured on $(\bar{2}01)$ β-Ga_2O_3 (N_d = $9.7x10^{18}$ cm^{-3}) using XPS and MOSCAP forward bias F-N tunneling currents [98]. These are the primary gate oxides investigated in β-Ga_2O_3 MOS devices although hafnium oxide (HfO_2) has been investigated in our group, as seen later. The $(\bar{2}01)$ plane;

however, is not the common plane for device homoepitaxial channel layer growth, and the gate oxide interface with the (100) or (010) planes which are more common may not follow the $(\bar{2}01)$ reported results. As an example, another important feature of the Al_2O_3-β-Ga_2O_3 interface, namely the interface trap density (D_{it}), was found to be significantly different between $(\bar{2}01)$ and (010) when extracted from C-V measurements on MOSCAP structures [99]. The authors found that a good lattice match of oxygen atoms between γ-Al_2O_3 and the (010) face of β-Ga_2O_3 caused the formation of a thin crystalline layer of γ-Al_2O_3 during the ALD deposition as shown in Figure 24. In our lab, we have observed apparent crystalline hafnium oxide at its interface with a (100) β-Ga_2O_3 surface through transmission electron microscopy (TEM) images (Figure 25), although, this effect requires more extensive study. The MOS structure is very important to the modeling of β-Ga_2O_3 devices and further characterization of this interface will be discussed throughout this work. Because of its importance, numerous investigations including some into more exotic ternary oxides, non-oxide insulators, and bilayer oxides have recently begun to emerge [100], [101], and important results are summarized for all potential gae insulators in Table 5. In our case, we have investigated only the oxides listed above (SiO_2, HfO_2, and Al_2O_3) which are those that have been successfully used to create MOSFETs so further discussion into the broad array of insulators and interface properties with β-Ga_2O_3 is beyond the scope of this work.



(a) (b)

Figure 24 Cross-sectional TEM micrographs of (a) Al_2O_3/β-Ga_2O_3 ($\bar{2}01$) and (b) Al_2O_3/β-Ga_2O_3(010) interfaces with Al_2O_3 films deposited at 250 °C. Reprinted from [99]**, under the Creative Commons open access policy https://creativecommons.org/licenses/by/3.0/. Available online at http://iopscience.iop.org/article/10.7567/JJAP.55.1202B5.**

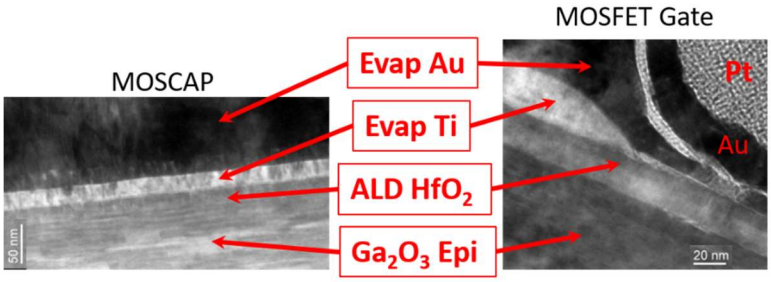


Figure 25 Preliminary results of transmission electron microscopy (TEM) at the ALD HfO_2-Epitaxial Ga_2O_3 interface for a MOSCAP (left) and a MOSFET gate stack (right). The interface appears to show some order in the HfO_2 layer. Further research is underway to characterize this structure.

Table 5 Summary of insulators used for the gate insulator in β-Ga_2O_3 capacitors or transistors. The band offsets are in reference to the conduction band and valence band of β-Ga_2O_3.

Insulator	Bandgap* (eV)	Relative Permittivity, ε_r or κ	Conduction Band Offset, ΔE_C (eV)	Valence Band Offset, ΔE_V (eV)
SiO_2 (ALD)	8.6 [98]	3.9 [102]	3.63 [98]	0.43 [98]
Al_2O_3 (ALD)	6.8 [97]	9-11 [102]	1.5 [97]	0.70 [97]
HfO_2 (ALD)	6.0 [103]	15-26 [102]	>1 [104]	-0.5 [104]
$HfSiO_4$ (ALD)	7.0 [101]	3.9-26 [102]	2.38 [101]	0.02 [101]

HBN	5.97 [105]	3-4 [105]		
$LaAl_2O_3$ (sputtered)	6.4 [106]	9-30 [102]	2.01 [106]	-0.21 [106]
ZrO_2	5.9 [107]	14-25 [102]	>1 [104]	-0.3 [104]

β-Ga_2O_3 Material Improvements

The maturation of devices also prompts improvements in the epitaxial channel materials used to create the devices described in the previous chapter. Material improvements usually focus on obtaining accurate thickness of homoepitaxial layers (even down to very thin layers), accurate prediction of chemical concentration and active carrier concentration from dopant species introduced during growth, and improvement in the mobility through reduction of crystal defects. Thickness and doping studies, often unpublished, are usually conducted by using secondary ion mass spectroscopy (SIMS) (which provides the chemical concentration) on samples grown with several different doped layers to verify thickness and doping parameters [73], [74]. Additionally, once reasonable confidence is obtained in growth parameters, SIMS, C-V measurements (which provide active carrier profiles), and Hall Effect measurements on finished homoepitaxial samples (or sister growth samples) are used to confirm thickness, doping, and actual active carrier concentrations for future material growth [47], [77]. In the discussions that follow, we generally assume that the thickness provided from the grower is accurate because of the familiarity of material growers in determining thickness and the invasiveness in verifying it. We verify carrier concentration levels via the Hall Effect,

C-V measurements, or both because the value before and after fabrication and the methods used to measure each often have significant variations.

Mobility improvements on the other hand can only be attempted one growth run at a time and require adaptations to the growth direction or conditions in that growth to be studied. The results are verified by Hall Effect measurements of the mobility (the doping concentration should also be known) or by field effect mobility on fabricated devices. Analysis of the results is often even more difficult requiring methods like TEM to analyze the level and type of defects in the crystal. As an example in ref [77], the authors used TEM images shown in Figure 26 to determine that planar defects in MOVPE grown β-Ga_2O_3 homoepitaxial layers were causing a reduction in mobility and doping efficiency that could be corrected by an optimum off-angle cut along the (100) plane [77]. The same effect was not seen in growth on the (010) plane using TEM [76]. Similar studies, though, are often not published, with only the high mobility values, often automatically attributed to high quality crystal growth, being reported. In this work, we measure mobility values via the Hall Effect, on devices at low field (although this method is less desirable because of the requirement for accurate C-V measurement), or both. We do not analyze the root causes of low or high mobility, and instead focus on the device performance given the mobility value.

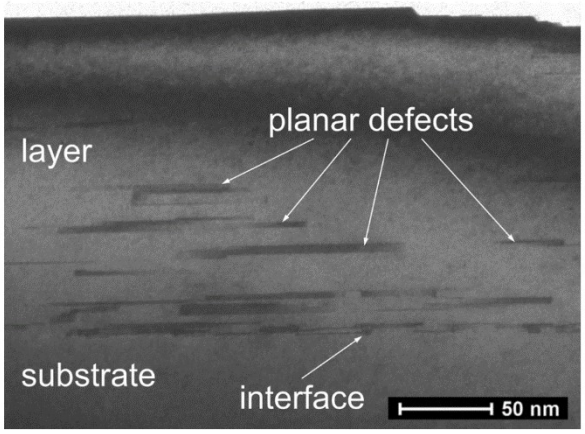


Figure 26 Bright field TEM image showing the presence of planar defects in the MOVPE grown β-Ga_2O_3 (100) layers. Reproduced from [77]. © Springer Science+Business Media New York 2015. With permission of Springer.

Similar Devices

As mentioned in Chapter 2, β-Ga_2O_3 has material advantages over several competitors in the field of power and RF switching electronic devices. Since realization of those material advantages requires fabrication in actual devices, it is beneficial to understand the advantages and limitations of β-Ga_2O_3 devices compared to devices in the GaN, GaAs, SiC, and Si material systems. This section will focus on the primary high voltage, high power device technologies for each of these material systems. In the last section, we will provide a summary of the state of the art results for β-Ga_2O_3 MOSFETs which will be the electronic device investigated in the rest of this work.

We start the comparison by returning to Baliga's figure of merit introduced in Chapter 1. Benchmarking for conduction loss is often presented as shown in Figure 27 where lower $R_{ON,sp}$ equates to lower conduction power loss at a given V_{BK} (movement to the lower right corner is desired). Devices are compared to the unipolar limit which is determined by Baliga's figure of merit and shown by the solid lines in Figure 27. Devices

that exceed the theoretical line are bipolar devices that cause Baliga's assumption of a junction field effect transistor (JFET) which is a simple unipolar device described in Chapter 1 to break down. Although, this is possible with bipolar devices, the unipolar line is still reasonably close to the material's theoretical limit and is thus used for materials comparison and device benchmarking.

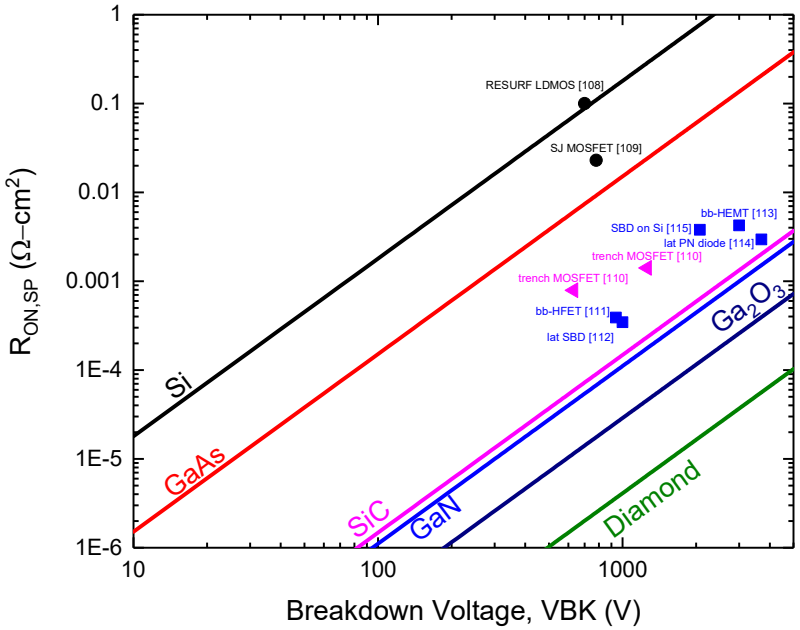


Figure 27 Benchmarking plot showing the specific on resistance, $R_{ON,sp}$, versus breakdown voltage, V_{BK}. The unipolar limit for each material is shown by the solid line, and several high performing devices for Si (black circles), SiC (magenta triangles), and GaN (blue squares) are shown by the symbols. Device data was taken from [108], [109], [110], [111], [112], [113], [114], and [115].

Silicon is still a dominant technology in high power, high voltage devices because of its maturity and excellent bipolar material properties. As mentioned previously, however, Si devices are fundamentally limited by the narrow bandgap of Si, and high

voltage, high power Si devices have matured nearly to the physical limits of the material. Still, both lateral and vertical Si devices play a prominent role in the power semiconductor market, and only the need for smaller more efficient devices has allowed for a greater role of other power semiconductors. Three levels of Si devices, the power MOSFET, the insulated gate bipolar transistor (IGBT), and the thyristor or gated thyristor, are used for power semiconductor applications (Figure 4) with each having an increased level of voltage or power handling [116]. IGBT devices and thyristors are primarily used for high voltage applications and have higher power losses not considered to be competitive with intended applications for β-Ga_2O_3 so these will not be further discussed. Power MOSFETs on the other hand operate at moderate voltages and have very good power loss characteristics. Lateral power MOSFETs are used for high frequency applications and applications requiring integration with other, typically logic or analog, Si devices, and vertical power MOSFETs are used for higher voltage and higher power applications which often do not require on chip integration.

The lowest conduction loss for Si vertical devices has been achieved using the super junction MOSFET (SJ-MOSFET). A very low loss SJ-MOSFET was presented in [109] and is plotted in Figure 27. The SJ-MOSFET achieves high breakdown voltages by leveling the electric field in the drift region using a p-n junction that partially depletes the surface of the drift layer as shown in Figure 28. This method is similar to the reduced surface field (RESURF) method that is used for lateral diffused MOS (LDMOS) devices to reduce the electric field at the surface of the drift region and increase the breakdown voltage of those devices [117][108]. The SJ-MOSFET and RESURF LDMOS represent

the state of the art for Si power MOSFETs as shown in Figure 27, while many variations exist in fabrication techniques of these devices they will not be discussed further here. The bipolar nature of these devices allows them to exceed the unipolar limit presented by Baliga; however, the devices cannot operate much beyond the unipolar limit making the limit still valid for comparing materials.

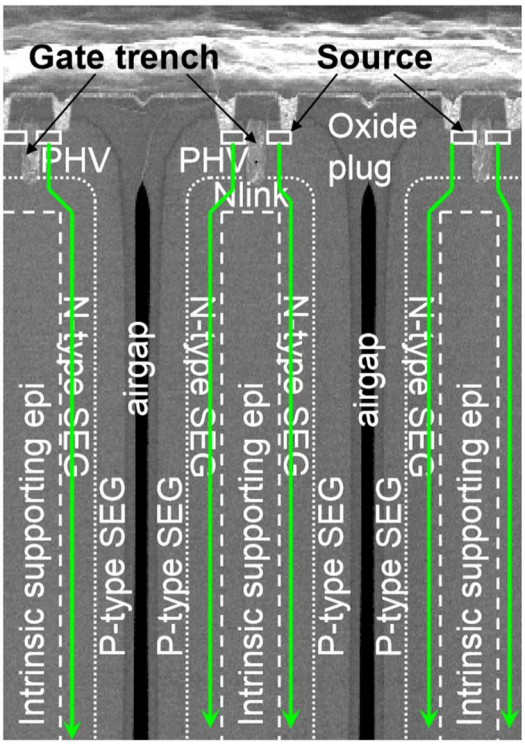


Figure 28 Detail of the SJ-MOSFET structure. The n-and p-type epi layers (selectively grown, SEG), are indicated. Nlink is the connection implant to connect the MOS channel to the n-type SEG layer. The current flow in on-state is shown by green lines and arrows. The I1 layer (separating N-and P-type SEG), is not shown for clarity of the figure). Reproduced from [109] **with permission. © 2011 IEEE.**

SiC high voltage, high power devices are also widely used in the power semiconductor market. The use of SiC is mainly limited by the material cost compared to

Si which can be traced back to the vapor transport method of bulk material growth compared to inexpensive Si melt growth techniques [118]. In certain applications, however, SiC is used because the overall system cost can overcome the cost of SiC because of the advantages of the material over Si.

Many different SiC devices have been attempted for power semiconductor applications including SBDs, Junction field effect transistors (JFETs), Bipolar junction transistors (BJTs), and MOSFETs [118]. The development of these devices has followed a similar path as Si devices incorporating techniques like RESURF and using SBDs and IGBTs for very high voltage operation and MOSFETs as the preferred devices for lower voltage, lower loss applications. In Figure 27, two of the lowest loss devices reported in the voltage range of interest are shown. These devices use a gate and source trench as shown in Figure 29 which reduces the electric field at the drain edge of the gate (bottom corner) by creating a source connected field plate using a slightly deeper source trench [110].

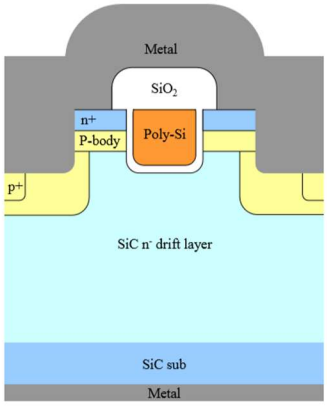


Figure 29 Schematic cross section of a 4H-SiC trench MOSFET with source trench and gate trench. The source trench and gate trench are fabricated simultaneously. Reprinted with permission from [110]**. © 2011 IEEE.**

Other than for optical devices, GaN devices have been typically targeted for high power RF applications, and have only been recently realized for non-RF power semiconductor applications. The market share of GaN in this area is limited by the high cost of producing defect free native GaN substrates, and the similar performance of less expensive SiC devices. Still, GaN SBDs, two dimensional electron gas (2DEG) diodes, and high electron mobility transistors (HEMTs) have been evaluated for conduction losses for switch operation [118]. Additionally, the cost of these devices has been addressed by attempting GaN on Si devices that take advantage of Si as a low cost substrate [115]. The best performers of these devices as shown in Figure 27 have been lateral SBDs that utilize trench technology with field plates to reduce the peak electric field [115], [112] and heterojunction field effect transistors (HFETs) that use a back barrier to reduce the potential for substrate leakage breakdown to occur as shown in Figure 30 [111], [113]. Additionally, in Figure 27 initial bipolar GaN results are shown by a vertical p-n diode that operates very close to the theoretical unipolar curve at higher

breakdown voltage [114]. Further investigation of vertical GaN devices and bipolar devices for low conduction loss is underway by several groups [119]–[121], however, these are limited by several factors including the expense of native GaN substrates and difficulty in establishing a piezoelectric two dimensional electron gas (2DEG) that takes advantage of extremely high mobility using an AlGaN/GaN barrier in a vertical device.

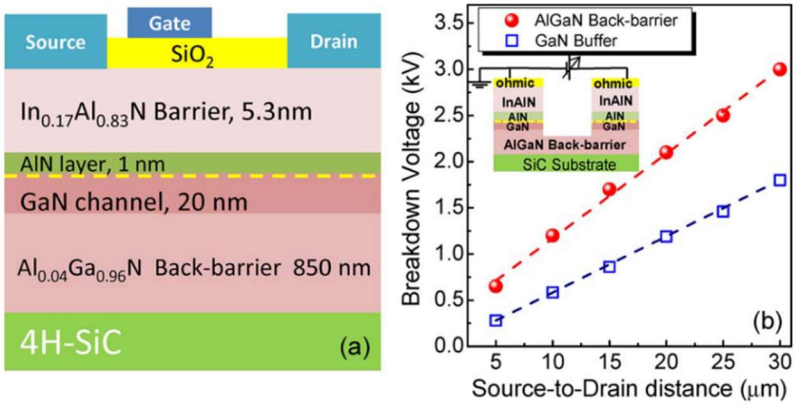
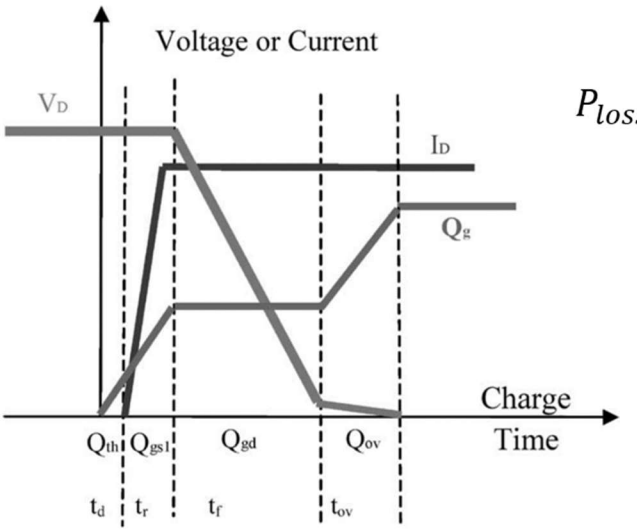


Figure 30 (a) Schematic cross section of a fabricated InAlN/GaN HEMT with an AlGaN back barrier. (b) Two-terminal lateral buffer V_{BK} as a function of source-to-drain distance in transistors with and without an AlGaN back barrier. The inset shows the measurement setup of the InAlN/GaN HEMT with an AlGaN back barrier. Reprinted with permission from [113]**. © 2012 IEEE.**

So far in this section, we have focused on devices with low conduction loss. Benchmarking dynamic losses is, however, more complex. As seen in Chapter 1 Baliga's figure of merit for high frequency includes a term for the gate voltage. Additionally, Baliga's figure of merit assumes that the switch operates at the breakdown voltage, associating this to the charge needed to be moved to turn the gate on or off; however, in true switch applications a separate supply voltage is turned on or off by the gate charge movement as shown in Figure 31. A slight adaptation of Baliga's figure of merit was

made by Huang in [122]. Huang's figure of merit uses $R_{ON,sp}$ and the specific gate-drain charge, $Q_{GD,\,sp}$, to determine the minimum power loss of a switch in a given material system. Two methods are often used for benchmarking high frequency switching devices based on Huang and Baligas' figures of merit. The first shown in Figure 32 compares $R_{ON,sp}$ and $Q_{GD,sp}$ to highlight the relationship between the dynamic and conduction losses in a given device (moving to the lower left is desired) with a target operating voltage. The second shown in Figure 33 compares the $R_{ON,sp}$*$Q_{GD,sp}$ product with the breakdown voltage to show the total switch loss at a given breakdown voltage in a material system (moving to the lower right is desired). Neither of these benchmarking methods is ideal for assessing materials because both require an operating voltage, V_D, to be assumed; however, for the second method, we can assume the operating voltage, V_D, is equal to the breakdown voltage, V_{BK}, as was done by Baliga. It is clear from Figure 32 and Figure 33 that the advantage of β-Ga_2O_3 for conduction loss carries over to provide an advantage for low total power loss. Some of the best GaN and Si performers for total switching losses are included in Figure 33 and good comparisons can be found in Ref. [123] and Ref. [124].



$$P_{loss} = I_{rms}^2 R_{ON} + V_D I_D (t_r + t_f) f$$
$$\approx I_{rms}^2 R_{ON} + V_D I_D t_f f$$
$$= \frac{I_{rms}^2 R_{ON,sp}}{A} + \frac{V_D I_D Q_{GD,sp} A f}{(i_{g,av})}$$

$$R_{ON,sp} Q_{GD,sp} = \frac{4kV_B\sqrt{V_B V_D}}{\mu E_C^2}$$

Figure 31 Switching waveforms of a generic unipolar power device and the calculations of Huang's figure of merit. *k* is an empirical parameter between 0 and 1. Other variables are explained previously. Reprinted with permission from [122]**. © 2004 IEEE.**

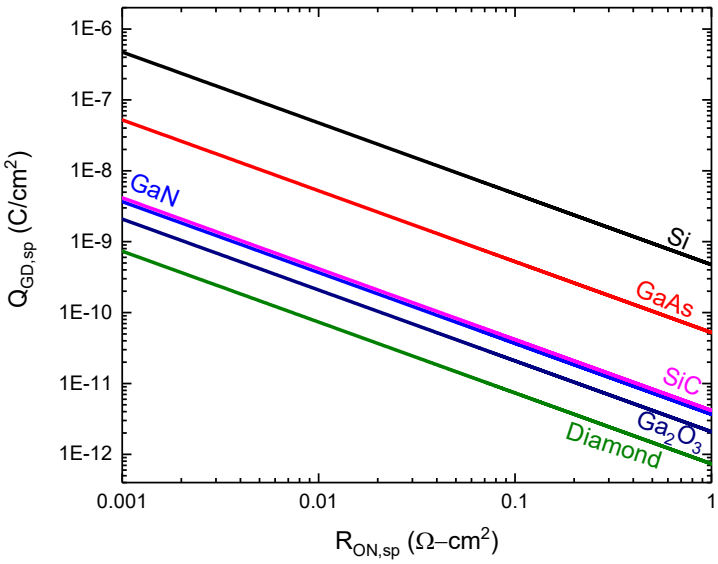


Figure 32 Benchmarking plot of dynamic loss at a given conduction loss showing the unipolar limit for various materials at a supply voltage of 100 V. A material with a theoretical line toward the lower left means that the material has a lower dynamic loss for a given conduction loss than a material with a theoretical line in the upper right.

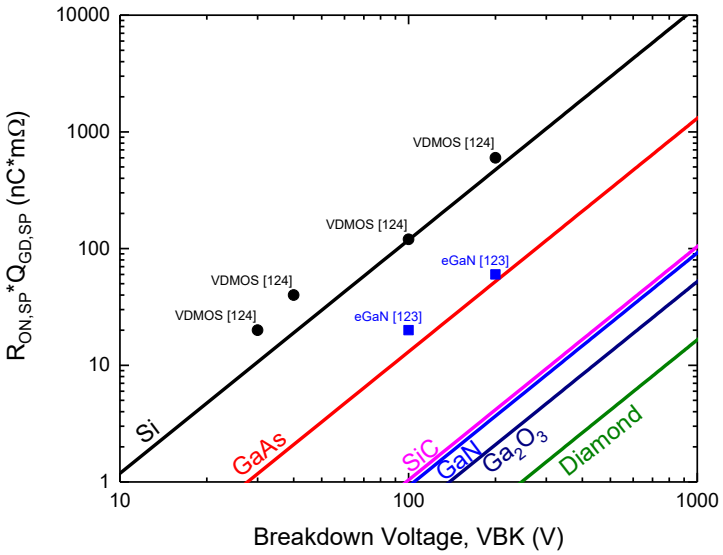


Figure 33 Benchmarking plot of total switch power loss at a given breakdown voltage showing the unipolar limit of several material systems at a supply voltage equal to the breakdown voltage. Moving to the lower right is desirable. Some state of the art results from Si (black circles) and GaN (blue squares) are shown by the symbols. Device data is taken from [124] **and** [123]**.**

Perhaps even more difficult to benchmark is the power-frequency capability of a given material system. Johnson's figure of merit provided in Chapter 1 is a first attempt at this type of benchmarking with results for the same materials in Figure 34. Johnson's figure of merit presents a very simplified picture of power-frequency performance because it assumes an arbitrary level of scaling can be performed to the device until the critical field strength is achieved in the lateral direction. The ratio of gate lengths between two materials needed to achieve the same power-frequency product would be equivalent, however, to the inverse ratio of the carrier velocities in the given materials. For instance, β-Ga_2O_3 gate lengths would need to be 0.44X the gate length in GaN for the same power-frequency product if the saturation velocity is already reached in both materials (the ratio

is worse if saturation has not been reached). It is well known that limitations exist on gate-length scaling in FET devices, and the nature of β-Ga_2O_3 MOSFETs exacerbates this problem as will be further discussed in Chapter 5.

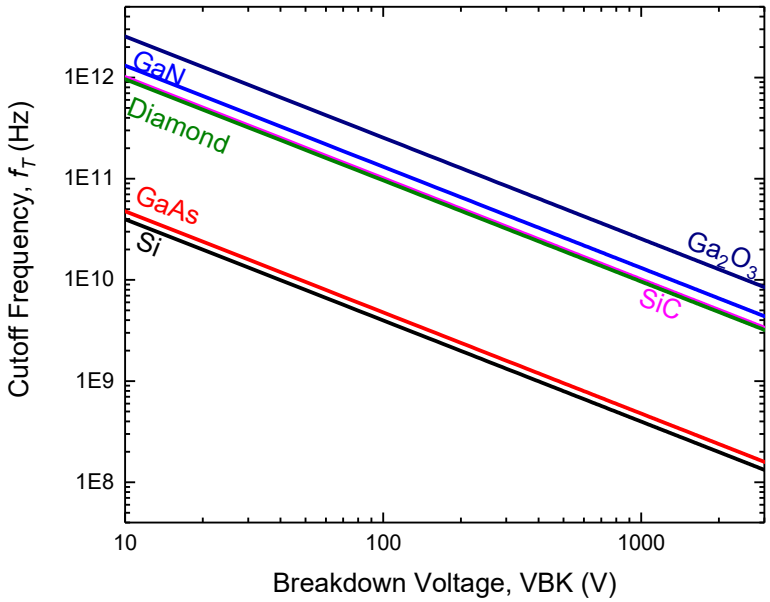
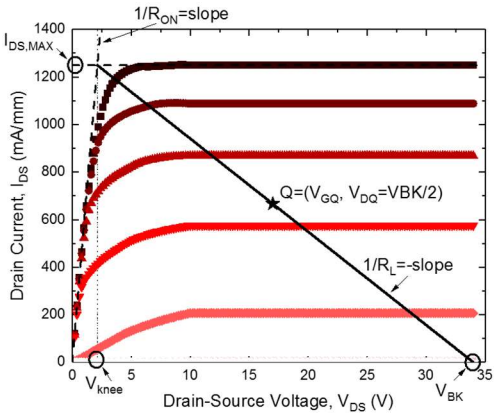


Figure 34 Benchmarking of different materials using Johnson's figure of merit which compares the cutoff frequencies at a given breakdown voltage to determine the ideal power-frequency product of the material system.

Given these difficulties in benchmarking the power-frequency product of different material systems, we instead focus on the operation of an RF amplifier as shown in Figure 35 and present state of the art results for GaAs and GaN devices for output power, P_{OUT}, drain efficiency, η_D, and power added efficiency, PAE, at given frequencies. It is evident from Figure 35 that β-Ga_2O_3 P_{OUT} and η_D values can be competitive based on the large critical field and large associated breakdown voltages. PAE performance which depends on the device gain is not immediately expected to compete with GaN because of

the much lower small signal gain at a given gate length as shown in Figure 36. These subjects will be discussed further in Chapter 7. For now, we present the GaN HEMT and GaAs MODFET, which other than the Si devices, which are primarily derived from logic devices and LDMOS devices already discussed, are the incumbent technologies for integrated power RF amplifiers. High frequency, but not high power, devices in materials such as InP will not be discussed.



$$P_{OUT,RF} = I_{DS,rms}^2 R_L = \frac{1}{8} I_{DS,MAX}^2 R_L = \frac{1}{8} I_{DS,MAX}(V_{BK} - V_{knee})$$

$$\eta_D = \frac{P_{OUT,RF}}{P_{IN,DC}} = \frac{1}{2}\left(1 + \frac{V_{knee}^2}{V_{BK}^2} - \frac{2V_{knee}}{V_{BK}}\right) \approx \frac{1}{2}\left(1 - \frac{V_{knee}}{V_{BK}}\right)$$

$$PAE = \frac{P_{OUT,RF} - P_{IN,RF}}{P_{IN,DC}} \approx \frac{P_{IN,RF}(G_M - 1)}{P_{IN,DC}}$$

Figure 35 Basic calculations for an example RF transistor acting as a power amplifier with Class A operation. The family of curves has been extended to the breakdown voltage of the device (34 V) for clarity. The RF output power, P_{OUT}, drain efficiency, η_D, and power added efficiency, *PAE*, can be estimated from the device performance from the parameters shown on the drain IV curves. The significance of the $Vknee/V_{BK}$ ratio and the device gain, G_M, are evident.

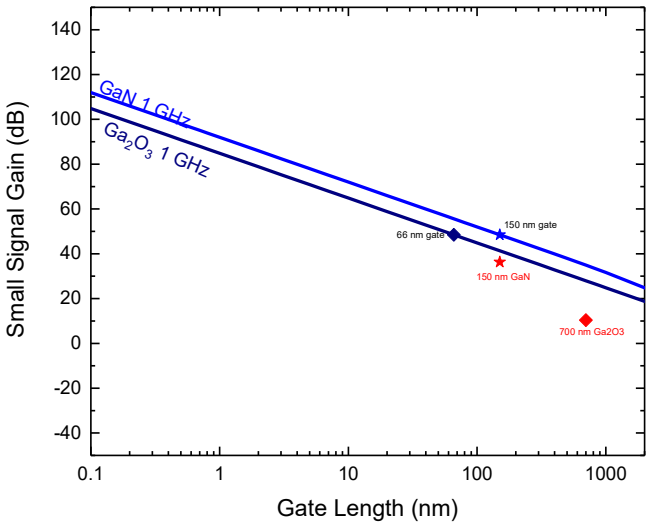


Figure 36 A comparison of the small signal gain vs. gate length for GaN and Ga_2O_3 technologies. At 1 GHz, the Ga_2O_3 device requires a gate length of 66 nm (navy diamond) to operate at the same small signal gain as the GaN device with gate length of 150 nm (blue star). The difference is related to the electron velocity in the material. Real device results are shown for a 150 nm GaN device operating at 1 GHz (red star) and a 700 nm Ga_2O_3 device operating at 1 GHz (red diamond). These results show some limitations related to Johnson's figure of merit which assumes an ultimate limit for the power-frequency product of a material if the gate length can be arbitrarily scaled.

A state of the art GaAs pseudomorphic HEMT (PHEMT), and its power performance are shown in Figure 37. GaAs devices like this one, operate using an extremely high mobility 2DEG channel that is formed without impurities by delta-doping the AlGaAs layer to provide carriers to the un-doped GaAs layer at the AlGaAs/GaAs heterojunction [125]. This device improves the confinement by adding indium to the channel layer (the pseudomorphic layer) creating a strained layer between the semi-insulating GaAs and AlGaAs. A number of fabrication process improvements are also employed [126], but these will not be further discussed here. The 100 nm gate length device with approximate source-drain spacing of 5 µm achieved a peak output power, P_{OUT}, of 2.4 W/mm at 30 GHz which is close to the value obtained using the calculations in Figure 35 (2.7 W/mm), and it achieved a gain of 3.6 dB which is somewhat smaller

than the predicted small signal gain of 5.42 dB. The *PAE* of this device, 44.6%, was very high for operation at 30 GHz; however, the bias condition of the device is not reported for clear comparisons.

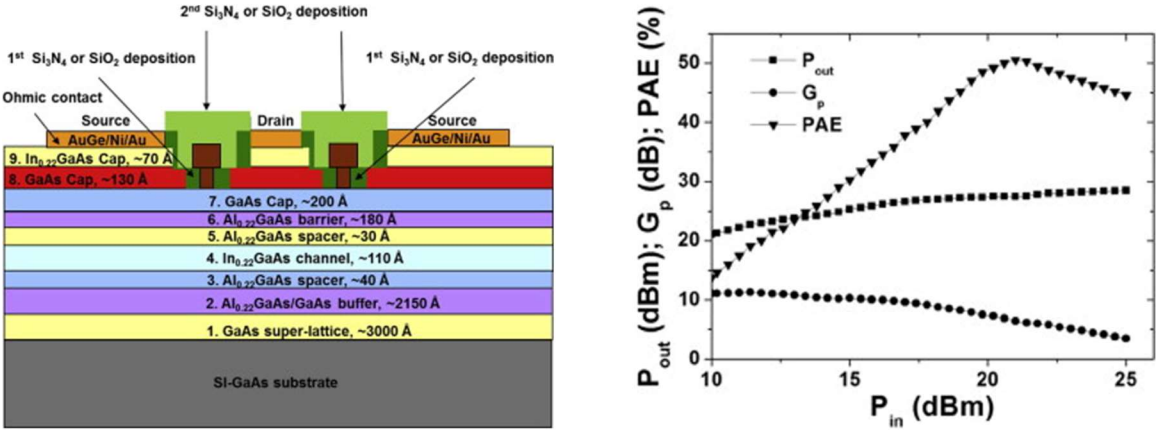


Figure 37 Left: A cross-sectional schematic diagram of an AlGaAs/InGaAs/GaAs PHEMT. Right: The measured output power, P_{out}, transducer gain, G_p, and power added efficiency versus input power, P_{in}, of an 8×(100×0.1) µm² gate periphery PHEMT device. Reprinted from [126]**, with permission from Elsevier. The measurement on the right is performed at 30 GHz with a bias voltage of 30 V.**

While GaAs PHEMT devices are widely used in commercial RF applications, GaN HEMT devices provide increased power-frequency performance in many cases and are thus expected to displace many GaAs and Si LDMOS devices in commercial applications as they mature. A state of the art GaN HEMT and its power performance are shown in Figure 38. The GaN device operates similar to the GaAs PHEMT; however, in most cases the 2DEG is not formed by doping and instead is formed by piezoelectric and spontaneous polarization induced charges at the AlGaN/GaN interface. The device shown in Figure 38, which is very similar to devices in our lab, also employs a thin AlN barrier to increase carrier confinement and a GaN cap layer to reduce the effects of surface states

[127]. The 300 nm gate length GaN HEMT with a 4 μm source-drain spacing pictured in Figure 38 recorded a peak output power, P_{OUT}, of 14.2 W/mm which is comparable to the expected P_{OUT} (14.6 W/mm at the given bias conditions) from the equations in Figure 35. Additionally, the GaN HEMT power gain, G_p, was 8 dB versus a prediction of 9 dB from the small signal values, and the peak *PAE* was 48% which is difficult to calculate because the bias was not in Class A operation. The GaN HEMT is currently the leader in power-frequency product for any known material system surpassing Si, GaAs, and SiC due to the high mobility obtained in the 2DEG and the high breakdown field strength of GaN [125].

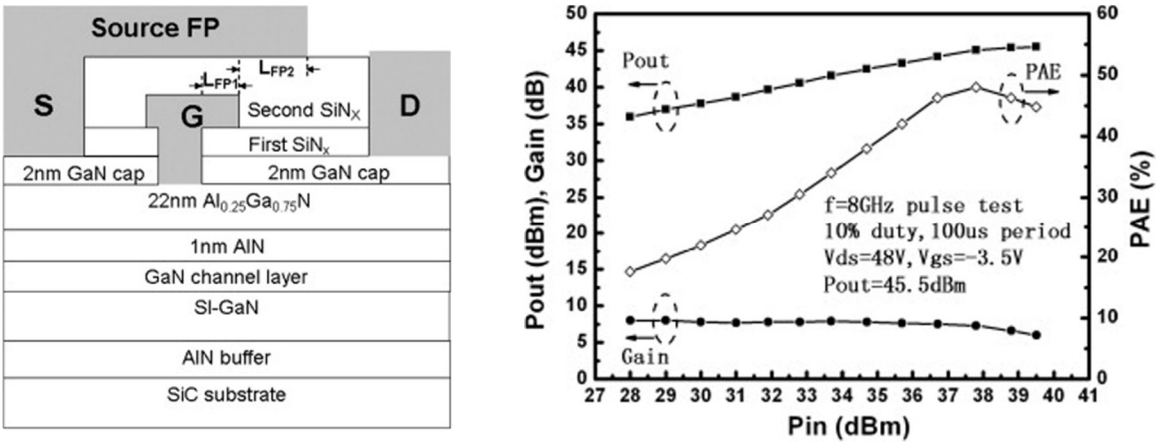


Figure 38 Left: The cross-sectional schematic of AlGaN/GaN HEMT device on SiC substrates. Right: Microwave power characteristics of 2.5 mm internally-matched GaN HEMT at 8 GHz. Reprinted from [127]**, with permission from Elsevier.**

Since power performance depends heavily on bias conditions/class of operation, operating frequency, and fabrication process parameters (lateral spacing) which can change breakdown voltages, further analysis of specific devices would become mundane.

Instead, we move back to the discussion of β-Ga_2O_3 by summarizing state of the art results obtained from the literature and by laying out a path to improve these results toward predicted theoretical values.

β-Ga_2O_3 Device Summary

Only a handful of relevant β-Ga_2O_3 FET devices have currently been reported in the literature with some results presented in Table 6. While high breakdown voltage, has been realized, only the MOSFET device presented by Green et al. achieved a higher critical field strength than GaN and SiC although this has also been achieved on some non-FET structures [92], [128]. In the remaining chapters we create a simple analytical model for these β-Ga_2O_3 FET devices and then analyze that model to determine the limitations and capabilities that can be achieved through use of similar devices in the β-Ga_2O_3 material system toward high power switching applications and integrated RF performance. Before doing this we present an excellent analysis by Green et al. in [92] that benchmarks his device (row 3 of Table 6) and lays out a path to achieving theoretical performance of β-Ga_2O_3 MOSFETs in relation to conduction losses. The paper by Green et al. concludes that the critical field must be maximized to near the theoretical value (Green's device achieves 3.8 MV/cm compared to the theoretical value of 8 MV/cm), that the parasitic resistances from the ohmic contacts and access region sheet resistances must be reduced to a minimum through advanced ohmic contacts and self-aligned source technology, and that the mobility must be improved to nearer the theoretical value (Green's device achieved a mobility of only 19.7 $cm^2/(V \cdot s)$ compared to the theoretical maximum of 150-300 $cm^2/(V \cdot s)$ at room temperature [47], [49]) to achieve the ultimate

potential of β-Ga_2O_3 MOSFETs for power switching applications. These values are already being improved in real devices as we will see in our analysis of devices in Chapter 5 and the analysis of our model in Chapter 6.

Table 6 A summary of published β-Ga_2O_3 FETs developed for power electronic applications.

Channel Type (method)	Device	N_d[a]	μ_n[b]	IDSS[c] (L_G)	V_{BK}[d] (G-D spacing)	RT I_{ON}/I_{OFF} (V_{off}[e])
Sn (MBE) [82]	MOSFET	$3.0x10^{17}$	NR	26 (2 µm)	370 (NR)	$>10^{10}$ (-15 V)
Sn (MOVPE)[92]	MOSFET	$4.8x10^{17}$	19.7	60 (2 µm)	200 (0.6 µm)	10^7 (-30 V)
Si (implant)[129]	FP-MOSFET	$3.0x10^{17}$	70-95	75 (2 µm)	755 (15 µm)	$>10^9$ (-36 V)
Sn (bulk)[91]	NM-MOSFET	$2.7x10^{18}$	48.8	150 (0.85 µm)	NR (0.85 µm)	10^{10} (-110 V)
Sn (bulk)[91]	NM-MOSFET	$2.7x10^{18}$	55.2	E-mode (1.3 µm)	185 (0.9 µm)	10^{10} (0 V)
Sn (MOVPE)[130]	WG-MOSFET	$2.3x10^{17}$	24	E-mode (2 µm)	612 (21 µm)	$>10^5$ (0-1 V)

[a]active carrier concentration in cm^{-3}, [b]effective mobility in $cm^2/V{\cdot}s$, [c]saturated drain current at gate voltage of 0 V in mA/mm, [d]three terminal breakdown voltage (total drain-source voltage) in V, [e]off-state voltage in V, FP=Field plated, NM=Nanomembrane, WG=Wrap gate, RT=Room temperature (300 K)

4. ANALYTICAL MODELING OF GALLIUM OXIDE MOSFETS

In this chapter, we introduce a simple analytical model for β-Ga_2O_3 transistors that will be verified with actual devices in Chapter 5. First though, we set the stage with a brief overview of general transistor modeling for RF and power devices and provide examples of model development for GaN HEMTs and Silicon MOSFETs.

Power and RF device Modeling Types

During the development cycle of a new material system, such as β-Ga_2O_3, many different types of modeling are used. In chapter 2, we described many physical models based on the crystal structure of β-Ga_2O_3. These models and experimental results supporting them are used to evaluate the β-Ga_2O_3 material system compared to other semiconductor materials such as was done in Table 4 at the end of Chapter 2. It is impractical from a time and computing cost standpoint to scale these atomistic models which are often performed at the scale of one or a few crystallographic unit cells assumed to extend infinitely [44][131] up to the macroscale of actual electronic devices with numerous boundaries between materials. Instead, the results of these physical atomistic models can be used as inputs to device models that are used to predict the expected results and analyze the design of β-Ga_2O_3 devices. Both types of models are simplified by numerous assumptions, and the number of these simplifications is directly related to the trades made between accuracy and computing cost. When a device is evaluated using a

device model, any discrepancies in the results should be appropriately addressed against the model. First, the assumptions made in the device model should be evaluated, and then, only after that evaluation, should the material parameters and the assumptions made in determining them be evaluated. Only very rarely will a new theory be needed to explain the new technology. Thus, we begin our gallium oxide modeling with the previously accepted electrostatic theories for semiconductors.

For β-Ga_2O_3, the primary device to be modeled is a depletion-mode MOSFET as described at the end of Chapter 3. Complex device related technology computer aided design (TCAD) modeling of this type of device has been performed in only a few instances [75], [132][133]. This type of modeling uses full three dimensional solutions of continuity PDEs including Poisson's equation, drift-diffusion equations, and electro-thermal equations to determine device function [134]. Device TCAD usually uses a finite element analysis method to solve continuity partial differential equations (PDEs) across boundaries in a mesh formed over the physical structure of the device. While mesh details are not at the atom level as in previously described atomistic models, the macroscale devices modeled can cause the computing cost to be high (hours to days, large amounts of memory used) especially when several simple device variations are evaluated.

Analytical models provide further simplification of the three dimensional Poisson's equation allowing closed form or simple iterative solutions. Device operation can still be predicted to a level that allows rapid assessment of many different device variations but at much lower computing costs (seconds or minutes, register memories).

Discrepancies between measured and predicted values can be compared over large sample sizes to evaluate the sources of errors and increase confidence in model results instead of using more detailed measurement techniques. Additionally, simple equation based analytical models allow rapid design of experiments for material assessment and device improvements (including scaling). Finally, the low computing cost of analytical models allows them to be quickly converted from the material development stage to the circuit design stage when the material is mature enough for circuit use. In the last section of this chapter, we develop a simple analytical model to predict the performance of a wide range of β-Ga_2O_3 depletion-mode MOSFETs, but first, we briefly look at the progress and use of analytical models for Si and GaN devices.

Before doing that, however, it is important to mention another type of model used for power and RF devices, namely the empirical model (sometimes called nonlinear). Small and large signal RF models used in circuit designs are often directly extracted from the devices themselves to ensure accuracy in the RF domain. When operating at high frequencies, parasitic elements from the device layout can become very important and extensive electromagnetic or statistical empirical modeling becomes necessary. RF circuit designers are, thus, often provided a small or large signal model created from empirical measurements on the specific device layout they are designing with. The empirical data in the model is fit to nonlinear mathematical equations that are presumed to best model the device operation over the range of operating conditions that will be used in the circuit [135]–[137]. These types of models have not been extracted yet for Ga_2O_3, but numerous

techniques exist [138] and can be combined with analytical techniques for RF circuit design success as will be mentioned in the next section.

GaN and Si Analytical Models

Silicon analytical models are in widespread use for instruction, circuit design, and statistical analysis of fabrication processes. Because of the vast silicon transistor markets, mature TCAD is also available to accurately predict fabrication process results and final device operation [134], [139]–[142]. Refinements in the form of tweaks to empirical constants obtained for physical analytical functions within the models to both types of model are often made only after analysis of large amounts of statistical data. Analytical silicon models can be divided into three groups; charge based, threshold voltage, and surface potential models [143]. Rather than conducting a full solution of the 2- or 3-dimensional (2D or 3D) continuity PDEs to obtain specifics of the underlying physics associated with a device, as is performed in TCAD, analytical models simplify these equations into multiple 1D solutions. A simplified solution of a silicon MOSFET was provided by Pao and Sah in 1966 [144]. This equation reduced the 2D solution to the drift-diffusion equation to two 1D solutions, in the *x* direction vertically through the channel (input voltage equation), and in the *y* direction laterally along the channel (output current equation), by employing what is called the **gradual channel approximation**. The gradual channel approximation is a simplification that assumes the electric field in the vertical direction of a MOSFET is not largely affected by the electric field in the lateral direction. In other words, the lateral potential changes gradually compared to the vertical field which controls the current flow. While Pao and Sah's double integral solution is

highly physical, it still has a high computing cost because it requires a numerical solution, thus for MOSFETs, other simplifications are often made [143].

Another important assumption made in the analytical modeling of Si MOSFETs is that near an interface the charge density is dominated by ionized donors and acceptors and not by free electrons and holes except for in a very narrow region immediately next to the interface. This assumption known as the **depletion approximation** allows for a simplified solution to Poisson's equation for the band-bending in a semiconductor interface with another material. Finally, Si MOSFET analytical models often assume that the majority carriers are found in a thin charge sheet near the surface of the semiconductor. This **charge sheet model** allows the depletion approximation to be extended into the region of strong inversion when the MOSFET majority carrier channel is formed and allows a closed form analytical expression for MOSFET operation in the subthreshold, linear, and saturation regions [1].

Recently, analytical compact models have been sought for GaN HEMT devices for accurate circuit design models. These models are normally surface potential based models that rely on mathematical smoothing functions to connect the piece-wise equations obtained from several regions of device operation[145]–[147]. The models typically use a triangular quantum well approximation to obtain the available energy states of electrons in the 2DEG at the AlGaN/GaN interface. Then, piece-wise solutions are obtained for the surface potential below the bottom of the triangular well, between the bottom of the well and the first available state, above the first available state, and sometimes in a state when carrier confinement by the quantum well is reduced. These

analytical models can be used with more established small signal model extraction techniques to predict small and large signal performance for GaN HEMT devices [148]. The GaN analytical models (and TCAD simulations as well) have lagged the development of GaN devices and circuits and have still not been largely implemented in the community as have the silicon MOSFET analytical (and TCAD) models. This means that GaN devices have been developed somewhat blindly with device developers lacking the benefit of evaluating results quickly against an accepted and reliable model. In the next section, we introduce an early simple model for β-Ga_2O_3 leveraging work in GaN and Si to ensure that the gallium oxide material system does not proceed in a similar manner.

Analytical Model for β-Ga_2O_3 MOSFETs

Lateral β-Ga_2O_3 depletion mode MOSFETs such as those investigated here have operation similar to junction field effect transistors (JFETs) whereby a lateral channel is completely modulated by a depletion region underneath the gate. The difference in these devices is an added gate oxide layer and extremely low probability for the formation of a conducting inversion layer due to heavy hole mass as explained in Chapter 2. We start with the basic equation for the drain current[1], Equation 12.

Equation 12 Basic equation for the drain current from [1]. The total channel charge per unit area, *Q*, is multiplied by the width of the channel, *W*, and the velocity, *v*, in m/s. The velocity can be interpreted as the mobility, μ, in $m^2/(V \cdot s)$ multiplied by the lateral electric field along the channel, *E(y)*, in V/m. Finally, *E(y)* is the negative differential voltage along the channel, *dV/dy*.

$$I_{DS} = -QWv = -QW\mu E(y) = QW\mu\frac{dV}{dy}$$

The calculations are then simplified using the requirement for current continuity along the channel with the gradual channel and depletion approximations to obtain a simple analytical expression for the drain current. To do this, we assume that the current is dominated by drift current in the depletion and accumulation modes because of the junction-less (n-n-n type) lateral structure. The total channel charge per unit area, Q, is given in Equation 13 which can be used with the depletion distance, Equation 14, and surface potential, Equation 15, to solve Equation 12. The surface potential is extracted from the band structure illustrated in Figure 39. The final solution for I_{DS} is obtained by ignoring the accumulation charge, Q_{acc}, and integrating from source to drain to obtain an equation valid for drift current when $V_G < V_{FB}$. First, however, we need to obtain the voltage drop across the gate oxide, V_{ox}, from Gauss's law, and the flat-band voltage from the Schottky-Mott rule as shown in Equation 16 and Equation 17, respectively. The final integrated solution for I_{DS} is shown in Equation 18.

Equation 13 Channel charge per unit area. N_d is the active carrier concentration in the channel, q is the electron charge, d is the thickness of the channel layer, and x_{dep} is the thickness of the depletion region. Q_{acc} is an added charge if the device is in accumulation.

$$Q = N_d q\big(d - x_{dep}(y)\big) + Q_{acc}$$

Equation 14 Depletion distance at a point along the gate length. N_d is the active channel carrier concentration, q is the electron charge, ε_s and ε_0 are the relative permittivity of the semiconductor and the permittivity of free space, respectively, and $\Psi_s(y)$ is the surface potential along the channel.

$$x_{dep}(y) = \sqrt{\frac{2\varepsilon_s\varepsilon_0\Psi_s(y)}{qN_d}}$$

Equation 15 Surface potential at a point along the gate length calculated from the flat-band voltage, V_{FB}, the gate voltage, V_G, and the voltage across the gate oxide, V_{OX}. The gate voltage has been modified for changes along the gate length by using V_G-$V(y)$ where $V(y)$ is $E(y)$*y, a voltage potential along the channel.

$$\Psi_s(y) = V_{FB} - \big(V_G - V(y)\big) - V_{OX}$$

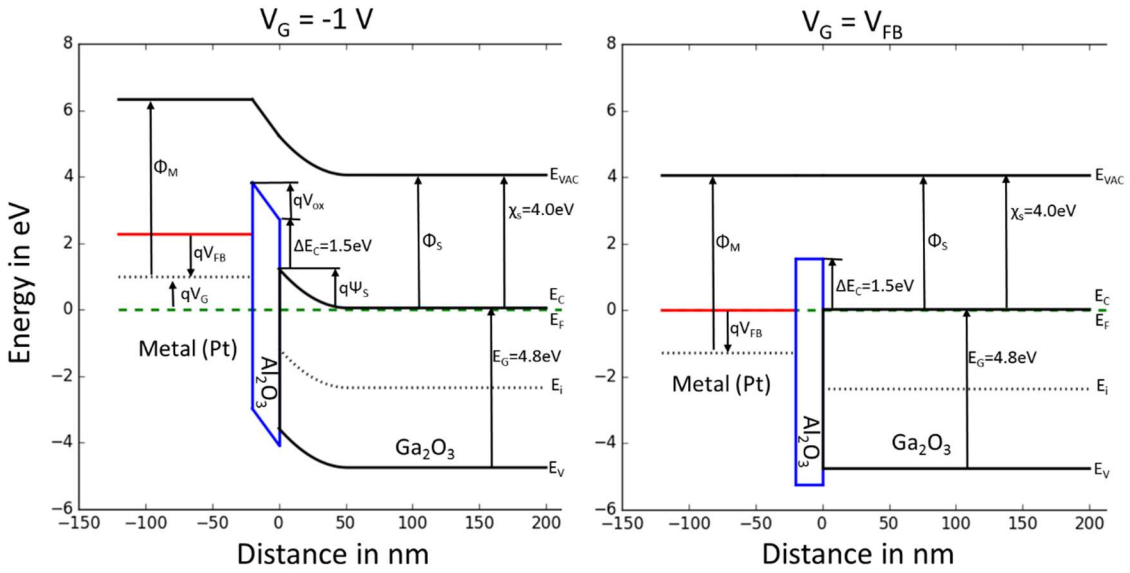


Figure 39 Band structure for the metal-oxide-semiconductor junction of a β-Ga_2O_3 MOSFET biased at V_G=-1 V (left) and V_G=V_{FB} (right). The fermi level at the flat-band voltage is shown at 0 eV and the oxide-semiconductor junction is shown at x=0 nm. Created from a solution of Poisson's equation assuming the values from [97], [132], **and Figure 1 for ΔE_C, χ_s, and N_C, respectively, as detailed in Appendix A: Python code for Bandstructure.**

Equation 16 Voltage drop across the gate oxide for a β-Ga_2O_3 MOSFET from Gauss's law. The relative permittivity of the oxide, ε_{OX}, multiplied by the electric field at the oxide surface is equal to the relative permittivity of the β-Ga_2O_3, ε_s, times the electric field at the β-Ga_2O_3 surface, $E_s(x=0)$. t_{OX} is the thickness of the oxide, q is the electron charge, N_d is the active carrier concentration in the β-Ga_2O_3, x_{dep} is the vertical depletion distance into the channel, C_{OX} is the oxide capacitance per unit area, and ε_0 is the vacuum permittivity.

$$V_{OX} = \frac{E_s(x=0)\varepsilon_s t_{OX}}{\varepsilon_{OX}} = \frac{qN_d x_{dep}(y)}{C_{OX}} = \frac{\sqrt{2q\varepsilon_s\varepsilon_0 N_d \Psi_s(y)}}{C_{OX}}$$

Equation 17 Flat-band voltage for a β-Ga_2O_3 metal-oxide-semiconductor junction from Schottky-Mott theory. The flat band voltage is equal to the difference between the metal work function, Φ_M, and the β-Ga_2O_3 work function, Φ_S. The work function of β-Ga_2O_3 is equivalent to the electron affinity, χ_S, added to the difference between the conduction band edge and the fermi level, i.e. the natural log of the conduction band density of states, N_C, divided by the active carrier concentration, N_d.

$$V_{FB} = \Phi_M - \Phi_S = \Phi_M - \left(\chi_S + \ln\left(\frac{N_C}{N_d}\right)\right)$$

Equation 18 Drain current equation for the depletion region of a β-Ga_2O_3 MOSFET by integration across the source-drain region using Equation 12 with Equation 13 through Equation 17. V_{DS} is the drain-source voltage and L is the gate length. The other variables are explained within the equations mentioned.

$$I_{DS} = \frac{qN_d\mu W}{L}\left\{V_{DS}\left(d + \frac{\epsilon_s}{C_{OX}}\right) + \frac{2}{3}\sqrt{\frac{2\epsilon_s}{qN_d}}\left[(A^2 - V_{GS} + V_{FB})^{3/2} - (A^2 - V_{GS} + V_{FB} + V_{DS})^{3/2}\right]\right\}$$

$$A = \frac{\sqrt{2\epsilon_s qN_d}}{2C_{OX}}$$

From Equation 14, Equation 15, and Equation 16, two valid solutions to Ψ_S exist. For Equation 18, however, only a single solution is needed because this solution gives the correct value in Equation 18 for the off-state voltage, V_{off}, which is the point when the entire channel layer becomes depleted ($x_{dep}(0)=d$) as shown in Equation 19.

Equation 19 Off-state voltage condition for a β-Ga_2O_3 MOSFET. The condition is reached when the gate voltage equals the off-state voltage, $V_G=V_{off}$, where V_{off} is the point when the entire active channel is depleted, $x_{dep}=d$, at the source side of the gate. V_{FB} is the flat-band voltage, d is the thickness of the channel, N_d is the active carrier concentration, q is the electron charge, C_{ox} is the gate oxide capacitance per unit area, and $\epsilon_s*\epsilon_0$ is the permittivity of β-Ga_2O_3.

$$V_{off} = V_{FB} - dqN_d\left(\frac{d}{2\epsilon_s\epsilon_0} + \frac{1}{C_{OX}}\right)$$

The drain current equation, Equation 18, is valid only in the linear part of the depletion region ($V_{off}<V_{GS}<V_{FB}$ and $V_{DS}<V_{sat}$); however, assuming the gradual channel approximation holds (i.e. the gate length is long enough and short channel effects do not dominate), we can approximate the saturation characteristics by simply using $V_{DS}=V_{Dsat}=V_{GS}-V_{off}$ for any $V_{DS}>V_{GS}-V_{off}$. This approximates a perfect saturation condition and makes the I_{DS} equation valid anywhere in the depletion region ($V_{off}<V_{GS}<V_{FB}$).

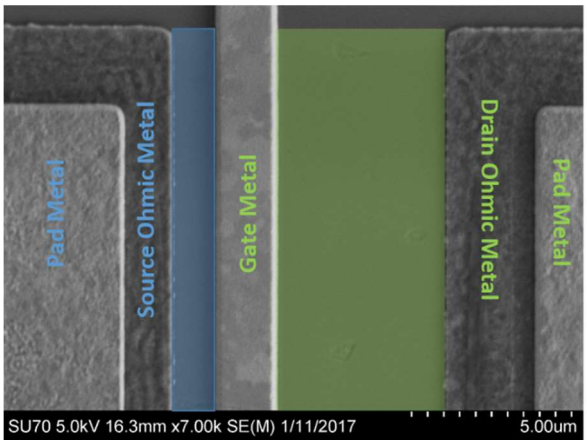


Figure 40 Scanning electron microscope (SEM) image of the source-drain region of a β-Ga_2O_3 MOSFET. The typical device layout has an access region (light blue) between the source ohmic metal and the gate metal for the source contact and an access region (light green) between the gate metal and the drain ohmic metal for the drain contact.

Equation 18 accounts for the current under the β-Ga_2O_3 MOSFET gate, however, as shown in Figure 40, typical β-Ga_2O_3 MOSFETs do not use a self-aligned gate process. Because the devices can have large sheet resistances, these gate-source (G-S) and gate-drain (G-D) access regions can exhibit large resistances. Additionally, the source and drain ohmic contacts themselves can have non-negligible resistances. As current increases, the voltage drop across these resistances, becomes significant and increases the

on-resistance, R_{ON}, of the device. Additionally, the G-S access region changes the value of the source voltage seen at the source edge of the gate leading to $V_{GS}=V_{GS}-I_{DS}*R_{access}$ (where R_{access} is the total resistance of the access region) and reducing the current level where saturation occurs ($V_{Dsat}=V_{GS}-I_{DS}*R_{access}-V_{off}$). This effect can be easily modeled by placing an equivalent resistor at the source and drain side of the I_{DS} model (Equation 18); however, the solution must be made by iteratively solving Kirchoff's current and voltage laws because the current is determined by the voltage and vice versa. A simple way to implement this iterative solution was to use the Verilog A coding language [149] with a commercially available Verilog A simulator known as TINA [150] as shown in Figure 41. The measured ohmic contact resistance and the access region resistance calculated from the measured sheet resistance and mobility as shown in Equation 20 are placed in series with the MOSFET I_{DS} model to obtain the full solution for an extrinsic (i.e. including the parasitic resistance) β-Ga_2O_3 MOSFET in the depletion region.

In accumulation, the surface potential equation, Equation 15, has a sign change which leads to difficulty in obtaining a continuous solution. To keep the model simple, a piecewise solution is implemented by using the charge sheet approximation for the additional accumulation charge as shown in Equation 21. An additional accumulation current can be calculated (Equation 22) from this charge, and summed with the maximum depletion current, Equation 18 with $V_{GS}=V_{FB}$. This is a simplified method for extending the model into the accumulation region which has been implemented in the VerilogA code in Appendix C: VerilogA Code For Drain Current. A more complicated model

assuming filling of the conduction band density of states was implemented using Python code; however, the difference in the results for small forward bias are negligible.

This completes the basic electrostatic model for β-Ga_2O_3 MOSFETs that will be verified and updated using real devices in Chapter 5. In Chapter 6, we will look at some of the implications on device performance from this model and the nature of the devices themselves. We will also note some of the limitations of the model and show ways the model can be improved as more empirical data is incorporated in Chapter 6.

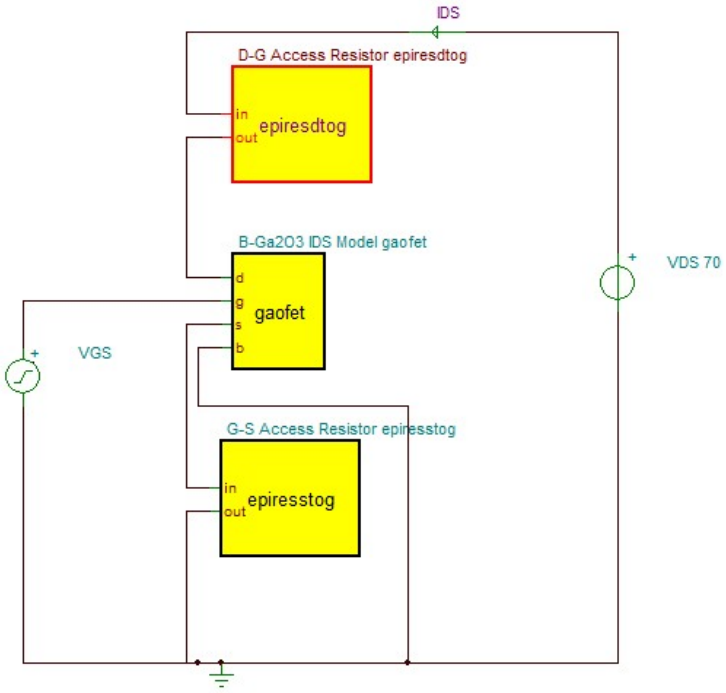


Figure 41 VerilogA [149] **model of a β-Ga_2O_3 MOSFET in the TINA circuit simulator** [150]**. The drain current, *IDS*, gate bias, *VGS*, and supply voltage, *VDS*, are shown. The extrinsic resistance from the G-S spacing is represented by the bottom resistor model (bottom yellow box, "epiresstog"), the extrinsic resistance from the D-G spacing is represented by the top resistor model (top yellow box, "epiresdtog"), and the drain current is represented by the middle "gaofet" model (middle yellow box). VerilogA code for the access resistors can be found in Appendix B: VerilogA Code for Access Resistors and for the drain current in Appendix C: VerilogA Code For Drain Current.**

Equation 20 Access region resistor for the drain-gate or gate-source access region in a β-Ga_2O_3 MOSFET. The measured contact resistance, R_C, in Ω-mm divided by the gate width, W, in mm is combined with the sheet resistor calculated from the measured active carrier concentration, N_d, or from the measured sheet resistance, R_{SH}, in Ω/□. L_{XY} is the length of the access region, q is the electron charge, d is the channel thickness, and μ is the effective carrier mobility.

$$R_{access} = \frac{R_C}{W} + \frac{L_{XY}}{W d q \mu N_d} = \frac{R_C}{W} + \frac{R_{SH} L_{XY}}{W}$$

Equation 21 Charge sheet approximation of the accumulation charge. The oxide capacitance per unit area, C_{OX}, is multiplied by the accumulation voltage which is the amount of gate-source voltage, V_{GS}, above the flat-band voltage, V_{FB}.

$$Q_{acc} = C_{OX}(V_{GS} - V_{FB})$$

Equation 22 Accumulation current for a β-Ga_2O_3 MOSFET based on the charge sheet approximation. The effective carrier mobility, μ, is multiplied by the lateral field equal to the drain-source voltage, V_{DS}, divided by the gate length to obtain the velocity. The velocity is multiplied by the accumulation charge, Equation 21, and the width of the device, W, to obtain the accumulation current.

$$I_{DS,acc} = \mu \frac{V_{DS}}{L} W C_{OX}(V_{GS} - V_{FB})$$

5. MODEL VERIFICATION AND IMPROVEMENTS

In this chapter, we present results on fabricated β-Ga_2O_3 MOSFETs and compare them to the model presented in Chapter 4. Improvements are made or suggested for the model to make it applicable for unique phenomena found in the β-Ga_2O_3 material system. In the next chapter, we will address the implications of the results presented here and discuss the limitations of the current analytical model.

Doping Variation of β-Ga_2O_3 MOSFETs

To verify our model accuracy for changes in doping concentration, MOSFETs were fabricated on single crystal β-Ga_2O_3 grown by MBE on commercially available Fe-doped (010) semi-insulating substrates [47]. Sn-doping was performed during the epitaxial growth and carrier concentrations from 0.7 x 10^{18} to 1.6 x 10^{18} cm^{-3} were measured after growth using electrochemical capacitance voltage (C-V) measurements. Table 7 includes these values as ***N_d As Grown*** and also summarizes the measured data for all samples with doping variation as described further throughout this section.

Table 7 Sample summary of β-Ga_2O_3 MOSFETs with different doping concentrations.

N_d As Grown[a]	V_{knee}[c]	IDSS[d]	V_{off}[c]	N_d Post Process [a]	μ_{eff} [b]	$IDSS_{mod}$[d]	$IDSS_{mod\ \Delta V_G}$[d]	$V_{knee\ mod\ \Delta V_G}$ [c]	R_C[e]
$0.70x10^{18}$	13.0	19	-9.6	$2.50x10^{17}$	74.5	36.5	20.5	12.9	80.0
$1.00x10^{18}$	33.9	111	-18.8	$4.84x10^{17}$	58.3	136.1	111.2	35.8	32.0
$1.30x10^{18}$	53.7	235	-24.5	$6.29x10^{17}$	52.4	258.8	235.4	54.7	14.0
$1.60x10^{18}$	69.6	381	-30.8	$7.88x10^{17}$	51.0	404.6	381.4	71.0	10.7

[a] cm^{-3}, [b] $cm^2/V \cdot s$, [c] V, [d] mA/mm, [e]Ohm-mm

A schematic process flow for the MOSFET is shown in Figure 42. Mesa isolation of the active channel was conducted using a BCl_3 inductively coupled plasma (ICP) dry etch and verified by profilometer measurement. Source and drain ohmic contacts were formed using an evaporated Ti/Al/Ni/Au metal stack and annealed for 60 sec in a nitrogen ambient at 470 ºC [82]. All contacts were ohmic and contact resistance (R_C) ranged from 10.7 to 80.0 Ω-mm as measured by circular transfer length method (TLM) [151] and shown in Table 7. A 20 nm thick gate dielectric layer of HfO_2 was deposited by plasma-enhanced atomic layer deposition (ALD) at 250 ºC without any surface pre-treatment. The gate dielectric was selectively removed in the ohmic pad regions by CF_4 reactive ion etching (RIE). Interconnects and 2-µm long gates were patterned and deposited simultaneously using a 20/480 nm Ti/Au metal stack.

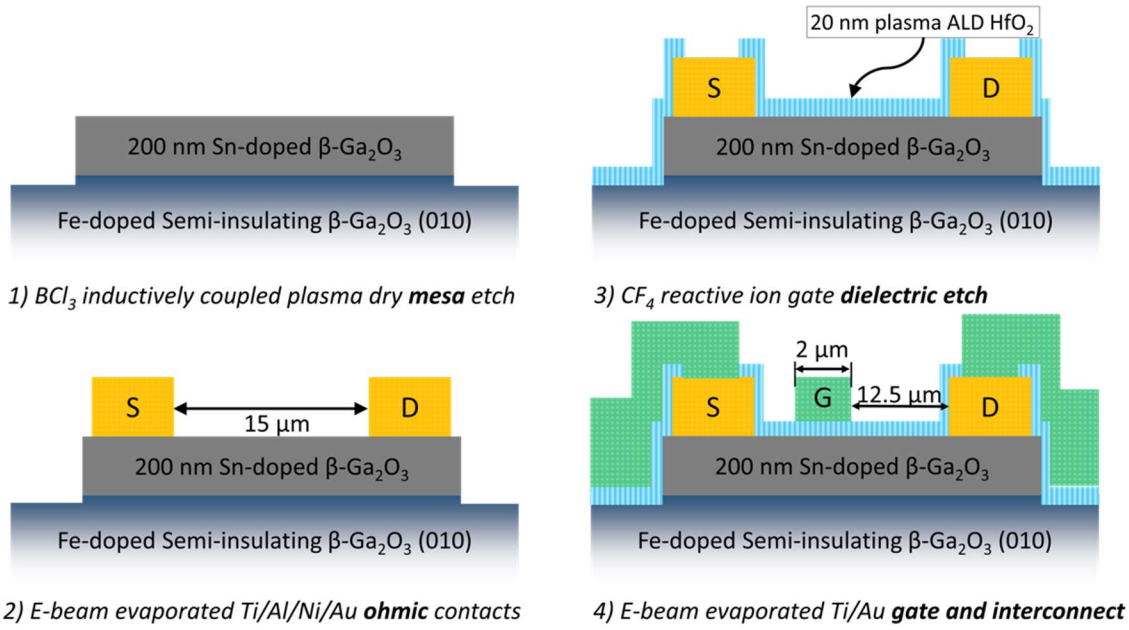


Figure 42 Mesa first process flow for β-Ga_2O_3 MOSFETs used for verification of analytical model.

All device electrical testing for different doping levels was conducted on self-isolating ring-type MOSFETs with a gate-source spacing of 0.5 μm and a total source-drain spacing of 15 μm (12.5 μm G-D spacing). The total gate width was 422 μm. All structures were fabricated on a single 10 mm x 15 mm sample for each doping level mentioned above. Figure 43 shows an example static log transfer curve (I_D-V_{GS}) for the highest current density MOSFET with good transistor operation including a high on/off current ratio of $>10^8$ which was typical of all devices measured regardless of the carrier concentrations listed in Table 7. Sister devices routinely achieved breakdown voltages >400 V for a 10.5 μm gate-drain spacing and were limited by failure of the gate dielectric indicating that the doping concentration difference did not affect the critical field at the levels investigated.

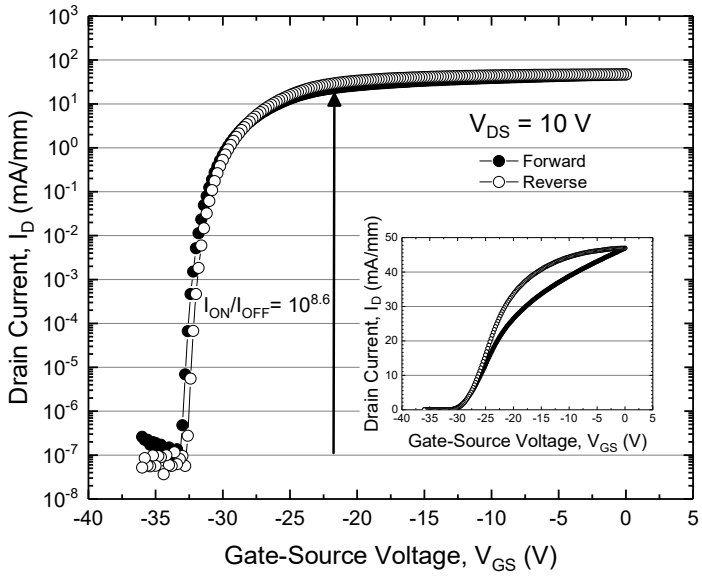


Figure 43 DC log transfer curve for a high current density β-Ga_2O_3 MOSFET showing good transistor operation. The inset is a linear plot of the transfer curve showing significant gate dispersion between forward and reverse curves.

Pulsed-IV measurements were conducted on MOSFET devices using an AMCAD system to provide a pulsed drain voltage and a Keysight E5270a to provide static gate bias. Pulse widths were 200 ns with a quiescent drain bias of 0 V and a low duty-cycle of 0.001 percent to minimize thermal effects. The pulsed measurement used represents an ideal environment where gate and drain dispersion and self-heating effects can be ignored to evaluate the β-Ga_2O_3 MOSFET analytical model under ideal conditions and assess the material system. Figure 44 shows a pulsed-IV and static family of curves (I_D-V_{DS}) for the highest current density device (Row 5 of Table 7). We extracted the knee voltage, V_{knee}, and the saturated drain current at V_G=0 V, I_{DSS}, from the inflection point in the pulsed-IV family of curves as shown in Figure 44. ***V_{knee}*** and ***IDSS*** are recorded for all doping variations in Table 7.

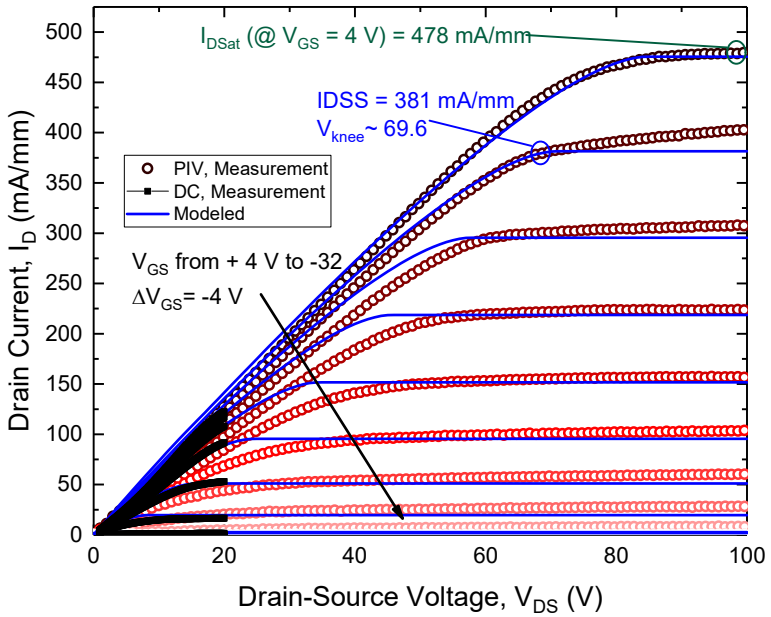


Figure 44 Pulsed family of drain current curves (symbols) for a high current density β-Ga_2O_3 MOSFET. The maximum current density measured was 478 mA/mm. The device operates very close to theoretical values shown using the analytical electrostatic model from Chapter 4 (blue lines). Gate dispersion was avoided by

measuring from the on to off states. A static measurement limited to V_{DS}=20 V and V_{GS}=0 V is also shown with a maximum current of 118 mA/mm @ V_{DS}=20 V and V_{GS}=0 V which agrees with the pulsed measurement (120 mA/mm @ V_{DS}=20 V and V_{GS}=0 V) and model.

To compare the results to the model presented in Chapter 4, we required a method to accurately evaluate the flat-band voltage, V_{FB}, and the active carrier concentration, N_d, for each sample listed in Table 7. Hall effect measurements were unfortunately not available for these samples after fabrication. Instead, we used capacitance-voltage (C-V) characteristics of the channel layers to obtain these values. C-V measurements were performed on lateral C-V structures with diameters of 75, 100, and 125 μm using a B1505a equipped with a multi-frequency capacitance measurement unit (MFCMU) and needle probes. A representative C-V curve for each sample is presented in Figure 45. Measurements were performed at frequencies that provided smooth C-V characteristics (100 kHz or 1 MHz), and measurement differences at frequencies between 1 kHz and 1 MHz were confirmed to have negligible effect on the experimental results. We used the C-V measurement data to determine the off-state gate voltage, V_{off}, from the inflection point where the C-V curve (and therefore the available drift carriers) are minimized. This inflection point is shown for one device in Figure 45, and $\boldsymbol{V_{off}}$ is recorded for all samples in Table 7. From this value, we obtained N_d (and V_{FB}) by solving Equation 19 iteratively starting from the maximum value of $V_{FB}=\Phi_M-\chi_S$ in Equation 17. The result obtained is an average of N_d through the active layer thickness of each sample, and it is recorded in Table 7 as $\boldsymbol{N_d}$ ***Post Process***. The difference between the carrier concentration before and after fabrication results from depletion of carriers at the epitaxy-substrate interface during processing and surface effects at the gate oxide-gallium oxide interface. The average

value extracted from V_{off} agrees reasonably with average values extracted from post-process C-V profiling (Figure 46); however, C-V profiling is unreliable near the gate oxide-gallium oxide interface.

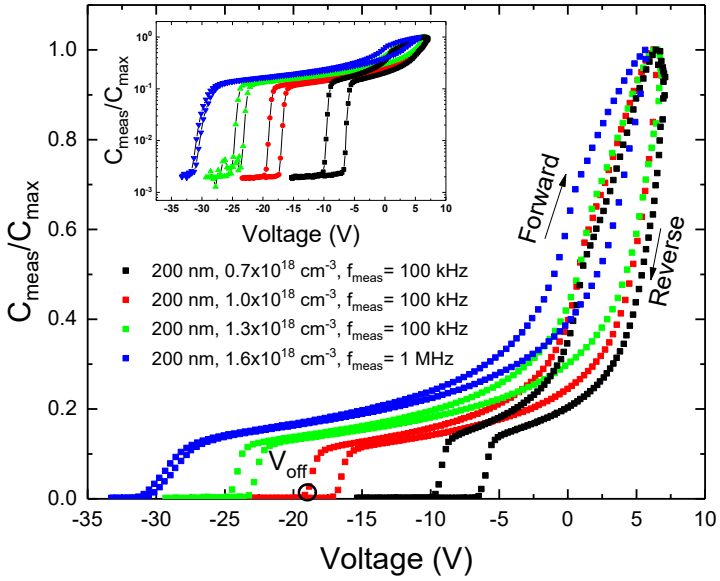


Figure 45 Normalized capacitance vs. voltage, C-V, for MOS structures on MBE grown β-Ga_2O_3 homoepitaxial layers with varying target doping and 200 nm active layer thickness. The inset shows log scale plots of the same. The inflection point used to determine the off-state voltage, $V_{off,}$ is shown for one device. All samples had HfO_2 gate dielectric.

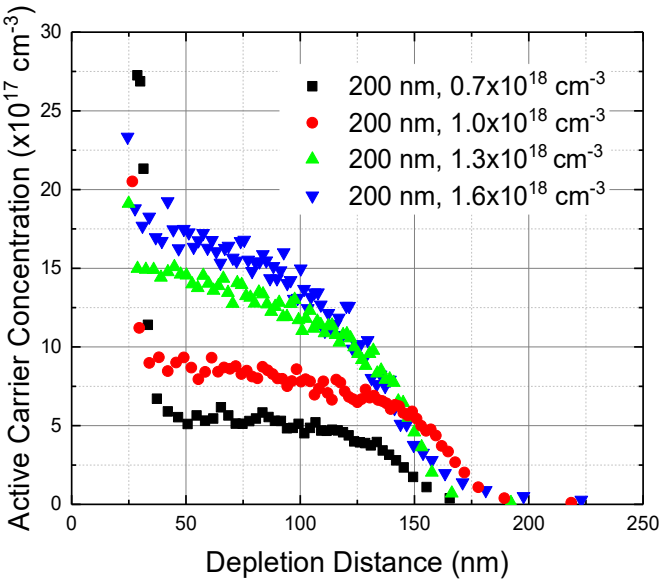


Figure 46 Depletion distance dependent carrier concentration through the channel thickness for β-Ga_2O_3 homoepitaxial layers after MOSFET fabrication extracted from capacitance vs. voltage measurement using the slope of $1/C^2$-V to extract carrier concentration and a depletion and gate oxide capacitor in series to extract distance from the gate oxide-gallium oxide interface. The result shows difficulty in characterizing the gate oxide-gallium oxide interface (near 0 nm) and the epi-substrate interface (near 200 nm) using C-V profiling after fabrication.

The measured value of the sheet resistance from circular TLM, R_{SH} was also used with N_d calculated above to determine the effective mobility from the N_d-μ product. This mobility is included in Table 7 as $\boldsymbol{\mu_{eff}}$ and it agrees with the expected value from sister epitaxial growth. Finally, N_d, V_{FB}, and μ_{eff} are used in Equation 18 in the TINA simulator (Figure 41) to estimate the drain current under isothermal, ideal-interface-state conditions. Additional parameters used in the model are shown in Table 8. The modeled value of I_{DSS} using Equation 18 is included in Table 7 as $\boldsymbol{IDSS_{mod}}$.

Table 8 Parameter values used for analytical model of β-Ga_2O_3 MOSFETs.

Parameter	Value
Relative dielectric constant of HfO_2, ε_{ox}	22.3 measured on MIM caps
Relative dielectric constant of Ga_2O_3, ε_s	10.0 ref [152]

Effective density of states in conduction band, N_C	3.72x10^{18} cm^{-3} ref [132]
Metal work function for Ti, Φ_M	4.33 eV ref
Electron affinity of Ga_2O_3, χ_s	4.0 eV ref [132]

While the value for $\boldsymbol{IDSS_{mod}}$ and $\boldsymbol{V_{off}}$ in Table 7 are close to theoretical values under pulsed conditions for the different doping concentrations studied, the drain current is still reduced by surface potential dependent negative charges at the gate oxide-gallium oxide interface [99] that effectively reduce the gate voltage applied by the value shown in Equation 23 [1].

Equation 23 Change in the applied gate voltage from a change in the interface charge, Q_{it}, resulting from the presence of filled versus empty negative surface traps. C_G is the gate voltage dependent capacitance. Dependence on the surface potential, Ψ_s, has been converted to dependence on the gate voltage, V_G.

$$\Delta V_G = \frac{\Delta Q_{it}(V_G)}{C_G(V_G)}$$

Based on the assumption that the time constant of traps is slower than the AC signal, and that interface traps are filled and empty for reverse and forward C-V sweeps, respectively, we calculate ΔV_G from the charge difference between the two curves in Figure 45 and the measured C_G at every point. We then replace V_{GS} with V_{GS}-ΔV_G in Equation 18 to obtain the values for $\boldsymbol{IDSS_{mod\ \Delta VG}}$ and $\boldsymbol{V_{knee\ mod\ \Delta VG}}$ in Table 7. We also include the accumulation mode by solving Equation 18 with V_{GS}=V_{FB} and adding an accumulation current from Equation 22 with V_{GS}=V_{GS}-ΔV_G. In doing so, we note that effects of the normal field on μ_{eff} have not been evaluated, and further investigation is

required. In our case, where the normal field is very small, however, this addition to our model accurately predicts the I-V curve for V_G=+4 V. The result is shown in Figure 44 for the highest doping level device. Similar agreement was observed for all but the lowest doped sample. As the doping level was decreased, the assumption that V_{off} is not significantly affected by interface trapped charges breaks down, and Equation 19 using the ideal value of V_{FB} miscalculates N_d. In other words, as the doping concentration (or active layer thickness) is reduced the magnitude of V_{off} is not sufficient to drive out negative interface trapped charges, and ΔV_G affects not only Equation 18 but also Equation 19. N_d calculated from Equation 19 becomes dependent on V_G and transfer characteristics of the analytical model become inaccurate without additional advanced measurement techniques. With thin or lightly doped devices, the interface charge effect on ΔV_G and V_{FB} is significant. In fact, thin enhancement-mode devices have been reported [91] with V_{off} greater than +75 V exceeding the band-gap-electron-affinity sum for β-Ga_2O_3 and indicating significant thickness of the gate oxide-gallium oxide interface trap layer. In these difficult cases, Hall measurements can be used to determine μ_{eff}, but techniques must be developed to overcome anomalies at the gate oxide-gallium oxide interface to accurately determine N_d and V_{FB}. This will be further discussed in the sections that follow.

Channel Thickness Variation of β-Ga_2O_3 MOSFETs

In this section we further evaluate the model in Chapter 4 versus variations in channel thickness for β-Ga_2O_3 MOSFETs. As described in the section above, as the channel becomes thinner, the effect of surface traps will become more dominant leading

to unreliable results for the active carrier concentration and transconductance of the device. In addition to this, it is impossible to increase and decrease the channel thickness arbitrarily while maintaining the same gate length because of Coulomb screening from the volume conducting channel, as will be further described in the next chapter. Finally, it is more difficult to control the active carrier concentration (doping) than the channel thickness, thus experiments based on a device with the same channel thickness and variable doping as presented above produce more reliable results than experiments based on the same active carrier concentration and different channel thicknesses. Still, the channel thickness dominates the off-state voltage as seen in Equation 19, and it is thus desirable to tailor it to an optimum value as we will show in Chapter 6. Here, we verify the results of the model in Chapter 4 for channel thickness as was done above for doping.

Table 9 Sample summary of β-Ga_2O_3 MOSFETs with different channel thickness and the same target doping concentration.

N_d As Grown[a]	d_{ch}[f]	V_{knee}[c]	IDSS[d]	V_{off}[c]	N_d Post Process [a]	μ_{eff} [b]	$IDSS_{mod}$[d]	$IDSS_{mod\ \Delta V_G}$[d]	$V_{knee\ mod\ \Delta V_G}$ [c]	R_C[e]
$1.60x10^{18}$	50	12.0	0.7	-1.5	$5.80x10^{17}$	–	4.9	0	–	–
$1.60x10^{18}$	100	10.9	13	-4.7	$4.66x10^{17}$	41.9	13.3	3.4	3.8	62.5
$1.60x10^{18}$	150	26.9	72.3	-12.6	$5.65x10^{17}$	65.2	98.6	75.1	23.8	25.0
$1.60x10^{18}$	200	69.6	381	-30.8	$7.88x10^{17}$	51.0	404.6	381.4	71.0	10.7

[a] cm^{-3}, [b] $cm^2/V \cdot s$, [c] V, [d] mA/mm, [e]Ohm-mm, [f]nm

A similar fabrication process and structure as depicted in Figure 42 was used for MOSFETs on MBE grown epitaxy with channel thicknesses from 50 to 200 nm recorded as d_{ch} in Table 9. The Sn-doping level, N_d ***As Grown,*** was targeted at $1.6x10^{18}$ cm^{-3} and verified by electrochemical C-V before fabrication. As seen above, this value can vary considerably after fabrication, so the same method presented above was used to

determine the active carrier concentration after fabrication, ***N_d Post Process*** in Table 9**,** from an iterative solution to Equation 19 using the measured off-state voltage, ***V_{off}*** in Table 9. ***V_{off}*** is extracted from C-V measurements as shown for the 150 nm thick device in Figure 47.

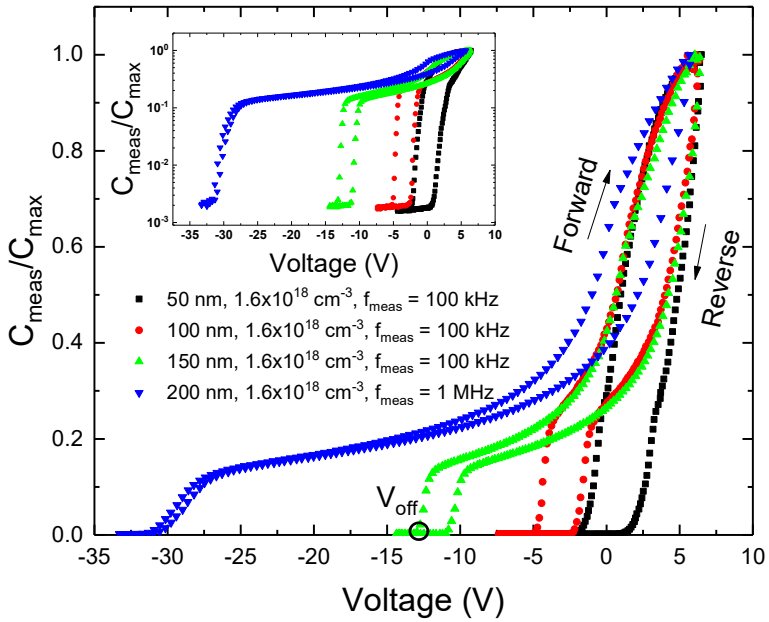


Figure 47 Normalized capacitance vs. voltage, C-V, for MOS structures on MBE grown β-Ga_2O_3 homoepitaxial layers with varying channel thickness and 1.6x10^{18} cm^{-3} target doping concentration. The inset shows log scale plots of the same. The inflection point used to determine V_{off} is shown for one device. All samples had HfO_2 gate dielectric.

TLM measurements were used to extract the contact resistance, recorded as ***R_C*** in Table 9, and the sheet resistance which was used with ***N_d Post Process*** to calculate the mobility recorded in Table 9 as ***μ_{eff}***. We again extracted the knee voltage, ***V_{knee}***, and the saturated drain current at V_G=0 V, ***IDSS***, from the inflection point in the pulsed-IV family of curves for each channel thickness as recorded in Table 9 and shown for the 100 nm

sample in Figure 48. A transfer curve of this sample is also shown in Figure 49 demonstrating excellent transistor performance with on/off ratio >10^8.

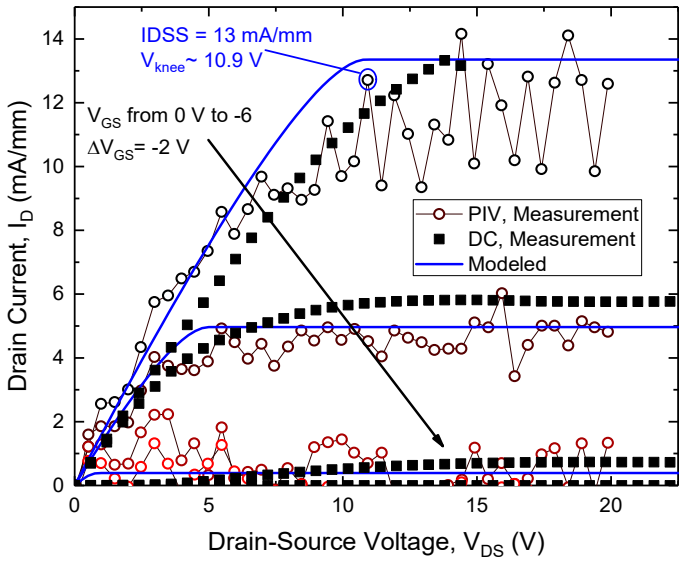


Figure 48 Pulsed family of drain current curves (symbols) for a β-Ga_2O_3 MOSFET with a 100 nm active channel thickness. Gate dispersion was avoided by measuring from the on to off states. Large fluctuations in drain current are a result of the fidelity of the pulsed IV measurement system. The device operates close to theoretical values as shown by an electrostatic analytical model which neglects the interface charge. In this case, negative charges are never removed and the interface charge is already captured in the low calculated doping concentration for the model. A power limited (80 mW limit) static measurement is also shown with similar results.

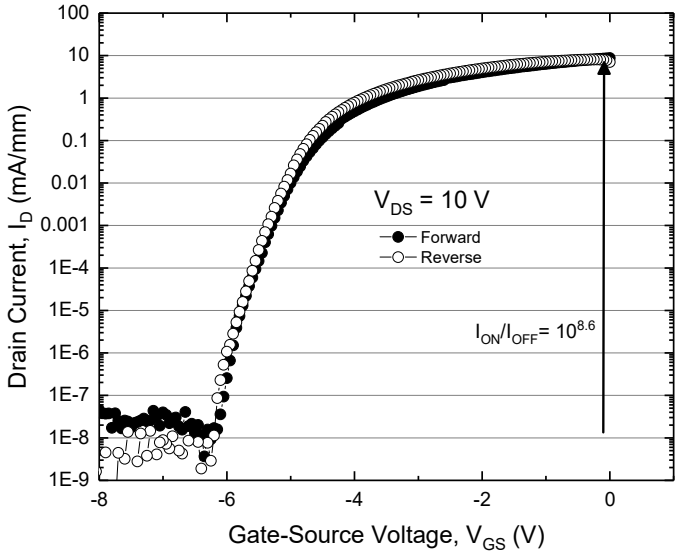


Figure 49 DC log transfer curve for a β-Ga_2O_3 MOSFET with a 100 nm thick active channel layer showing good transistor operation.

The model in Chapter 4 is used to calculate ***IDSS$_{mod}$*** in Table 9 which is the theoretical value of the drain current at V_G=0V without surface charge effects included. A modeled family of curves is also shown in Figure 48 for the 100 nm device. We also use Equation 23 to calculate the gate voltage offset induced by negative surface traps at the HfO_2-Ga_2O_3 interface. (Since the 50 and 100 nm samples exhibit very weak depletion characteristics in the C-V measurement, the value of ΔV_G can be approximated from the difference in the forward and reverse off-state voltage. However, as seen in Figure 48 trap states are not changed in these devices and the value of N_d calculated from V_{off} may already compensate for the negative interface charges.) This leads to ***IDSS$_{mod\ \Delta VG}$*** and ***V$_{knee\ mod\ \Delta VG}$*** in Table 9 which are the drain current at V_G=0V and knee voltage, respectively, with both corrected for interface charge.

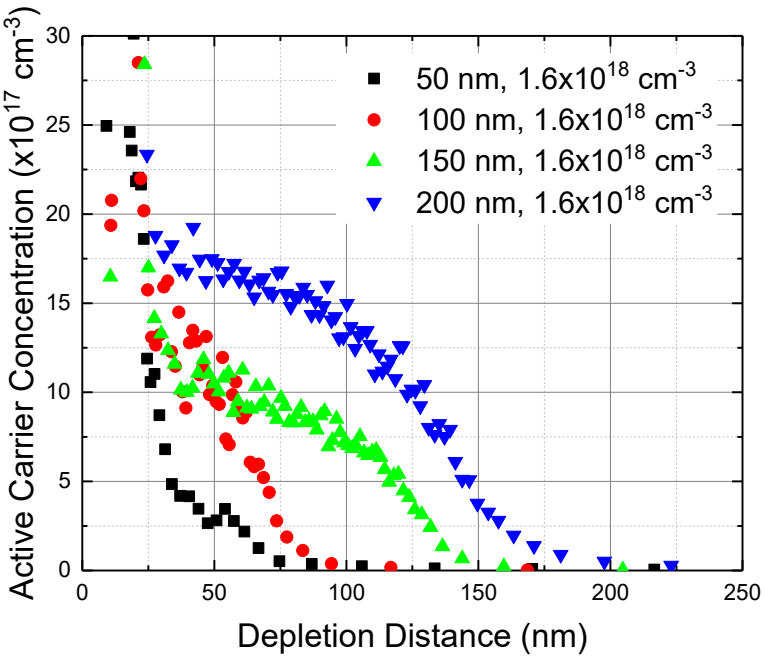


Figure 50 Depletion distance dependent carrier concentration through the channel thickness for β-Ga_2O_3 homoepitaxial layers after MOSFET fabrication extracted from capacitance vs. voltage measurement using the slope of $1/C^2$-V to extract carrier concentration and a depletion and gate oxide capacitor in series to extract distance from the gate oxide-gallium oxide interface. The result shows difficulty in characterizing the gate oxide-gallium oxide interface (near 0 nm) and the epi-substrate interface using C-V profiling after fabrication.

A quick comparison of Table 8 with Table 9 highlights some of the difficulty in applying the simple model in Chapter 4 to β-Ga_2O_3 MOSFETs. As mentioned, and shown in Figure 46 and Figure 50, it is difficult to accurately determine the average active carrier concentration, N_d, through the channel after fabrication because the value varies at the gate-oxide-gallium oxide and gallium oxide-substrate interface. In our devices, this problem is evident in the 50 nm sample which is almost an enhancement mode device in spite of still having a large amount of volume carriers in the channel. In fact, TLM structures could not be accurately measured on the 50 nm thick sample, and therefore, values of R_C=25.0 Ω-mm and μ_{eff}=62.5 $cm^2/(V \cdot s)$ were used in the model from the sample with the most similar doping level (150 nm thick sample in row 3). It is also seen

that variation still exists in the crystal quality and uniformity of epitaxial growth as the mobility of the 150 nm sample is the highest, in spite of a higher doping than the 100 nm sample. Finally, we note that some large variations in R_C can exist using different extraction methods or TLM sites, and even small variations in R_C can lead to large variations in both I_{DSS} and V_{knee}. Immediate improvements can be made through more accurate measurements of μ_{eff} using the Hall Effect and N_d using C-V. This and additional, improvements to the model and supporting measurements will be discussed in Chapter 6. For now, model prediction of the trends in off-state voltage, drain current, and knee voltage with varying channel doping and thickness have shown that the model is mostly limited by material system immaturity when predicting depletion mode operation, and the model is thus sufficient to quickly predict performance of β-Ga_2O_3 MOSFET designs as device design parameters are changed. Next, we quickly evaluate the ability of the model to predict changes in the gate oxide, and in the final section of this chapter, we address some of the concerns with modeling thermal effects.

Gate Oxide Variation of β-Ga_2O_3 MOSFETs

Besides thickness of the active channel and doping concentration of the channel which are designed through epitaxy growth, the type and thickness of the gate oxide can be chosen during the fabrication of β-Ga_2O_3 MOSFETs. Characterization of the gate-oxide-β-Ga_2O_3 interface for different MOS structures is, however, difficult. Sample sizes for MOSFET devices are small and material system immaturity often leads to non-uniformity in epitaxial growth which makes routine experiments with different gate oxides on the same MOSFET channel extremely difficult compared to more mature

technologies. Additionally, as shown above through C-V measurements, significant anomalies occur at the gate oxide- gallium oxide interface leading to changes in the flat-band voltage, V_{FB}, and carrier concentration of the channel layer, N_d. This results in difficulty in obtaining strong accumulation characteristics which allow more accurate extraction of V_{FB} and N_d. In fact, in spite of reports of numerous e-mode devices [91], [130], [153], no clear demonstration of accumulation mode has been conducted for β-Ga_2O_3 MOSFETs. Further, biasing the devices or MOS structures into accumulation mode can require large forward biases which lead to degradation of the gate oxide from leakage currents caused by potentially small conduction band offsets between the wide bandgap Ga_2O_3 and the wide bandgap gate oxide.

With all of these difficulties taken into account, the analytical model in Chapter 4 allows us to at least compare the effects of different gate oxides on the drain current, Equation 18, and the off-state voltage, Equation 19, versus simple electrostatic theory while ignoring the effects on MOS structure itself.

We fabricated β-Ga_2O_3 MOSFETs using the process depicted in Figure 42 except this time a Mg-doped semi-insulating substrate with (100) orientation was used for two different samples with either a 20 nm thick thermal ALD Al_2O_3 or a 20 nm thick plasma enhanced ALD HfO_2. Both samples had a 200 nm channel thickness. A post process average carrier concentration of $3.40\text{x}10^{17}$ and $3.42\text{x}10^{17}$ cm^{-3} and an effective mobility of 12.4 and 15.5 $cm^2/(V\cdot s)$ were obtained from room temperature Hall Effect measurements on van der Pauw (VDP) structures for the sample with Al_2O_3 and HfO_2, respectively. From C-V measurements as shown in Figure 51 and the extracted doping

concentration in Figure 52, we can see that the carrier profiles are nearly identical for the two samples which makes them good for comparison of the MOSFET electrical parameters with different gate oxides. From Figure 52, it is also clear that Hall Effect measurements underestimate the average volume doping concentration because the thickness is assumed to be 200 nm, whereas, it is actually closer to 180 nm because of depletion at the channel-substrate interface. In Figure 53, we present the measured and modeled values of V_{off} and I_{DSS} for both samples. The relative difference in the electrical parameters is reasonable if the C-V doping profile is assumed to be more accurate; however, the sample with Al_2O_3 has a higher than expected V_{off} and I_{DSS} based on our model. Further investigation is required for this discrepancy; however, it otherwise appears that the model can accurately predict changes in MOSFET electrical characteristics for different gate oxides.

Although, in this case, we were limited to a single comparison of gate oxides (the only samples with different gate oxides combined with similar doping profiles) additional verification of the model fit for each oxide can be found in the other sections of this chapter, where we have assumed in each model the corresponding value of Al_2O_3 or HfO_2 measured from metal-insulator-metal (MIM) capacitors. From Figure 51 and Figure 53, we can also see that, as expected, the HfO_2 with its higher relative dielectric constant provides better gate control of the channel charge.

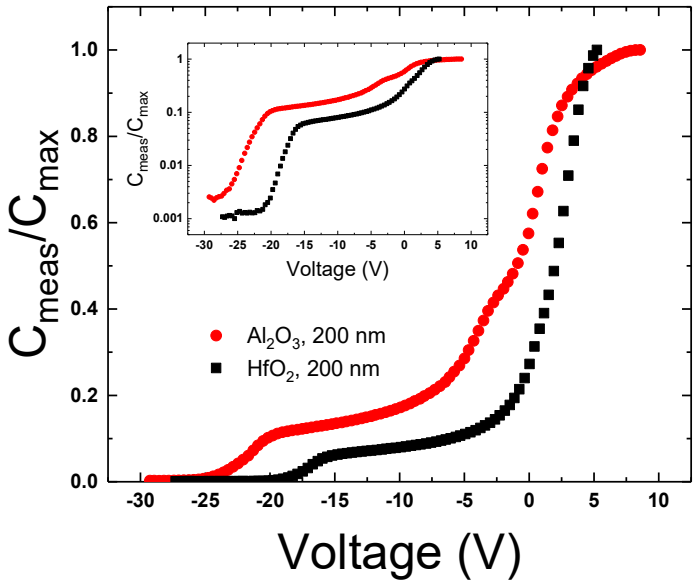


Figure 51 Normalized capacitance vs. voltage, C-V, for MOS structures on MOVPE grown β-Ga_2O_3 homoepitaxial layers with two different oxide layers and nearly identical doping profiles. The inset shows log scale plots of the same.

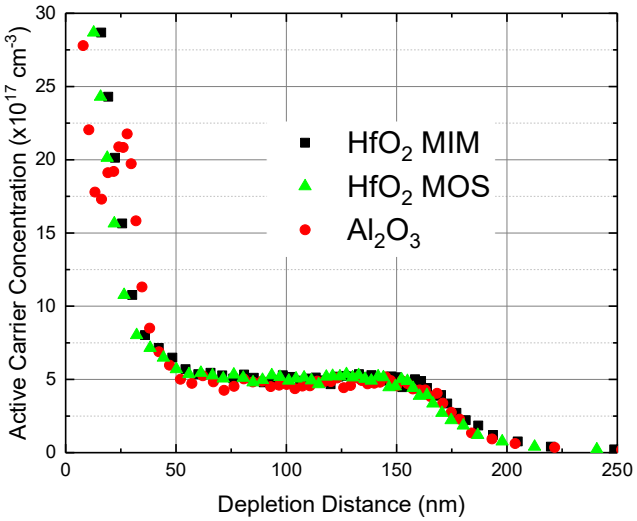


Figure 52 Depletion distance dependent carrier concentration through the channel thickness for β-Ga_2O_3 homoepitaxial layers after MOSFET fabrication extracted from capacitance vs. voltage measurement using the slope of $1/C^2$-V to extract carrier concentration and a depletion and gate oxide capacitor in series to extract distance from the gate oxide-gallium oxide interface. The profiles are shown for MOS capacitors with two different dielectric layers. The HfO_2 profiles are calculated using the relative dielectric constant from metal-insulator-metal (MIM) capacitors, 22.3, and from the maximum capacitance of the measured metal-oxide

semiconductor (MOS) capacitor, 16.6. The Al_2O_3 MIM and MOS relative dielectric constants were both measured to be 8.3.

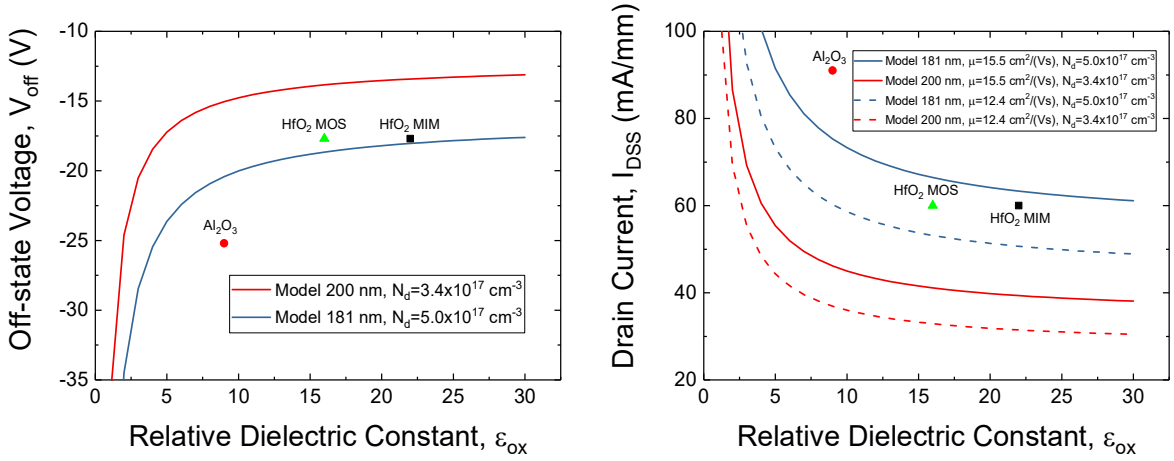


Figure 53 Off-state voltage (left) and drain current @ V_G=0 V, I_{DSS}, (right) versus relative dielectric constant of the gate oxide in β-Ga_2O_3 MOSFETs. Model results for two different doping concentrations measured by Hall Effect (red) and by C-V doping profile (blue) are presented with measured data from samples with Al_2O_3 or HfO_2 gate dielectric. For the C-V doping profile, the model results are reasonably matched to the measured electrical performance although the Al_2O_3 sample indicates a higher doping concentration or channel thickness. The modeled I_{DSS} does not include the voltage drop across the source contact or access region.

β-Ga_2O_3 MOSFET Thermal Variations

Drain current measurements in the previous sections have been based on pulsed IV measurements with a static gate voltage specifically to avoid self-heating effects [154] that may be present at higher power because of the poor thermal conductivity of β-Ga_2O_3. The model in Chapter 4 does not include the temperature dependence on the parameters used with the exception of the thermal voltage in the calculation of the flat-band voltage, and so, it may be insufficient for modeling self-heating effects or electrical performance at high temperature. This will be discussed in the next chapter. To conclude this chapter

we instead quantify the self-heating by comparing a device to our model at different baseplate temperatures.

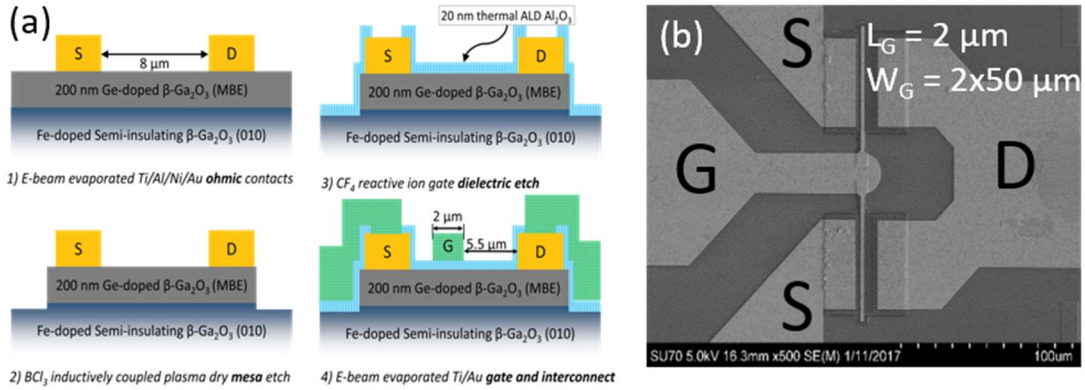


Figure 54 (a) Ge-doped β-Ga_2O_3 MOSFET process flow and (b) SEM of 2x50 µm device reported. Device dimensions are included in both.

Our MOSFET process flow is shown schematically in Figure 54. A first-ever, Ge-doped homoepitaxial β-Ga_2O_3 channel was grown by MBE to a target thickness of 200 nm using a germanium cell temperature of 580 ºC on commercially available (010) Fe-doped semi-insulating substrates [155]. After visual inspection and stepper lithography, source and drain ohmic contacts were formed by electron beam evaporation of a Ti/Al/Ni/Au metal stack. Mesa isolation of active regions was performed using a BCl_3 inductively coupled plasma (ICP) dry etch followed by a 470 ºC 60-second ohmic anneal in N_2 ambient. A 20 nm thick Al_2O_3 gate dielectric was deposited by thermal atomic layer deposition (ALD) at 250 ºC with no surface pre-treatment after the ohmic anneal. A CF_4 reactive ion etch (RIE) was used to clear the ohmic pad regions of the gate dielectric; then, interconnects and 2-µm long gates were patterned and deposited simultaneously

using evaporated 20/480 nm Ti/Au. A Keysight B1505a power device analyzer equipped with source measurement units and a multi-frequency capacitance measurement unit was used for electrical testing on MOSFETs with dimensions presented in Figure 54 and for C-V testing on lateral MOSCAP structures with various diameters. Room temperature and temperature dependent Hall measurements were conducted on van der Pauw (VDP) structures following device fabrication and test. An AMCAD Bilt system was used for pulsed-IV. Temperature dependent DC and pulsed-IV measurements were conducted on a Cascade Microtech Summit 12000 series probe station with a thermal chuck housed inside a microchamber enclosure with a slight nitrogen overpressure. The device was allowed to sit for >30 min on the base plate at the desired temperature before each successive test.

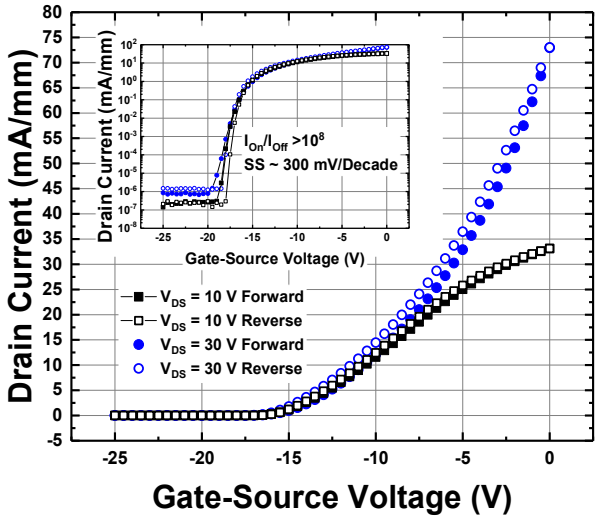


Figure 55 Linear and log (inset) DC transfer curve (I_{DS}-V_{GS}) for a Ge-doped β-Ga_2O_3 MOSFET at V_{DS} = 10 (black squares) and 30 (blue circles) V.

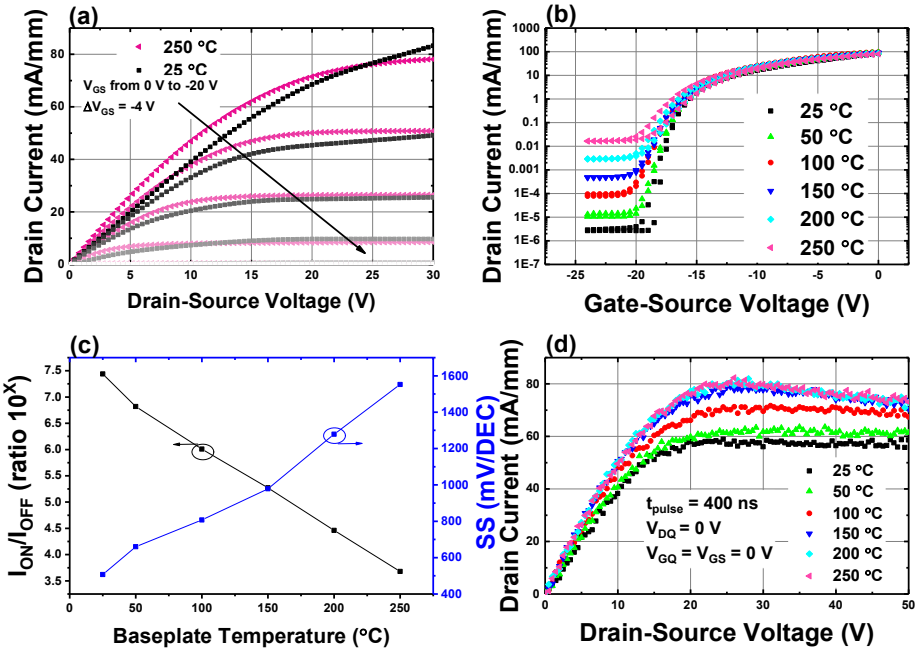


Figure 56 (a) DC family of drain current curves (I_{DS}-V_{DS}) for a Ge-doped β-Ga_2O_3 MOSFET at 25 ºC and 250 ºC. (b) Log tranfer curves (I_{DS}-V_{GS}) at various temperatures for the same device in a. (c) Subthreshold parameters (I_{ON}/I_{OFF} and subthreshold swing, SS) versus temperature extracted from b. (d) V_{GS}=0 V pulsed-IV curve at various temperatures for the same device in a.

The MOSFETs, as shown in Figure 54(b), have a two finger layout with total gate width, W_G=100 µm, a gate length, L_G=2 µm, an 8 µm source-drain (S-D) spacing, and a 0.5 µm gate-source (G-S) spacing. Electrical characteristics of a representative device showing on-off current ratio, $I_{ON}/I_{OFF}>10^8$, and maximum drain current, I_{Dmax}>75mA/mm, at V_{GS}=0 V are presented in Figure 55 and Figure 56. The devices showed low gate dispersion as observed from the hysteresis between forward and reverse sweeps in Figure 55 indicating a low number of surface traps at the Al_2O_3-Ga_2O_3 interface. Figure 56(a) includes a family of curves at high temperature showing stable operation with only a slight difference in maximum current. Figure 56(b) shows transfer

characteristics over temperature and Figure 56(c) summarizes the I_{ON}/I_{OFF} and subthreshold swing (*SS*) over the same temperature range. The transistor off current increases exponentially with temperature with a corresponding increase in *SS*. In Figure 56(d), we present a 0.004% duty cycle, 400 ns drain pulse (10 ms period) pulsed-IV measurement at V_{GS}=0 V to demonstrate transistor operation in the absence of self-heating [154]. A slight increase in drain current occurs with temperature until 200 ºC with maximum pulsed current density approaching the maximum DC value shown in Figure 56(a). The observation of increasing drain current with temperature in Figure 56(a) and (c) indicates a complex dynamic relationship between carrier activation/emission from traps and mobility degradation both of which can be induced by self-heating and ambient temperature. The sheet resistance, R_{SH} was 10.58 kΩ/square and the average carrier mobility, μ_{eff}, was 111.0 $cm^2/(V \cdot s)$ as determined by post-process room temperature Hall effect measurements on VDP structures nearest this device. High mobility was generally observed across the whole 10 mm x 10 mm sample with μ_{eff}=103.4±9.8 $cm^2/(V \cdot s)$ as measured from 12 VDP sites. Figure 57 shows temperature dependent Hall Effect measurements of the carrier concentration and mobility using VDP structures. A Hall factor of one was assumed when calculating the Hall carrier density and Hall mobility. Fitting of the carrier concentration versus temperature with the charge neutrality equation for a single compensated donor yields a donor energy of 17.5 meV, a donor concentration of 6.1×10^{17} cm^{-3}, and a compensation ratio of N_a/N_d = 0.61 for the Ge dopant. An effective mass of 0.3 m_e [22], [156], [157] was used for the calculation. The donor energy determined for Ge is comparable to estimates for Sn and Si [50], [82].

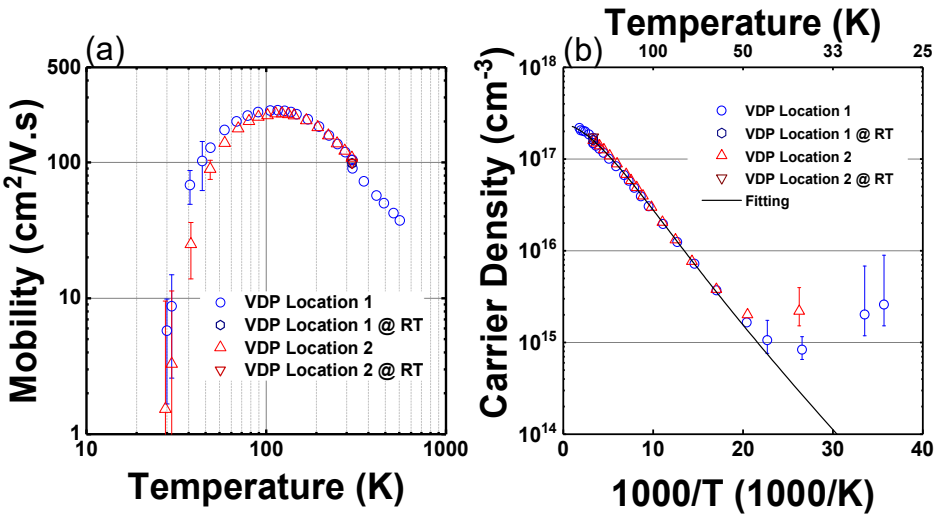


Figure 57 Temperature dependent Hall mobility (a) and Hall carrier concentration (b) from van der Pauw (VDP) structures at two locations on the same Ge-doped β-Ga_2O_3 channel layer. Fitting of the data in (b) yields a donor energy of 17.5 meV, donor concentration 6.1x10^{17} cm^{-3}, and compensation ratio of 0.61.

Measurements from lateral C-V structures (Figure 58(a)) were used to estimate the channel carrier concentration, 3.9x10^{17} cm^{-3}<N_d<4.36x10^{17} cm^{-3}, and the flat-band voltage, 2.19 V<V_{FB}<4.5 V, using the slope and intercept of the linear region of $1/C^2$-V curves, respectively, as shown in Figure 58(b). There is a slight mismatch with the carrier concentration calculated from Hall effect measurements (i.e. 2.9x10^{17} cm^{-3}) because the Hall method ignores depletion at the gate oxide and substrate interfaces and assumes a thickness of 200 nm and because the Hall factor was assumed to be one. The depletion effects can be observed in the inset of Figure 58 at both the substrate and surface interfaces. Unlike the mobility, a larger variation in carrier concentration was observed across the sample and analysis was thus limited to specific devices for temperature dependent modeling.

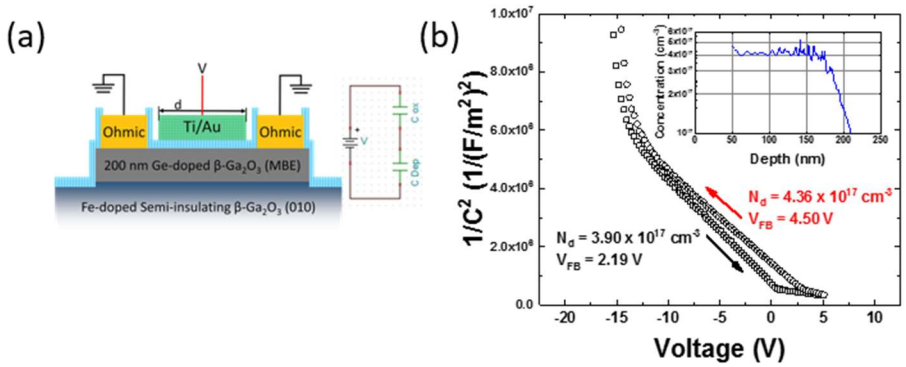


Figure 58 (a) Lateral MOSCAP structure with diameter=*d* used for C-V to measure (b) 1/C^2-V characteristics of the channel of a Ge-doped β-Ga_2O_3 MOSFET. The carrier concentration and depth profile (inset of b) were extracted from the slope for forward (black squares) and reverse (red circles).

To compare the temperature dependent measurement in Figure 56(d) to the model in Chapter 4, we updated the model with temperature dependent mobility using a polynomial fit to the data in Figure 57(a) and with temperature dependent carrier concentration using Equation 24 with values presented above and a calculated effective density of states in the conduction band (Equation 25) assuming an effective mass of 0.28 m_e. These temperature dependent functions replaced N_d and μ in Equation 18 and Equation 19 and in the VerilogA code in Appendix C: VerilogA Code For Drain Current and Appendix B: VerilogA Code for Access Resistors. Additionally, we corrected the value of the Hall carrier concentration by a factor of 2.63 to match the C-V measurement in Figure 58 at room temperature, and we reduced the modeled channel thickness to 190 nm to remove the depletion at the substrate surface. Results for saturated drain current are presented in Figure 59.

Equation 24 Charge neutrality equation used to determine the active carrier concentration, n, versus temperature, T, in the channel of a β-Ga_2O_3 MOSFET. N_A is the compensating acceptor level, N_D is the donor concentration, N_C is the effective density of states in the conduction band, k is Boltzmann's constant, and E_D is the activation energy. This equation can be fit to measured temperature dependent Hall carrier concentrations to determine, N_D, N_A, and E_D [50].

$$\frac{n(n+N_A)}{N_D-N_A-n}=\frac{N_C}{2}e^{-E_D/kT}$$

Equation 25 Effective density of states in the conduction band versus temperature, T, calculated from the electron effective mass, $m_r^* m_e$. k is Boltzmann's constant and $\hbar$ is the modified Planck's constant. The value of the relative electron effective mass, m_r, is found from the band diagram.

$$N_C=2\left(\frac{m_r m_e kT}{2\pi\hbar^2}\right)^{3/2}$$

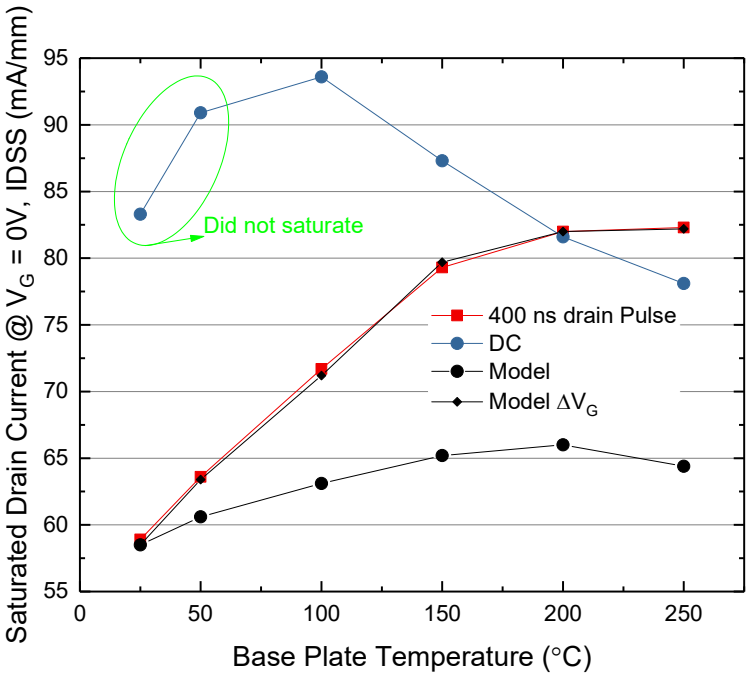


Figure 59 Saturated drain current extracted at the knee voltage versus base plate temperature for a Ge-doped Ga_2O_3 MOSFET. The results include a 400 ns drain pulse pulsed IV measurement that minimizes the effects of self-heating, a DC measurement that is largely affected by self-heating, and two modeled results using temperature dependent Hall effect measurements for the mobility and carrier concentration of the channel.

Both the model and pulsed measurements show that the current increases with temperature until the mobility degradation dominates. The larger increase in current with temperature can be explained by decreased negative trapped charge under the gate as the temperature is increased (as shown using Model ΔV_G).

While the current does increase slightly from the conflicting effects of reduced mobility and increased carrier concentration as temperature increases, the model alone is not enough to match the measured data as shown in Figure 59. We hypothesize that the increased current also results from the removal of negative charge in surface states under the gate. This can easily be modeled by reducing the flat-band voltage of the device from the measured C-V value of 4.5 V as the temperature increases. We have done this in the ***Model ΔV_G*** curve in Figure 59 to match the measured data. The change in the flat-band voltage necessary (Figure 60) is reasonable compared to the difference in forward and reverse C-V sweeps in Figure 58. The curves shown in Figure 61, however, still do not match the decreased on resistance at high temperatures (in fact it increases). We believe this is a result of decreased access resistance from removal of negative charge in the access regions at the source and drain; however, modeling this requires extensive iteration beyond the scope of the current model. For now, we have shown that electrical performance at temperature is dependent on at a minimum changes in mobility, carrier concentration, and occupation probability of negative surface states at the gate-oxide-gallium oxide interface. Thermal modeling of real devices is further complicated by device self-heating owing to the low thermal conductivity of Ga_2O_3. This will be discussed further in the next chapter.

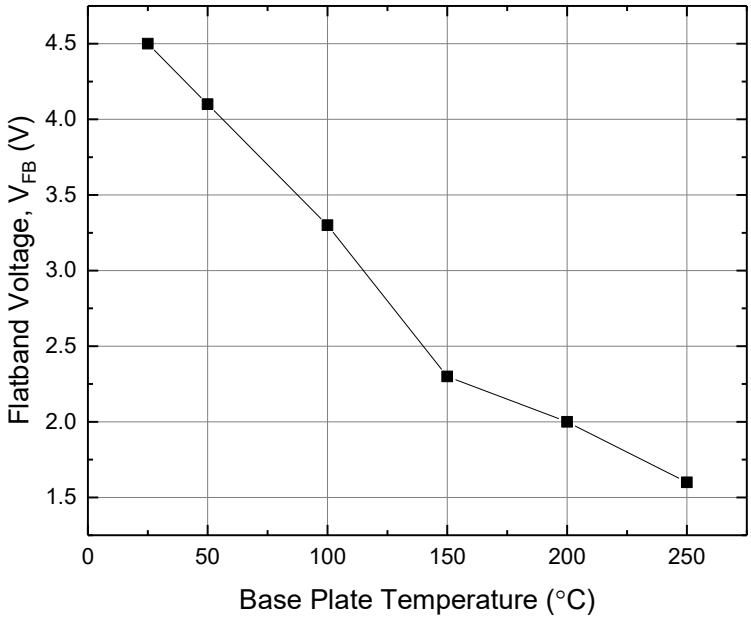


Figure 60 Flat-band voltage values at different base plate temperatures used to match measured to modeled drain current of a Ge-doped Ga_2O_3 MOSFET. The flat-band voltage is reduced at high temperatures to simulate the removal of negative surface charge as the temperature is increased.

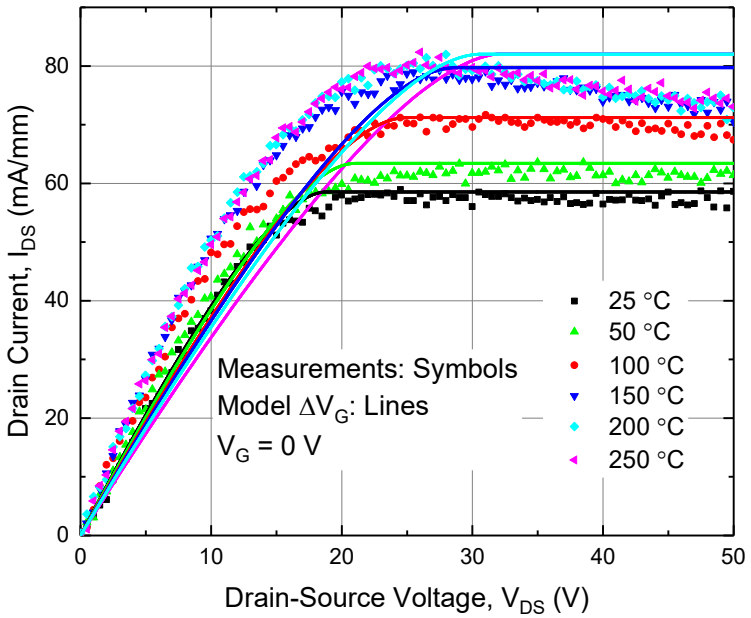


Figure 61 Drain current at V_G = 0V vs. drain voltage for the same Ge-doped Ga_2O_3 at different base plate temperatures. Measured values are from a pulsed IV measurement with a 400 ns drain pulse. Modeled values are from a model that includes changes in the flat-band voltage at higher temperature. The model does not include changes in the access region resistance, and thus, the knee voltage/on-resistance of the modeled and measured data does not agree.

6. MODEL IMPLICATIONS AND LIMITATIONS

In this chapter, we focus on the design trades evident in the simple model developed in Chapter 4 and the limitations of that model related to the material that have become and will become evident as the material system and devices are developed.

Optimal Device Performance

The calculations used in formulating Baliga's figure of merit provide a good basis for designing an optimized power switch. For lateral devices with a given gate-drain spacing, W_B, we can calculate the doping required, N_B, (and expected breakdown, V_B) from the material parameters, E_C and ε_s, to optimize the on-resistance, R_{ON}, and gate charge, Q_G, for any power switching device using the equations in Figure 5. This calculation is fairly trivial and is a very good starting point for designing a power switch or RF device. In the calculation, however, the assumption is made that the device is nearly symmetric with channel thickness equal to the channel width to allow simple calculation using E_C for the gate charge. In real devices, the channel thickness must be carefully chosen to optimize R_{ON} and Q_G while maintaining good transistor performance as measured through high on-off current ratios. In an RF device, it is also important to maximize the gain (transconductance). All of this must be done with consideration of the the breakdown voltage predicted by Baliga.

We show the on-resistance in the linear region, R_{ON}, and transconductance in saturation, G_{Msat}, from our model in Chapter 4 in Equation 26 and Equation 27, respectively. It is clear that R_{ON} depends on the channel thickness and thus the minimum value would be that of Baliga if we could successfully modulate the current at that thickness. In reality, because the device is conducting a volume current through the channel, Coulomb screening effects need to be considered as shown in Equation 28 and Figure 62. The screening at a given distance in the channel is similar to the off-state voltage from Equation 19 for a given channel thickness as shown in Figure 62; however, the Coulomb ratio is more robust because it does not rely on assumptions for V_{FB} used to calculate V_{off}. Solutions to Poisson's equation including Coulomb screening require numerical solutions. To keep our analysis simple, instead, we begin to formulate an empirical estimate in Figure 62 by comparing the measured on-off current ratios of devices with different calculated values of Coulomb screening using Equation 28. The devices are separated into devices that successfully turned off, $I_{ON}/I_{OFF} > 10^6$, and those that did not $I_{ON}/I_{OFF}<10^6$. A horizontal line can be drawn dividing devices above the line operating sufficiently as transistors and those below the line being unacceptable for transistor applications. For the best power switch, a device should be chosen by calculating the doping concentration from Baliga as described above from the available G-D spacing (a layout requirement) and then selecting the thickest layer that can be turned off at that doping level. The mobility at the given doping level should also be optimized.

Equation 26 On resistance in the linear region of a β-Ga_2O_3 MOSFET. I_{DS} is the drain current, V_{DS} is the drain-source voltage, L is the gate length, W is the gate width, q is the electron charge, N_d is the active carrier concentration, μ is the effective mobility of electrons in the channel, d is the thickness of the channel, V_{FB} is the flat-band voltage, C_{OX} is the oxide capacitance per unit area, and $\varepsilon_G=\varepsilon_S\varepsilon_0$ is the dielectric constant of Gallium Oxide.

$$RON = \left(\frac{dI_{DS}}{dV_{DS}}\right)^{-1} = \frac{L}{q\mu N_d W}\left\{\left(d + \frac{\varepsilon_G}{C_{OX}}\right) - \sqrt{\frac{\varepsilon_G^2}{C_{OX}^2} - \frac{2\varepsilon_G}{qN_d}(V_{GS} - V_{FB} - V_{DS})}\right\}^{-1}$$

Equation 27 Transconductance in the saturation region of a β-Ga_2O_3 MOSFET. I_{DS} is the drain current, V_{GS} is the gate-source voltage, L is the gate length, W is the gate width, q is the electron charge, N_d is the active carrier concentration, μ is the effective mobility of electrons in the channel, d is the thickness of the channel, V_{FB} is the flat-band voltage, C_{OX} is the oxide capacitance per unit area, and $\varepsilon_G=\varepsilon_S\varepsilon_0$ is the dielectric constant of Gallium Oxide. The device is assumped to saturate at the pinch-off point $V_{DS} = V_{GS}-V_{OFF}$ where V_{OFF} is the off-state voltage given in Equation 19.

$$G_{Msat} = \frac{dI_{DS}}{dV_{GS}}|_{V_{DS}=V_{GS}-V_{OFF}} = \frac{\mu W\sqrt{2qN_d\varepsilon_G}}{L}\left\{\left(A^2 + dqN_d\left(\frac{d}{2\varepsilon_G} + \frac{1}{C_{OX}}\right)\right)^{1/2} - (A^2 - V_G + V_{FB})^{1/2}\right\}$$

$$A = \frac{\sqrt{2\epsilon_s qN_d}}{2C_{OX}}$$

Equation 28 Potential ratio at a channel distance d versus the surface potential. λ_D is the Debye length, N_d is the active carrier concentration in the channel, q is the electron charge, k is boltzmann's constant, T is the temperature, and $\varepsilon_G=\varepsilon_S\varepsilon_0$ is the dielectric constant of Gallium Oxide.

$$\frac{\psi(d)}{\psi(0)} = e^{-d/\lambda_D} = \exp\left(-d\sqrt{\frac{N_d q^2}{\varepsilon_G kT}}\right)$$

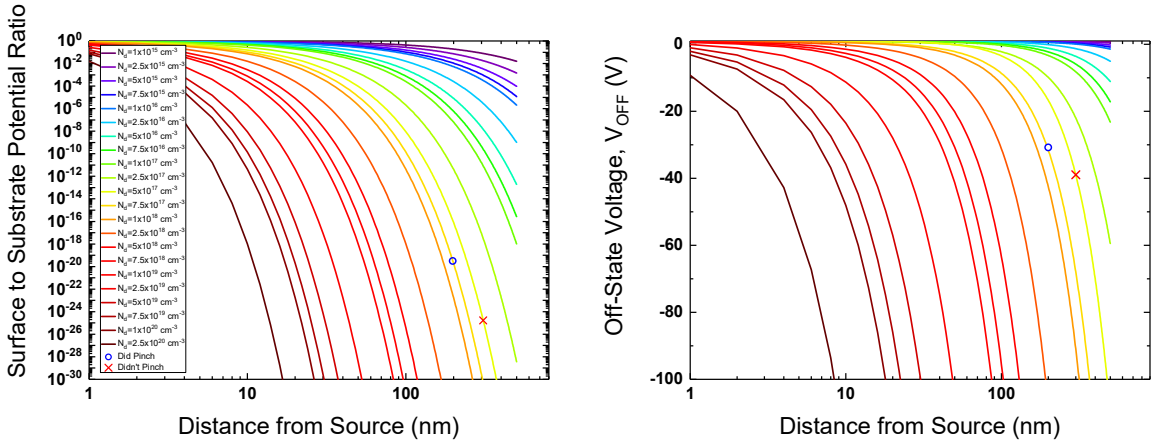


Figure 62 Coulomb screening effects through the channel of a β-Ga_2O_3 MOSFET. Right: potential ratio at a distance in the channel from the surface for a given doping level at room temperature. Left: off-state voltage required to turn off a channel at a given distance from the voltage source for a given doping level. The legend is the same for both right and left, with each line showing a different doping level. The symbols represent two measured devices with the lowest potential ratio that did turn off (blue circle) and the highest potential ratio that did not turn off (red X). A horizontal line can be drawn between these points with devices above the line having good transistor characteristics and below the line not functioning as a transistor.

The saturated transconductance depends on both the channel thickness and carrier concentration as seen in Equation 27. To optimize the power-frequency product for a given technology node (gate length), the highest N_d-μ product achievable should be chosen first and followed by selection of the thickest channel allowable for that doping concentration as above. N_d is chosen first because it can be varied over orders of magnitude whereas the channel thickness cannot. At room temperature, for all reasonable doping levels (between $1x10^{15}$ and $1x10^{21}$ cm^{-3}), the sheet resistance with respect to N_d shown in Figure 63 continues to decrease for higher N_d in spite of reduced mobility indicating that the channel should be maximally doped to achieve the highest G_{Msat}. Based on Figure 62 then, the channel must be dramatically thinned to allow good transistor turn off at the highest doping level achievable for the best RF device. In reality, limitations exist because of differences in the transport characteristics at the surface (gate

oxide-gallium oxide interface) in the MOSFET, and because of growth control limitations on the doping level-thickness combinations for very thin layers. The final step in the RF design process is to choose the minimum G-D spacing for maximum breakdown with minimum R_{ON} using Baliga's calculations for the high doping level already chosen. Again, fabrication limitations will exist in optimization of the G-D spacing as the doping level becomes larger.

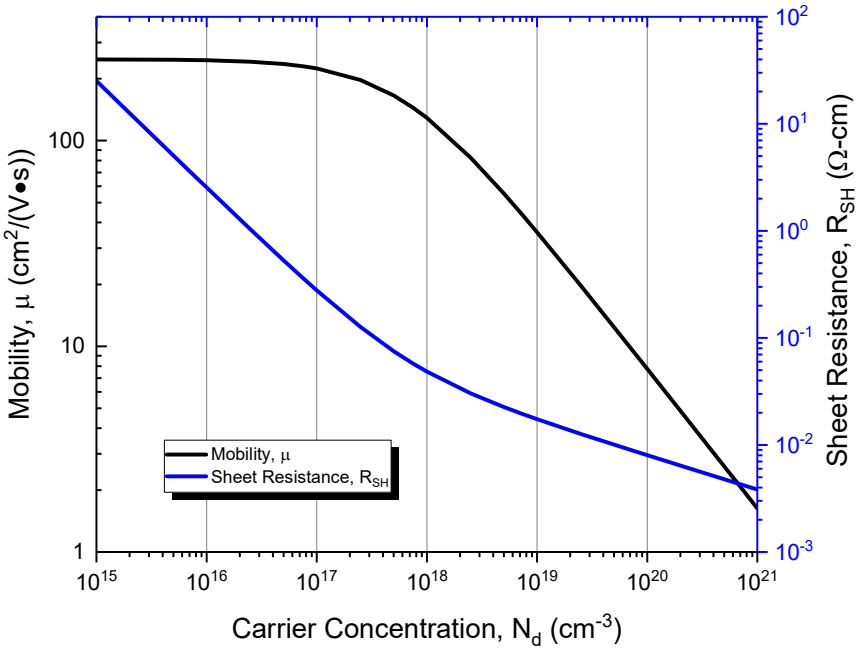


Figure 63 Mobility and sheet resistance versus carrier concentration as calculated using the empirical formula based on polar optical phonon scattering and ionized impurity scattering found in [49].

For power switching and RF devices it is also imperative to reduce any parasitic resistance in the device including the contact resistance and access region resistances. If the G-D spacing is optimized as described above for the depletion width, the parasitic gate-drain access resistance is already minimized. Ideally, the source-gate access

resistance should be reduced to zero using a self-aligned source whereby the gate is immediately at the edge of the source. This leaves the contact resistance which must be minimized at the source and drain ohmic contact. Since electron transport in ohmic contacts is dominated by field emission causing transmission through a thin energy barrier, it is advantageous to use a degenerately doped ohmic contact region and a metal with a low work function difference to gallium oxide such as titanium [1]. We can do this by selective ion implantation of the ohmic contact regions [75], [80], [158]; however, this may lead to adverse consequences such as iron diffusion from the semi-insulating substrate into the channel [62] or increased process complexities from the high temperature required.

To reduce contact resistance in our lab, we used Si-doped MOVPE grown channel layers on commercially available (010) Fe-doped semi-insulating substrates [76] with or without a 20 nm MOVPE grown ohmic cap layer degenerately doped with Si to a target concentration of ~8.0 x 10^{19} cm^{-3}. All device channels were 200 nm with Si chemical concentration targeting ~1.0 x 10^{18} cm^{-3}. Using these samples we developed a gate recess process that included the previously described mesa and ohmic steps (Figure 42) followed by removal of the ohmic cap layer between source and drain ohmic contacts by BCl_3 plasma etching, plasma enhanced chemical vapor deposition (PECVD) of 200 nm of SiO_2 as a protect mask, a CF_4 reactive ion etch (RIE) of the SiO_2 to pattern the gate recess dimension, and another BCl_3 plasma etch to recess the gate dimension to an adequate depth in the Ga_2O_3 to achieve target off-state voltage values based on our model from Chapter 4. These steps were followed by ALD gate dielectric, patterning, and

gate/interconnect evaporation as described previously (Figure 42). The entire gate recess process is shown in Figure 64(a). To verify reduction of the ohmic contact resistance, van der Pauw measurements were taken on a sample without an ohmic cap layer after mesa isolation and ohmic contact formation showing average mobility of 107 $cm^2/(V \cdot s)$ and active carrier concentration, $N_d \sim 1.1x10^{18}$ cm^{-3}. The resulting sheet resistance was R_{sh} = 2.6 kΩ/sq, and R_C without our ohmic cap was approximately ~23 Ω·mm using TLM measurements as shown in Figure 64(b). After employing the same mesa and ohmic process on a sample with an ohmic cap layer, the R_C and R_{sh} measured using TLM drastically improved to < 0.7 Ω·mm and ~1.1 kΩ/sq, respectively, as shown in Figure 64(c).

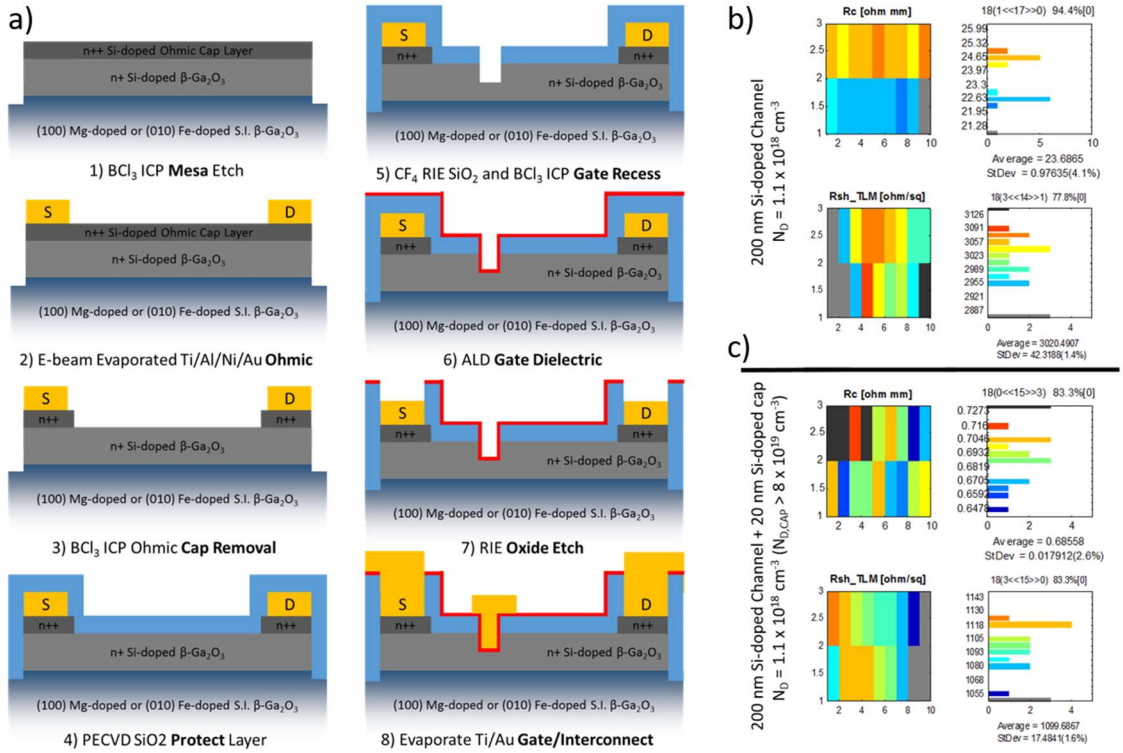


Figure 64 a) Gate recess process developed and used for reducing the contact resistance of β-Ga_2O_3 devices. The ohmic cap layer is used to reduce the contact resistance and the gate recess thins the channel to provide desired threshold characteristics. b) and c) Chip level comparison of contact resistance, *Rc* and sheet resistance, *Rsh_TLM* measured using the transfer length method for β-Ga_2O_3 samples with (b) and without (c) a highly doped ohmic cap layer. The uniformity of the ohmic contact is also shown for the 10 mm x 10 mm sample.

Achieving Enhancement Mode β-Ga_2O_3 MOSFETs

To this point, we have largely ignored the fact that as a power device it is desirable for β-Ga_2O_3 MOSFETs to operate in the enhancement (normally off) rather than depletion (normally on) mode. Enhancement mode, or e-mode, is desirable because it avoids dangerous currents and large power losses if the device or a controlling power supply fails. In the last section, we noted that maximizing N_d and channel thickness is the best way to achieve the best RF and power switch results. Unfortunately, these

parameters also play a large role in increasing the magnitude of the negative voltage required to turn the depletion mode devices off (see Equation 19). Thus, the optimum β-Ga_2O_3 MOSFET for enhancement mode must be designed much differently.

Since a suitable acceptor dopant has not been found to create p-type gallium oxide, we are limited to creating e-mode devices by exploiting the small positive flat-band voltage in the off-state voltage equation to raise the off-state voltage to a value >0 V. Equation 17 describes this flat-band voltage as the difference between the metal and semiconductor work function. Additionally, as seen in Chapter 5 negative surface states exist near the gate oxide-gallium oxide interface that further decrease the gate voltage applied-essentially increasing the flat-band voltage; although, these surface states negatively affect the maximum current and value of R_{ON} which are both undesirable. Thus, to obtain an e-mode device, we should first maximize the flat-band voltage by increasing the metal work function using metals like Pt and Ni that have higher work functions than Ti which was previously used. While a change in metal provides a very small increase in the flat-band voltage, this is currently the only way to move toward an e-mode device without adversely affecting the device performance until a p-type dopant can be found.

Maximization of the flat-band voltage using metal with a high work function increases the depletion of the channel carriers without any voltage applied. Realizing this, it is desirable to maximize the number of depleted carriers for a given surface area on the chip at 0 V to create the maximum on current per unit area for the e-mode device; however, in a lateral structure we can only deplete the carriers at the channel surface

which limits the number of depleted carriers per unit surface area to $N_d x_d$ where N_d is the active carrier density, and x_d is the amount of depletion caused by the gate metal interface. If we use a three dimensional (3D) device such as a wrap-gate fin structure, however, we can increase the depleted carriers to $>2hN_d x_d/p$ where h is the height of the fin and p is the pitch distance from the center of one fin to the center of the next fin and each fin has a thickness of $2x_d$. As long as $p<2h$ the depleted carriers per unit area are increased and the current density per unit area for the e-mode 3D device should also be increased. This advantage is not limited to e-mode devices because the threshold voltage for a given current per unit area can be decreased using the same method in the depletion-mode.

In our lab, we developed a process for an e-mode wrap gate finFET as shown in Figure 65(a). As predicted, the higher work function metal used (N_i=5.15 eV) and the channel doping (N_d = 2.7x10^{17} cm^{-3}) and triangular shape of the fin (W_{fin} = 300 nm, H_{fin} = 200 nm) allowed the fin to be completely depleted at V_G = 0 V. In fact, our device with a source-drain spacing of 21 μm achieved the highest breakdown voltage of 612 V with V_G = 0 V to date for an e-mode device. The current, however, was not maximized because in our initial process we developed the fin across the entire source-drain spacing leading to a nearly depleted source access region and extremely high parasitic source resistance (Figure 65(b)). Additionally, surface states at the gate-oxide interface are not well understood and were not controlled for the etched fin surfaces causing the gate voltage applied to be reduced considerably by negative surface traps. Further investigation into 3D structures for enhancement and depletion mode devices is underway, and the

implications on our development of this lateral fin structure for vertical devices will be discussed in Chapter 7. For now, we note that, as expected, e-mode devices with high breakdown voltages can be achieved by taking advantage of the positive flat-band voltage, and it is possible to achieve high on-off current ratios (>10^6) using 3D device technologies. Additionally, a p-type dopant even without high hole conductivity could be advantageous for moving future devices into the enhancement mode by depleting larger volumes of n-type carriers at a gate voltage of zero.

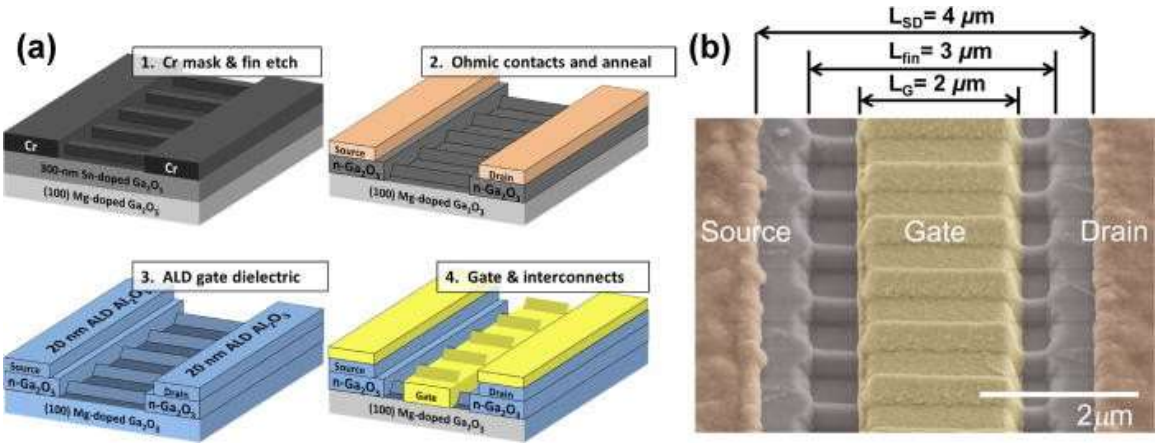


Figure 65 (a) Fabrication process for Ga_2O_3 finFETs and (b) the tilted false-colored SEM image of a L_{SD} = 4 μm finFET depicting the geometry of Ga_2O_3 fin channels and contacts. From [130]**. Used under a Creative Commons open access license.**

β-Ga_2O_3 MOSFETs Scaling

In the first section of this chapter we discussed some of the tradeoffs between doping, thickness, and mobility for β-Ga_2O_3 MOSFETs. Particularly, as shown in Figure 62 there is a tradeoff between R_{ON} and G_M and the ability to successfully turn off the device channel because of gate voltage screening effects at a certain depth in the channel.

While this tradeoff between doping and channel thickness is necessary to achieve good transistor operation as measured by the on-off current ratio, to perform gate length scaling, which can reduce power switch dynamic losses and improve the power frequency product in RF devices, we must also consider geometrical concerns related to the ratio between the gate length and channel thickness with the doping concentration as an additional parameter. These geometric effects as in other FET devices relate to the so-called ***short channel effects*** when the ***gradual channel approximation*** used for our model is no longer valid and the electric field along the gate is comparable to the field normal to the gate (i.e. the drain voltage begins to control the current in the channel). A full scale investigation of these effects requires extensive experiments of scaled gate lengths on similar material and is beyond the scope of the work presented here-if it is not impossible with the current maturity level of the material system. However, it is evident from our model that I_{DS} (Equation 18), R_{ON} (Equation 26), and G_M (Equation 27) all scale as other FET devices in proportion to the inverse of the gate length if the short channel effects are not dominant. Additionally, from Equation 29 it is evident that the cutoff frequency should also scale with the inverse of the gate length.

Equation 29 Cutoff frequency vs. gate length, *L*. *v* is the carrier velocity. The cutoff frequency is proportional to 1/*L*. The equation is similar to Equation 10.

$$f_T = \frac{v}{2\pi L}$$

In our lab, we have primarily investigated 2 μm-gate-length devices with channel thickness up to 200 nm and doping levels <1x10^{18} cm^{-3} maintaining a gate length-channel

thickness, L_G:d, ratio of >10:1. The primary concern with these devices has been sufficient turn-off, and thus, little has been done to characterize short channel effects. During recent pursuit of RF operation, however, we reduced the channel length to 0.7 μm, and through the process in Figure 64, reduced the channel thickness to ~90 nm maintaining our L_G:d ratio > 7:1 while reducing the gate length by a factor of 2.9.

The 0.7-μm-gate-length device was fabricated on a Si-doped MOVPE grown channel layer on a (100) Mg-doped semi-insulating substrate. The active carrier concentration, N_d, was ~1.3x10^{18} cm^{-3} in the channel and the mobility was ~96 cm^2/(V·s) as measured using the Hall effect on VDP structures nearby the device. A 25 nm ohmic cap layer with target doping of 1x10^{19} cm^{-3} was also grown, and the contact resistance, R_C, measured using TLM was 3.3 Ω-mm. DC and RF results are presented in Figure 66. The off-state voltage was -12.2 V which predicts a doping concentration of ~1.2x10^{18} cm^{-3} for a thickness of 90 nm from the model in Chapter 4. The maximum cutoff frequency, f_T, and maximum transconductance, G_{Msat}, were 3.0 GHz and 21.2 mS/mm, respectively, at a gate voltage V_G=-3.5 V. G_{Msat} can be compared to the model using Equation 27 which gives a saturated transconductance at V_G=-3.5 V of ~116.0 mS/mm which is much higher than the value in the device. The predicted saturation current at V_G = 0 V, I_{DSS} = 546 mA/mm, is also much higher than the measured value, I_{DSS} = ~150 mA/mm. This indicates again that negative surface charges may be present, and by adding a gate voltage factor (Equation 23), ΔV_G = 7.3 V, we obtain reasonable values for G_{Msat} (29.2 mS/mm) and for I_{DSS} (152 mA/mm) from the model. The high ΔV_G value indicates a greater effect from negative surface states on the applied gate voltage which may result

from the etched surface of the channel during the gate recess step. Previous results have also shown that simply using a narrower channel thickness results in a more positive off-state voltage indicating that the effect of surface states dominates for thin channel layers [91]. The source of this effect requires further study.

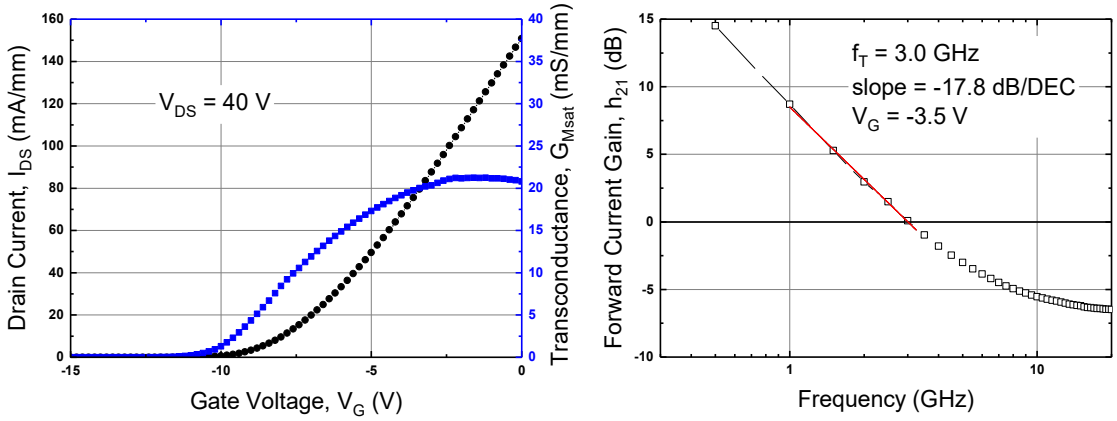


Figure 66 Left: Transfer curve (I_{DS}-V_G) for a β-Ga_2O_3 MOSFET with a 0.7 µm gate length. Right: Measurement of the cutoff frequency, f_T, of the same MOSFET using small signal scattering parameters to extract the forward current gain, h_{21}, versus frequency.

At a gate length of 0.7 µm, at the knee voltage (~12 V), a field of ~90 kV/cm is dropped across the gate length indicating from Figure 13 that it is very unlikely that saturation velocity has been reached for the doping level specified. To quantify the required L_G:d ratio to avoid short channel effects will require multiple channel thicknesses and gate lengths across very similarly doped samples which are unavailable at this time. In our case, we compare the result above with a 2-µm-gate-length device with a lower doping (6.3×10^{17} cm^{-3}) and thicker channel (200 nm) as shown in Figure 67. These values give a nearly identical volume charge under the gate. The 2-µm-gate-length

device had a peak G_{Msat} of ~8.7 mS/mm and peak f_T of 957 MHz at V_G = -15 V. Even though the comparison is not perfect the device with the gate length reduced by a factor of 2.9 had a 2.4X increase in G_{Msat} and a 3.1X increase in f_T which are reasonable values for a preliminary scaled gate length device.

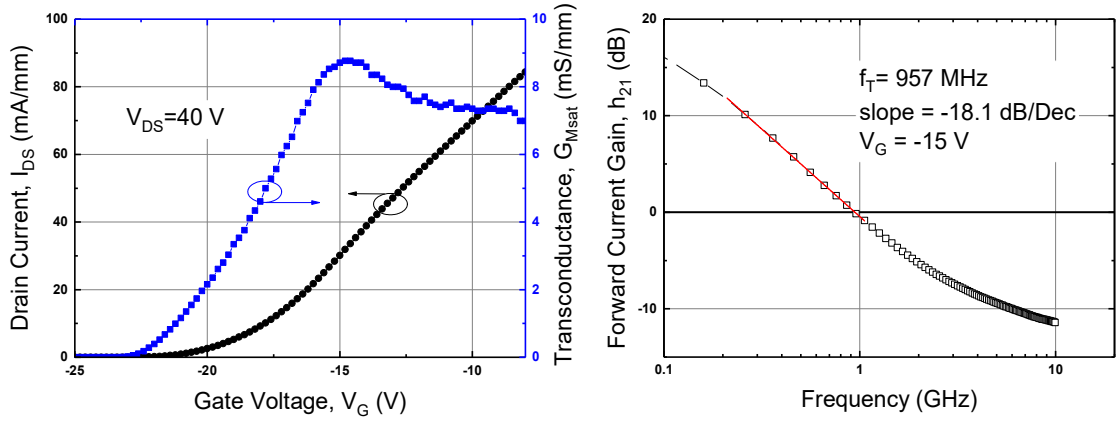


Figure 67 Left: Transfer curve (I_{DS}-V_G) for a β-Ga_2O_3 MOSFET with a 2 µm gate length. Right: Measurement of the cutoff frequency, f_T, of the same MOSFET using small signal scattering parameters to extract the forward current gain, h_{21} versus frequency.

β-Ga_2O_3 MOSFET Model Limitations

In this section we describe a few of the model limitations of the simple model from Chapter 4. The model can be immediately improved by adding empirical or physical models for high field velocity characteristics as presented in Figure 13 and for temperature dependence of the carrier concentration and mobility as was alluded to in the last section of Chapter 5. More difficult improvements include modeling the mobility in lieu of surface states and the normal field, modeling short channel effects as the gate

length is reduced, modeling device self-heating, and modeling of the gate and drain dispersion caused by surface states. Also, it is unclear if subthreshold characteristics and accumulation mode operation can be accurately predicted at all using the model.

State-of-the-art β-Ga_2O_3 MOSFET devices have gate lengths >0.5 μm, and as shown in the last section, do not reach fields sufficient for velocity saturation (saturation occurs at ~200 kV/cm). The model proposed in Chapter 4, however, can be modified to estimate high field effects by adapting the velocity, v, in Equation 12 to include the effects of velocity saturation as shown in Equation 30. This simplified method is similar to the method used for silicon analytical models. Currently, device technology does not allow for verification of this model adaptation; however, when gate length scaling becomes available, it is simple to empirically measure the small signal cutoff frequency versus gate length as in Equation 29 to determine when the velocity, v, becomes saturated, $v = v_{sat}$, and to verify the model result by comparing electrical measurements of saturated versus unsaturated IV curves.

Equation 30 Electron velocity in a MOSFET channel depending on the lateral field, $E(y)$, the mobility, μ, and the lateral electric field required for saturation, $E_{sat}=v_{sat}/\mu$. n is a fitting parameter for a velocity versus field curve such as in Figure 13. For n=1 an analytical solution can be found as shown in [1].

$$v = \frac{\mu E(y)}{\left\{1 + \left({}^{E(y)}/_{E_{sat}}\right)^{n}\right\}^{1/n}} = \frac{\mu \frac{dV}{dy}}{\left\{1 + \left(\frac{\mu}{v_{sat}}\frac{dV}{dy}\right)^{n}\right\}^{1/n}}$$

Temperature dependent mobility has been added to the model using an empirical fit to measured Hall Effect data in Chapter 5. This can also be done by adding an

effective mobility that depends on the temperature such as described by Ma et al. in [49] and shown in Equation 31. Equation 31 was used previously to estimate the sheet resistance and mobility versus active carrier concentration shown in Figure 63, and it can be easily implemented in the model for a more physical representation of the device at different ambient temperatures. The temperature dependence of the carrier concentration can also be easily incorporated as performed previously by replacing N_d with the solution for n from Equation 24 assuming all other parameters (N_A, N_D, E_D) are known for the given channel dopant.

Equation 31 An empirical expression for the relationship between mobility, μ_{eff}, temperature, T, and active carrier concentration, N_d. Reprinted with permission from [49]. The expression is an empirical fit to numerical solutions for the mobility effects of several scattering mechanisms.

$$\mu_{eff} = \frac{56\left\{\exp\left[\frac{508}{T(\mathrm{K})}\right]-1\right\}}{\left\{1+\frac{N_d(\mathrm{cm}^{-3})}{[T(\mathrm{K})-278]2.8\mathrm{x}10^{16}}\right\}^{0.68}}\frac{\mathrm{cm}^2}{\mathrm{Vs}}$$

It is possible, although, significantly more difficult to incorporate the mobility dependence on channel depth and normal field into our simple model. Currently, the normal field from the gate voltage can only be raised to a small positive voltage (~4 V) before significant leakage currents or gate oxide degradation become a factor. Additionally, the negative surface traps play a large role in reducing the normal field applied and would cause difficulty in measuring the field's effects on the channel mobility. An empirical expression, however, is possible if the negative surface states can be quantified and maintained in a design of experiments with constant active carrier

concentration and varying channel thickness and positive gate voltages. The model could then be implemented to match the measured data for these variations leading to an empirical expression for the effective mobility at a given channel depth or a given normal field. Current material system immaturity does not allow controlled results for conducting this type of model improvement.

Other than velocity saturation, which is fairly easy to model and measure, short channel effects such as drain induced barrier lowering (DIBL) and channel length modulation are difficult but plausible as an improvement to our analytical model. Like silicon models, channel length modulation (not currently evident in long channel devices) can be implemented by assuming a drain voltage dependent reduction to the channel length, $L\text{-}\Delta L(V_D)$. Unfortunately, silicon models assume the charge sheet approximation where the singular value of ΔL is not dependent on the vertical direction, but this is not the case in the volume conducting channel of our β-Ga_2O_3 MOSFETs where channel pinch off is achieved to different degrees from the bottom of the channel up to the gate oxide interface. Fortunately, this reduces the impact of channel length modulation until the gate length becomes even smaller, which as predicted above means the channel thickness must also be thinner leading to a more silicon-like charge sheet result. Additionally, the variation of ΔL through the channel thickness should be a smooth function of the vertical distance, x, making the potential for a mathematical expression more likely. As gate length scaling becomes more prominent these assumptions can be verified with our model.

DIBL manifests as a drain voltage dependent change in the threshold voltage, and it is related to the effective lowering of the lateral barrier height at the source side of the channel by the lateral field caused by the drain-source voltage. Because of the large magnitude of off voltages (and thus knee voltages), some amount of DIBL has already been observed in β-Ga_2O_3 MOSFETs with relatively long channels, although the measurement has not been quantified. DIBL can be implemented in our model by adding an empirical expression for the off-state voltage with a dependence on the drain voltage. Again, the previous discussions on gate length scaling versus channel thickness affect the ability to perform the empirical analysis accurately with the current maturity level of the material system.

Self-heating and gate and drain dispersion effects can all theoretically be added to our analytical model as well. Temperature dependent analysis of our model was already performed in Chapter 5, but this analysis was performed using pulsed-IV measurements at different base plate temperatures to virtually eliminate self-heating. The low thermal conductivity of β-Ga_2O_3 indicates that the device channel will significantly self-heat as power levels increase to those expected for common modes of operation for a power transistor. In these cases, the temperature effects shown in Chapter 5 will occur with or without changes to the ambient temperature, and it becomes pertinent to understand the channel temperature of the device resulting from self-heating at a given operating point to accurately predict the electrical performance. Normally, self-heating effects can be modeled by including a thermal resistance, R_{th} (in K/W), that is used to calculate the change in channel temperature from ambient, ΔT_{ch} (in K), at a given power level, P_{tot} (in

W). The thermal resistance is extracted for the specific device layout using numerous extraction techniques including direct channel temperature measurement using infrared thermometry techniques [159] or extraction of channel temperature through comparison of electrical performance for a device measurement with a self-heating signature (usually DC) versus device measurements without self-heating (usually pulsed-IV) at several ambient temperatures [154], [160]. Unfortunately, for β-Ga_2O_3 MOSFETs the devices also exhibit gate and drain dispersion as shown in Figure 68 whereby the on resistance, R_{ON}, and drain current, I_{Dsat}, are affected by the previous state of the gate, V_G, or drain, V_D, voltage. These changes in electrical performance can be attributed to the level of occupation of negative trap states under the gate or in the source and drain access regions. The effects of dispersion can be modeled by including gate and drain RC circuits with time constants similar to the time constants of trap states that correct the current source based on empirically obtained trap characteristics [161]. While self-heating and dispersion effects are not unique to β-Ga_2O_3, the effects can be more difficult to differentiate between because of the low thermal conductivity which causes self-heating effects to manifest at lower power levels (possibly before the knee voltage [133]) and the apparent long time constants of trap states which can cause anomalous results even in near DC measurements. Additionally, the possibility of device degradation or catastrophic failure due to immaturity of the material system and the intent to operate at high power, high temperature, or high voltage further complicates the analysis of dispersion and self-heating effects. Still, with extensive advanced measurement

techniques these items can be implemented in future iterations of the analytical model from Chapter 4.

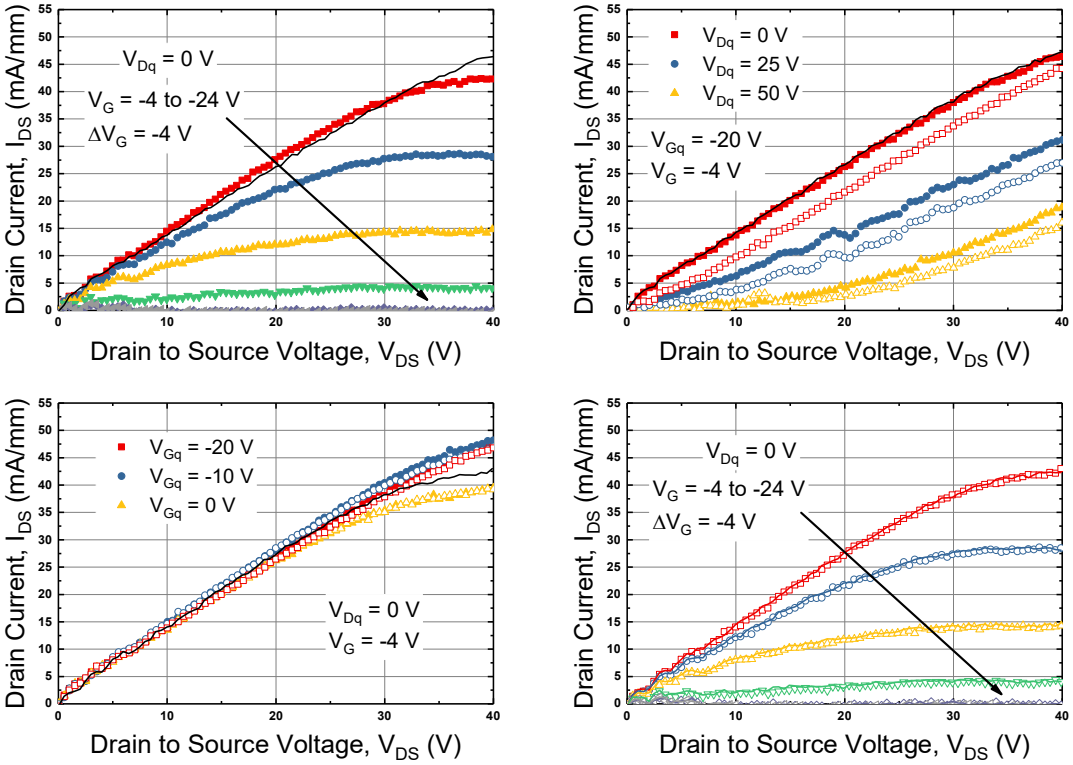


Figure 68 Pulsed IV measurements of a β-Ga_2O_3 MOSFET with a 150 nm channel on a semi-insulating Fe-doped substrate with N_d ~ 8x10^{17} cm^{-3} (Sn-doped) showing the effects of gate and drain dispersion. All pulsed measurements used a 200 ns pulse with a 0.0075% duty cycle. The V_G = -4V for the next curve going clockwise is shown by the black line for continuity. Top Left: Original pulsed-IV (I_{DS}-V_{DS}) curves for the device. Top Right: Drain dispersion effects showing changes in the on resistance at different quiescent drain voltages. This device mainly suffered from drain dispersion effects. Bottom Left: Gate dispersion effects showing changes in the saturation current I_{Dsat} for different quiescent gate voltages. This device did not exhibit large gate dispersion. Bottom Right: First and last measurement after extensive pulsed testing showing that this device exhibited almost no degradation; however, it had not been tested thermally.

While it is predictable from the discussion above and the progression of other small and large signal models, that the previously described effects can eventually be incorporated in our model, creating a physical analytical model that accurately predicts

the subthreshold characteristics (i.e. subthreshold swing and off-current) or smoothly predicts both the depletion and accumulation mode characteristics of β-Ga_2O_3 MOSFETs may only be achievable with new theoretical formulations or extensive mathematical estimations of the device performance. In our model in Chapter 4, we have labeled the point when the device no longer conducts any current the off-state voltage, V_{off}. The modeled device operation is thus broken into only three modes of operation; off ($V_G<V_{off}$), depletion ($V_{off}<V_G<V_{FB}$), and accumulation ($V_G>V_{FB}$). In these devices, the model assumes because of the junction-less lateral structure (n-n-n) that the dominate current in all modes is drift current. This is in contrast to silicon MOSFETs where device current is dominated by drift current in the off state, diffusion current in weak inversion, and again by drift current in strong inversion and the devices do not conduct current in the accumulation region [1]. It is unlikely then that subthreshold characteristics can be predicted using methods borrowed from silicon MOSFETs. Additionally, it is difficult to make a smooth transition from the depletion to accumulation mode using a surface potential model because of the sign change of the voltage drop across the gate oxide when the gate voltage crosses the flat-band value ($V_G=V_{FB}$). New methods need to be examined to create models that incorporate these two things. For now, our model simply models the subthreshold using drift current; predicting a uniform *SS* based on the depletion approximation and providing no prediction for the off-state current level. Additionally, the accumulation mode is modeled using a piece-wise solution that sums the additional accumulation current with the maximum depletion current (see Equation 22). In Figure 69, it is shown that the model does not accurately predict the subthreshold

characteristics using our basic approach. The source of the discrepancy, however, has not been analyzed. Since the model V_{off} was extracted from the minimum of the C-V characteristic in Figure 45, the variation in the MOSFET turn-off may be related to the difference between the ability to modulate the conducting versus the non-conducting channel (Coulomb screening effects), but further investigation is required. The model does predict the accumulation current accurately as shown in Figure 44 up to a small forward gate bias; however, the level of accumulation obtained in current β-Ga_2O_3 MOSFETs has not been confirmed. Further, studies can be performed by increasing the gate oxide thickness to provide more positive forward bias and achieve good accumulation results to confirm the model; however, the piecewise nature of the model still makes it limited for calculation where a continuous relation between the surface potential and charge is desirable.

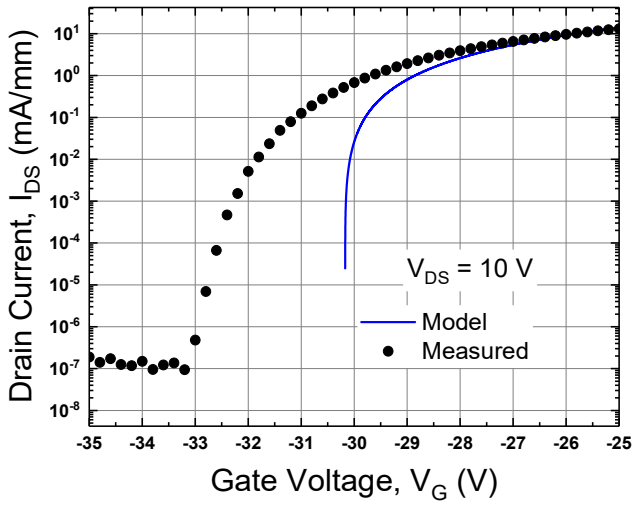


Figure 69 Log scale plot of the transfer characteristics (I_{DS}-V_G) of a β-Ga_2O_3 MOSFET. While a simple analytical model using a drift current assumption can accurately predict the depletion mode on current as shown in Figure 44, it overestimates the slope of the device turn-off when the current nears its minimum value.

The model improvements and limitations described in this chapter provide some future research for modeling of β-Ga_2O_3 MOSFETs. In the next section, we will discuss some future research related to the design of the FETs themselves.

7. FUTURE GALLIUM OXIDE RESEARCH

Performance of the current state-of-the-art β-Ga_2O_3 MOSFETs can be predicted by the model developed in Chapter 4 as shown in Chapter 5 and Chapter 6. It is also likely that this simple model can be used to help develop some future devices that are likely to be pursued in the gallium oxide material system. In this Chapter, we describe a future vertical FET device and a heterojunction FET device, and we show how the previous success of our simple model can be used to aid in the design of these devices.

Vertical Ga_2O_3 FETs

In Chapter 1, we introduced the figures of merit for a unipolar device developed by Baliga. For lateral devices, however, the interface at the surface causes spikes in the electric field often leading to premature voltage breakdown in the semiconductor or in the materials fabricated on top of the semiconductor (e.g. passivation layer) even if the device design is optimized using Baliga. Thus, a vertical device that confines the breakdown characteristics entirely to the material of interest, in this case β-Ga_2O_3, is the ideal device for power switch applications. It is also true that vertical devices allow the highest density of devices per unit surface area and therefore, have the highest current density per area. While RF applications often still use lateral devices because of easier scaling, it is beneficial for power switch applications to investigate the plausibility of vertical β-Ga_2O_3 MOSFETs.

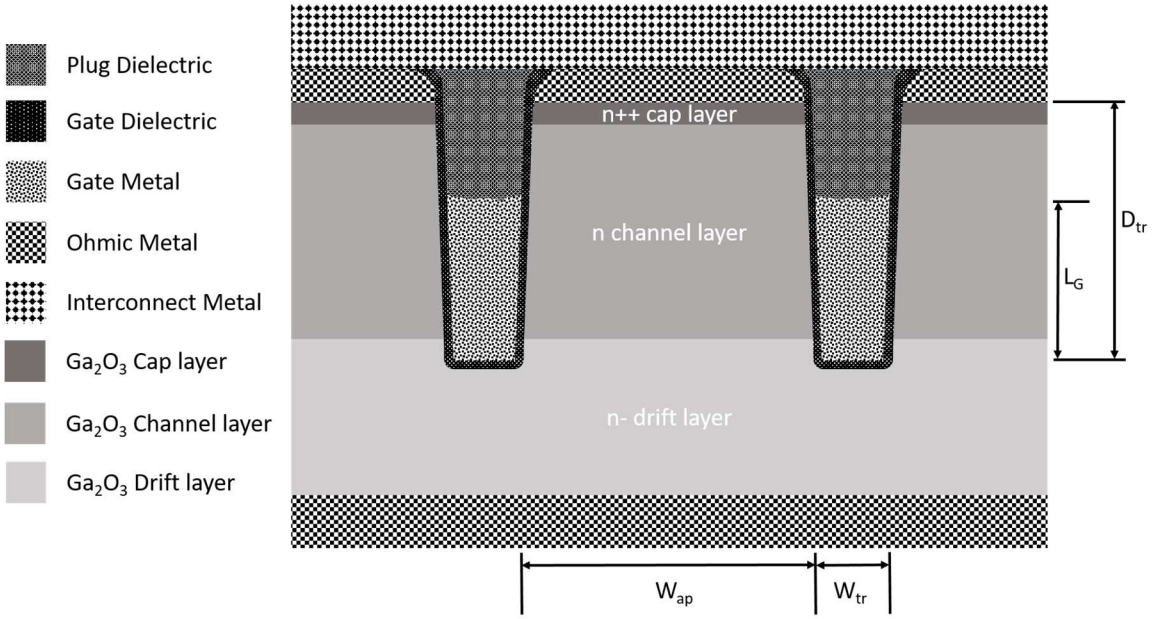


Figure 70 Initial design for a vertical β-Ga_2O_3 MOSFET for power switching applications. The aperture width, W_{ap}, trench width, W_{tr}, trench depth, D_{tr}, and gate length, L_G, all present fabrication or design challenges for implementing vertical device designs.

Figure 70 depicts a conceptual cross section of a vertical β-Ga_2O_3 MOSFET. The vertical design presents several fabrication and design challenges compared to the lateral designs previously discussed. First, there is a tradeoff between the aperture width, W_{ap}, and the doping level in the channel layer, N_d. The off-state voltage, V_{off}, will be determined by N_d and $d=W_{ap}/2$ in Equation 19. It is clear from Figure 62 that there is also a maximum W_{ap} at a given N_d that can be sufficiently turned off; thus, N_d is limited by the fabrication limits placed on the width of the aperture. It is also evident from, Figure 70 that the source ohmic contact area is directly determined by W_{ap} leading to potential high source resistance or source starvation of the channel. This issue is common for depletion-mode devices such as n-type GaN FETs but is not true for an inversion layer channel

device such as a silicon MOSFET because the channel is confined to the sidewall. An excellent presentation on the development of GaN vertical devices was provided by Sun, Zhang, and Palacios in ref. [119], and a description of silicon devices was presented by Omura in ref. [116]. For GaN, many of the same issues exist as do for Ga_2O_3; however, the GaN material (perhaps only because of its maturity) has available p-type dopants and allows a poorly conducting inversion layer to form. Still unique methods of aperture design are required for GaN vertical devices.

A second design issue for vertical FETs is that the gate length, L_G, is determined by the trench depth, D_{tr}. If the fabrication process does not support large vertical trenches, then the device will be limited to shorter gate lengths where short channel effects can dominate the device characteristics as discussed in Chapter 6. Numerous fabrication issues also occur with the trench gate including the gate contact required along the trench sidewall. This leads to some tradeoff between the trench width, W_{tr}, and the thickness and uniformity of the gate metal. The surface area of the gate metal also determines the gate resistance, R_G. These complications are common among all vertical FET designs because the gate contact is made vertically; however, the restrictions placed on the aperture width, Wap, as mentioned above further complicate the design for Ga_2O_3 devices because the gate metal cannot extrude the surface of the trench. This is similar to GaN, but not true for Silicon where the gate metal often extrude the trench and then is simply covered with a dielectric layer above the surface to avoid shorting to the source.

A third challenge is the doping of the drift layer, N_{drift}. Ideally, N_{drift} and the depth of the drift region are designed to provide the desired breakdown voltage (with lowest

loss) as found by Baliga. The channel length, L_G, need only be long enough to support the critical field without depleting all of L_G (this avoids punch through when the device is off). As mentioned above, however, an upper limit exists for the doing level of the channel layer, N_d; thus, a tradeoff exists between L_G, W_{ap}, and N_{drift}. The lightly doped N_{drift} region forces the channel doping, N_d, and gate length, L_G, to assume certain values for appropriate current blocking, thus forcing the W_{ap} needed to turn the device off and the D_{tr} needed to deposit the gate metal with gate length L_G. Again, the problem is similar to those in n-type GaN devices, but does not occur in Silicon devices where the inversion channel layer is p-type and is inverted to create the n-type channel. In GaN, unique backside processing is being investigated to optimize the vertical device drift region thickness [162].

Other process complexities and tradeoffs also exist when creating a vertical device, but these three problems demonstrate how our analytical model along with the figures of merit and design tradeoffs described in Chapter 6 can be used to design the device around the available process technology and to evaluate the performance of the devices against theory after fabrication.

β-Ga_2O_3 Heterojunction Field Effect Transistors

As shown in Table 4, β-Ga_2O_3 has low mobility compared to incumbent power semiconductor materials. Creating a heterojunction to confine charge carriers to the surface of the β-Ga_2O_3 is one way to potentially increase the carrier mobility by limiting the carrier movement to the horizontal direction (i.e. along the channel). Additionally, heterojunction field effect transistor (HFET) structures like the GaAs MODFET use

barrier layer dopants to create a conducting channel in an otherwise very low impurity GaAs channel [163], [164]. This reduces the level of ionized impurity scattering which normally limits the mobility at high donor levels (see Figure 11). Thus, for lateral switching devices where the on resistance depends inversely on the mobility (Equation 26) and lateral RF devices where the saturated transconductance depends directly on the mobility (Equation 27), it is highly desirable to investigate the potential for β-Ga_2O_3 HFETs.

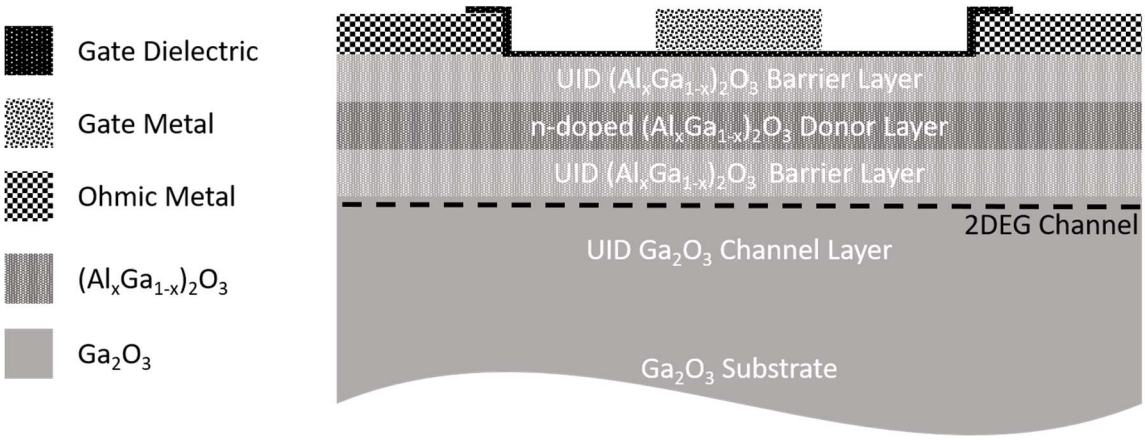


Figure 71 Concept for a β-Ga_2O_3 heterojunction field effect transistor (HFET) for RF and power switching applications. Carriers in the two dimensional electron gas (2DEG) channel near the interface between Ga_2O_3 and the wider bandgap $(Al_xGa_{1-x})_2O_3$ are supplied by donors in the n-type $(Al_xGa_{1-x})_2O_3$.

Figure 71 shows a conceptual design for a β-Ga_2O_3 HFET with many similarities to the design of AlGaAs/GaAs MODFETs. In the device, the conduction band offset between Ga_2O_3 and $(Al_xGa_{1-x})_2O_3$ is used to create a triangular quantum well at the surface of the Ga_2O_3 that confines movement of the electrons to only two directions (i.e. along the channel and along the gate width). The specifics of the development of these

devices is beyond the scope of the research presented here; however, it is evident that the model presented in Chapter 4 can be used during the HFET development process to determine achievement of some development goals.

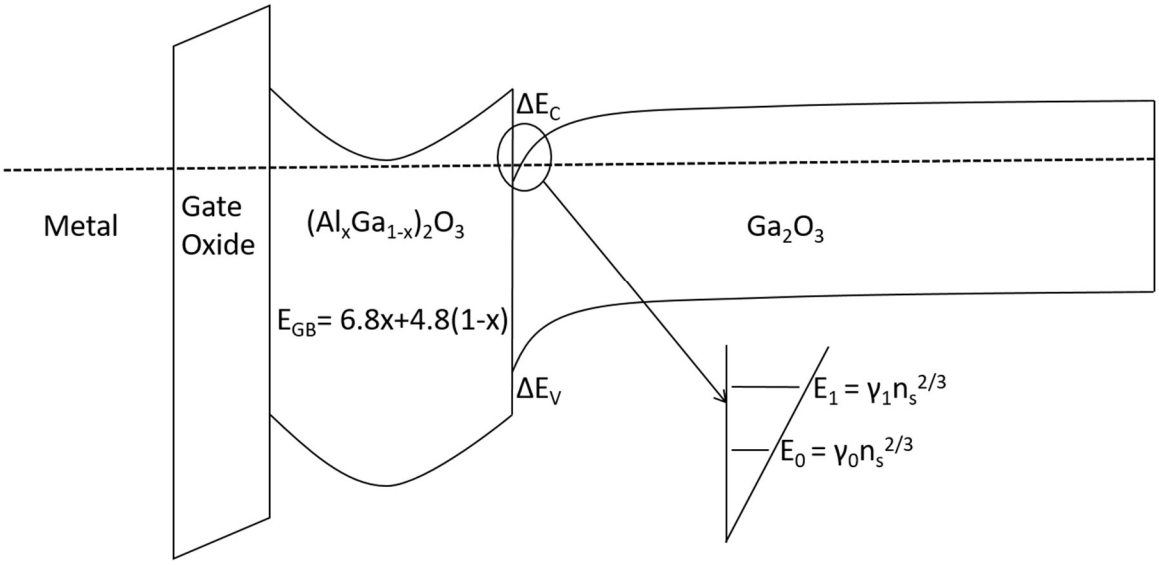


Figure 72 Depiction of the energy band structure of an AlGaO/GaO heterojunction field effect transistor (HFET) showing exaggerated conduction and valence band offsets. A two dimensional electron gas (2DEG) is formed in a triangular quantum well at the heterojunction interface from the offset of the conduction bands, ΔE_C. The available energies in the quantum well, E_0 and E_1, are quantized as shown with γ_x experimentally determined and n_s the sheet charge in the quantum well. A linear approximation of the band gap, E_{GB}, for the $(Al_xGa_{1-x})_2O_3$ barrier is also included.

Figure 72 depicts a simplified band diagram of an AlGaO/GaO HFET. The development of these devices is underway[165]–[169]. In these studies, delta-doping of both the Ga_2O_3 [167]and $(Al_xGa_{1-x})_2O_3$ [166], [168]has been performed and verified in devices, expected carrier confinement has been observed by C-V measurements [168], [169], and devices have been fabricated with different sheet carrier concentrations based on the location of the modulation doping in the $(Al_xGa_{1-x})_2O_3$ layer (unpublished).

However, the key breakthrough for an HFET, increased mobility in the two dimensional channel, has not yet been realized, and therefore, a concentrated sheet charge appears to be the only benefit thus far. Our model in Chapter 4 would require numerous updates to include HFET devices such as a change to a sheet carrier concentration, n_s, rather than a volume carrier concentration, N_d, which is calculated from the position of the fermi level in the quantum well and an adjustment to the off-state voltage to include only the discrete energy levels available in the triangular quantum well for carrier conduction. These changes are similar to those previously mentioned for GaN analytical models in the beginning of Chapter 4. The model can be used, however, to quickly compare the off-state voltage (Equation 19) of devices with thin channels to HFET devices with thin, quantum confined channels. It can also be used to compare the thin channel or delta-doped device on state current (Equation 18) with a given mobility to HFET devices with a higher expected mobility to quantify the HFET improvement beyond simple mobility measurements. These studies and additional device experiments can be used to determine the value of the HFET designs compared to conventional designs, and eventually, the model can be updated like those of GaN to include HFET operation.

It is clear from these examples that our simple model derived using approximations from silicon can be used as the β-Ga_2O_3 material system is matured and device libraries are expanded to include HFET and vertical transistor devices. The last chapter concludes this discussion and summarizes all of the results presented.

8. SUMMARY AND CONCLUSION

As a material gallium oxide, and particularly the stable β polymorph, β-Ga_2O_3 has promising characteristics for high voltage, high power, and high temperature switch and possibly RF applications. As described in the previous chapters, the combination of three characteristics set β-Ga_2O_3 apart from other power semiconductor materials. No other semiconductor (i.e. Si, GaN, diamond, or SiC) or insulator (i.e. AlN or various oxides), as yet, combine an extremely high critical field strength related to a wide bandgap of >3 eV, inexpensive, defect-free native substrates from melt growth techniques, and a broad range of conductivity control through n-type doping. In this Chapter, we conclude with a discussion of these three competitive advantages in relation to our models and the previously described figures of merit to better predict how β-Ga_2O_3 devices may be used in the broader power semiconductor devices market in the future. Along the way, we caveat our discussion with some of the shortfalls in the material system that must be overcome to achieve total success (i.e. supplanting current technologies) even though it is more likely that β-Ga_2O_3 will become another option for designers rather than a complete power semiconductor solution by itself.

In our lab, the transistor three terminal breakdown voltage related to a given doping concentration has correlated well with the predictions of Baliga for a material with the expected 8 MV/cm critical field of Ga_2O_3 as shown in Figure 73 and described

in Chapter 1. This promising trend is insufficient to establish the field strength because the devices have not been scaled appropriately to achieve the maximum field in the drift region. Still, this result combined with already measured breakdown fields greater than those of GaN or SiC [92] indicate high potential for β-Ga_2O_3 devices that operate at extremely high voltages. The current lack of acceptor dopant species, however, may limit the ultimate voltage performance compared to SiC and GaN which both have p-type material available albeit limited compared with n-type material [118], and the current critical field level does not exceed that of diamond.

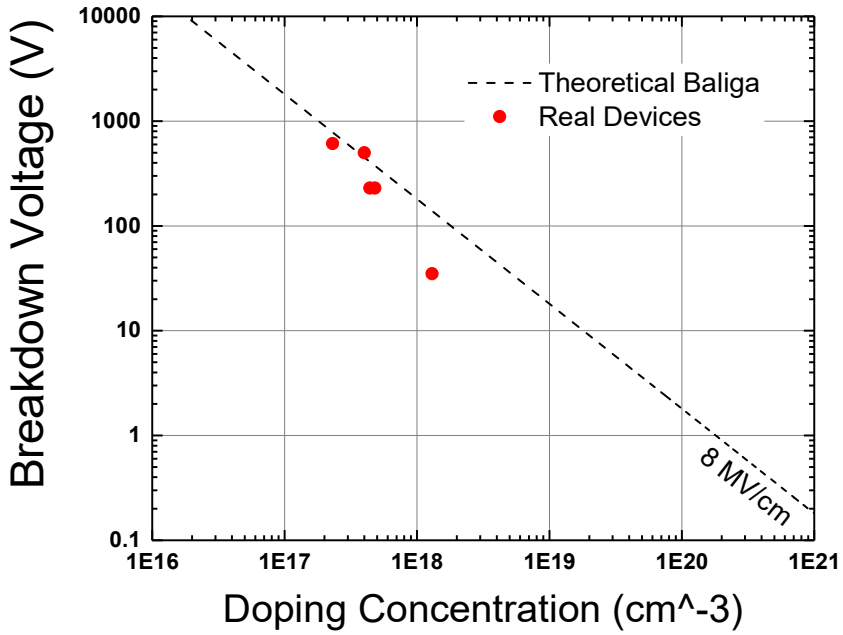


Figure 73 Breakdown voltage versus doping concentration for several real β-Ga_2O_3 MOSFETs compared to the prediction by Baliga (see Figure 5) for a material with 8 MV/cm critical field strength. Many real devices already operate close to the theoretical line.

The high breakdown field strength also positions β-Ga_2O_3 well for power RF devices and low dynamic switch losses. In fact, the power-frequency product predicted by Johnson's figure of merit is similar to GaN and several switching figures of merit are better than GaN. This indicates the potential for β-Ga_2O_3 to operate in RF devices with extremely high power levels or high frequency switches with extremely low losses. High frequency performance, however, is limited by fabrication technology where a shorter gate length is required for β-Ga_2O_3 devices to match the gate transit times of longer gate length devices in higher carrier velocity materials like GaN HEMTs.

The answer to the shortfalls for β-Ga_2O_3 mentioned above, may of course be the defect-free native substrate which can lead to low cost, high yield, large area vertical and lateral devices with extremely high voltage and high current operation at, at least, moderately high frequencies. Here, the limitation becomes the poor thermal conductivity of the material, but this again can be overcome by engineering thermal solutions, operating in high temperature environments, and/or avoiding self-heating by application engineering.

Our prediction for the power semiconductor market is, thus, shown in Figure 74. Here SiC with higher expense than Si and more maturity than β-Ga_2O_3 assumes the high voltage, low to moderate frequency market. GaN assumes the high frequency, moderate voltage market because of its achievement of HEMT devices, lack of vertical devices, and higher expense than Si. Finally, β-Ga_2O_3 assumes the moderate frequency, high voltage market because of its expected lower cost than GaN or SiC and previously mentioned material advantages. It is also entirely possible to predict the-inexpensive-to-

produce β-Ga_2O_3 supplanting some of the range of SiC in high voltage devices and of GaN in high frequency devices. It should also be noted that while Figure 74 is nice for a brief market comparison it does not include all of the performance goals of the power semiconductor market such as the desire for enhancement-mode operation, specific current-voltage tradeoffs for real applications, or material and process integration requirements.

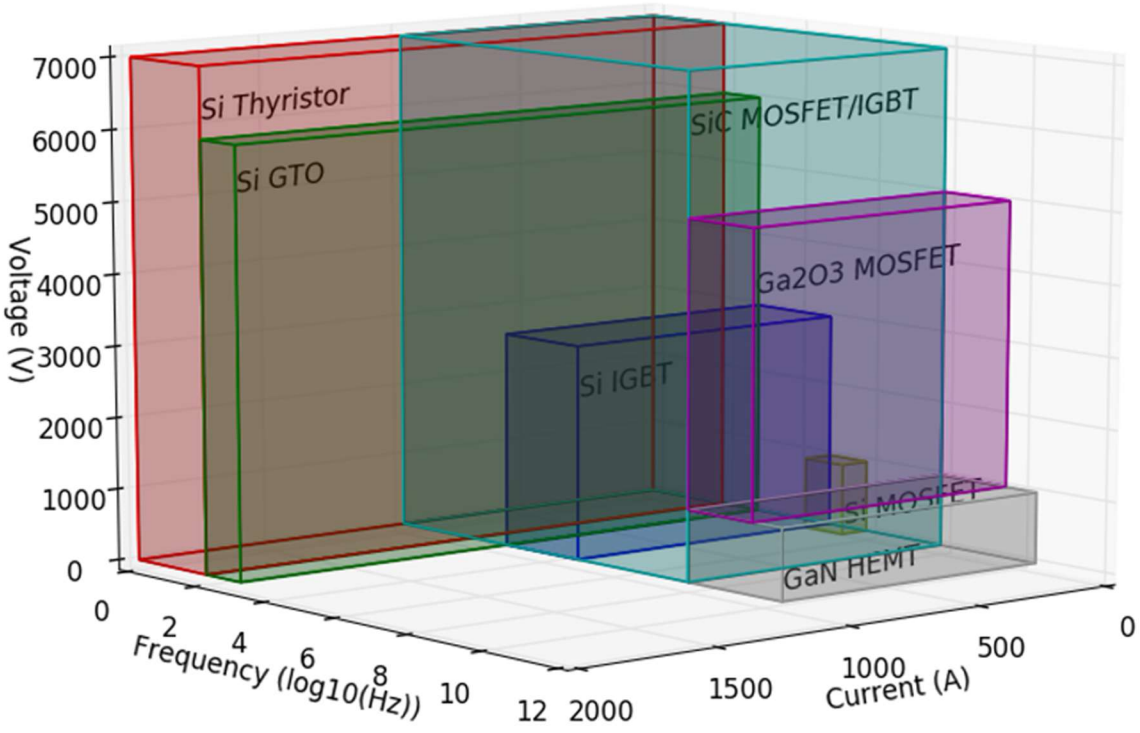


Figure 74 Potential future of power semiconductor device operating characteristics for maximum operating voltage, current, and frequency that each type of device can achieve. We predict extremely high voltage operation to be dominated at low frequencies by SiC insulated gate bipolar transistors (IGBT) and field effect transistors, extremely high frequency power devices to be dominated by GaN high electron mobility transistors, and moderate high frequency moderate high voltage devices to be dominated by Ga_2O_3 MOSFETs. Low performance considerations are dominated by cost and high performance considerations are dominated by the materials intrinsic properties. Adapted from https://en.wikipedia.org/wiki/Power_semiconductor_device.

To achieve even this modest market share, scaling and fabrication improvements can begin to be made immediately to move devices in the β-Ga_2O_3 material system toward their ultimate performance for conduction and total dynamic switch losses. Additionally, developments like those mentioned in Chapter 7 should be pursued.

Our simple analytical model developed in Chapter 4 provides an excellent tool to quickly assess device developments as engineers work to realize the strengths of β-Ga_2O_3 in real devices and applications. In Chapter 5, we demonstrated the applicability of this model for channel changes (doping and thickness), gate dielectric changes, and operating temperature changes, showing that the assumptions used for silicon MOSFETs, namely the gradual channel approximation and the depletion approximation, apply for state-of-the-art β-Ga_2O_3 depletion mode MOSFETs at least in the depletion region if not in accumulation. We further clarified the implications and limitations of the model in Chapter 6 for creating the ultimate performance for β-Ga_2O_3 MOSFETs for RF and power switching devices realizing some of the limitations for the current device design in relation to achieving the ultimate for Baliga's and Johnson's figures of merit.

In Chapter 7 we evaluated our simple model's applicability to future devices that may be developed using β-Ga_2O_3 including heterojunction field effect transistors and vertical field effect transistors. The simple model can aid the design or verification for each of these devices that will be game changing if they can be realized in the β-Ga_2O_3 material system. Additionally, we note that the analytical model lends itself well to future improvements toward a simple analytical model for circuit designs when device maturity warrants this type of development. The model implemented in VerilogA is well suited to

adaptation to many circuit design tools and can be utilized to provide a rapid assessment of the performance of β-Ga_2O_3 MOSFETs in complex RF and power switching circuits as has been done with silicon device models in the past.

The rapid development of β-Ga_2O_3 MOSFETs may create the misperception that this material system is mature; however, it remains in its infancy with the first relevant devices fabricated only about five years ago. Development of this material system has and will continue to benefit greatly from the availability of inexpensive, melt-grown, defect-free, native substrates with large area; doping control over a large range with several epitaxial growth techniques; test techniques and equipment developed for incumbent power switch and RF devices like SiC and GaN; and simple physical understanding of MOSFET and FET devices from development of silicon and GaN models to evaluate material performance through the creation of new models like the one described here.

APPENDIX A: PYTHON CODE FOR BANDSTRUCTURE

```
import matplotlib.pyplot as plt
import matplotlib.text as txt
import numpy as np
from mpl_toolkits.mplot3d import Axes3D
from matplotlib import cm
import csv
import Util as UT

#Constants
epsFS = 8.854e-12 #F/m
elecQ = 1.602e-19 #C
boltz = 1.38e-23 #m^2*kg/(s^2*K)

#Material Parameters
workM = 5.33 #eV
workO = 2.5 #eV
affS = 4.0 #eV
affO = 2.5 #eV
EgS = 4.8 #eV
EgO = 6.8 #eV (Aluminum Oxide)
epsS = 10.2 *epsFS #F/m
#epsO = 20 *epsFS #F/m (Hafnium Oxide)
epsO = 8.5 *epsFS #F/m (Aluminum Oxide)
NcS = 3.71e18 * 100**3 #1/m^3

#Environmental
roomTemp = 300 #K
kt_q = boltz*roomTemp/elecQ

#Geometry Parameters
tox = 20e-9 #m
ts = 200e-9 #m
Nd = 5e17 *100**3
#Nd = 1.7e18 *100**3 #1/m^3
gateW = 422e-6 #m
gateL = 2e-6 #m
numFing = 1
gateP = gateW*numFing

#Measured Values
mu = (15.1)/(100**2) #m^2/(V*sec)

workS = affS-kt_q*np.log(Nd/NcS)

print("The semiconductor Work Function: " + str(workS))
```

```
distance = np.arange(-120, 300)
VFB = workM-workS
Cox = epsO/tox
Vth = VFB - (elecQ*Nd*(ts**2)) /(2*epsS) - (elecQ*Nd*ts)/(epsO/tox)
Vg = VFB
Vd = 10

E_FB = []
E_CMNB = []
E_CMB = []
E_CO = []
E_VO = []
E_vacM = []
E_vacO = []
E_CS = []
E_VS = []
E_vacS = []
E_intS = []
E_FS = []

KA = (2*elecQ*Nd*epsS)/(Cox**2)
KC = (KA**2/4)-KA*Vg+KA*VFB
KB = Vg
KD = VFB
KF = np.sqrt(2*epsS/(elecQ*Nd))
if Vg>VFB:
    B = (np.sqrt(2*elecQ*(NcS-Nd)*epsS))/Cox
else:
    B = (np.sqrt(2*elecQ*(Nd)*epsS))/Cox
A = 1
if Vg>VFB:
    C2=-Vg-Vd+VFB
    C = -Vg+VFB
else:
    C2 = Vg-Vd-VFB
    C = Vg-VFB

surfPotS_half= (-B+np.sqrt(B**2-4*A*C))/(2*A)
surfPotS = surfPotS_half**2
print(surfPotS)
surfPotD_half = (-B+np.sqrt(B**2-4*A*C2))/(2*A)
surfPotD = surfPotD_half**2
if Vg>VFB:
    Vox = np.sqrt(2*elecQ*(NcS-Nd)*epsS*surfPotS)/Cox
else:
    Vox = np.sqrt(2*elecQ*Nd*epsS*surfPotS)/Cox
if Vg>VFB:
    xd = np.sqrt((2*epsS*surfPotS)/(elecQ*(NcS-Nd)))
else:
    xd = np.sqrt((2*epsS*surfPotS)/(elecQ*(Nd)))
if Vg>VFB:
    Vox = -Vox
    surfPotS = -surfPotS
print(Vox+surfPotS, Vg-VFB)
```

```
print(Cox*(Vg-Vth))
print(xd*(NcS-Nd)*elecQ+ts*Nd*elecQ)

for x in distance:
    E_FB.append(0)

for x in range(-120,-19):
    #E_CMNB.append(VFB)
    E_CMB.append(VFB-Vg)
    E_vacM.append(workM-Vg)
    E_CMNB.append(workM-Vg-workM)

for x in range(-20, 1):
    E_CO.append((Vox/(-20))*x+workM-Vg-affO-Vox)
    E_VO.append((Vox/(-20))*x+workM-Vg-affO-Vox-EgO)
    E_vacO.append((Vox/(-20))*x+workM-Vg-Vox)

for x in range(0, 201):
    if (x*1e-9) < xd:
        if(Vg>VFB):
            E_vacS.append(workS-(elecQ*(NcS-Nd)*(x*1e-9)**2)/(2*epsS)+(elecQ*(NcS-
Nd)*xd*x*1e-9)/epsS+surfPotS)
            E_CS.append(workS-affS-(elecQ*(NcS-Nd)*(x*1e-
9)**2)/(2*epsS)+(elecQ*(NcS-Nd)*xd*x*1e-9)/epsS+surfPotS)
        else:
            E_vacS.append(workS+(elecQ*Nd*(x*1e-9)**2)/(2*epsS)-(elecQ*Nd*xd*x*1e-
9)/epsS+surfPotS)
            E_CS.append(workS-affS+(elecQ*Nd*(x*1e-9)**2)/(2*epsS)-
(elecQ*Nd*xd*x*1e-9)/epsS+surfPotS)
    else:
        E_vacS.append(workS)
        E_CS.append(workS-affS)

E_intS = np.subtract(E_CS, EgS/2)
E_VS = np.subtract(E_CS, EgS)

fig, bandD = plt.subplots()
bandD.plot(distance, E_FB, linewidth = 2, color = 'green', linestyle = '--')
bandD.plot(distance[0:101], E_CMNB, linewidth = 2, color = 'black', linestyle =
':')
bandD.plot(distance[0:101], E_CMB, linewidth = 2, color = 'red')
bandD.plot(distance[0:101], E_vacM, linewidth = 2, color='black')
bandD.plot(distance[100:121], E_CO, linewidth = 2, color = 'blue')
bandD.plot([-20, -20], [E_VO[0], E_CO[0]], linewidth = 2, color = 'blue')
bandD.plot([0, 0], [E_VO[-1], E_CO[-1]], linewidth = 2, color = 'blue')
bandD.plot([0,0], [E_VS[0], E_CS[0]], linewidth = 2, color = 'black')
bandD.plot(distance[100:121], E_VO, linewidth = 2, color = 'blue')
bandD.plot(distance[100:121], E_vacO, linewidth = 2, color = 'black')
bandD.plot(distance[120:321], E_vacS, linewidth = 2, color = 'black')
bandD.plot(distance[120:321], E_CS, linewidth = 2, color = 'black')
bandD.plot(distance[120:321], E_VS, linewidth = 2, color = 'black')
bandD.plot(distance[120:321], E_intS, linewidth = 2, linestyle=':', color =
'black')
#bandD.text(distance[-1], E_FB[-1], 'Flat Band Level/Fermi Level of Bulk')
#bandD.text(distance[-1], E_vacS[-1], 'Vacuum Level')
```

```
#bandD.text(distance[-1], E_CS[-1], 'Conduction Band')
#bandD.text(distance[-1], E_VS[-1], 'Valence Band')
#bandD.annotate('Xs', xy=(105, E_CS[99]), xytext=(100, E_vacS[99]),
arrowprops=dict(arrowstyle='->', linewidth=3))
#bandD.annotate('Os', xy=(120, E_FB[114]), xytext=(115, E_vacS[114]),
arrowprops=dict(arrowstyle='->', linewidth=3))
#if Vg != VFB:
#    bandD.annotate('Ps', xy=(5, E_intS[-1]), xytext=(0, E_intS[0]),
arrowprops=dict(arrowstyle='->', linewidth=3))
#plt.figure(2)
#plt.plot(distance[0:100], UT.SimpDerivative(E_CMNB,distance[0:100]))
#plt.plot(distance[0:100], UT.SimpDerivative(E_CMB,distance[0:100]))
#plt.plot(distance[100:120], UT.SimpDerivative(E_CO,distance[100:120]))
#plt.plot(distance[120:320], UT.SimpDerivative(E_CS,distance[120:320]))
bandD.set_ylim([-6,8])
plt.show()
```

APPENDIX B: VERILOGA CODE FOR ACCESS RESISTORS

```
`include "disciplines.vams"
`include "constants.vams"

// ************************************************************
 // * Ga2O3 access region resistor model version 1.0
 // ************************************************************

module epiresgaogtod(in, out);
 //
 // Node definitions
 //
         inout           in, out ;   // external nodes
         electrical      in, out ;   // external nodes
 //
 //*** Local variables
 //
 real Per, mu_eff;
 //
 //*** material parameters
 //
 parameter real workM  =  4.33         from[0.0:inf];
 parameter real affS   =  4.0          from[0.0:inf];
 parameter real affO   =  0.95         from[0.0:inf];
 parameter real EgS    =  4.8          from[0.0:inf];
 parameter real EgO    =  7.0          from[0.0:inf];
 parameter real relS   =  10.0         from[0.0:inf];
 parameter real relO   =  22.3         from[0.0:inf];
 parameter real epsS   =  relS*`P_EPS0 from[0.0:inf];
 parameter real epsO   =  relO*`P_EPS0 from[0.0:inf];
 parameter real NcS    =  3.72e24      from[0.0:inf];
 parameter real mu     =  42.7e-4      from[0.0:inf];
 parameter real StoD   =  15e-6        from[0.0:inf];
 parameter real StoG   =  0.5e-6       from[0.0:inf];
 parameter real Vsat   =  1.1e5        from[0.0:inf];

 //
 //     ***geometry parameters
 parameter real TOX    =  20e-9        from[0.0:inf];
 parameter real TS     =  100e-9       from[0.0:inf];
 parameter real Nd     =  4.66e23      from[0.0:inf];
 parameter real W      =  422e-6       from[0.0:inf];
 parameter real L      =  2e-6         from[0.0:inf];
 parameter real Nf     =  1.0          from[1.0:inf];
 parameter real RC     =  62.5e-3      from[0.0:inf];
```

```
analog begin // Ga2O3 Access region resistance models

// calculated material and device parameters
 Per   = W*Nf;

 //mu_eff = mu*(pow((pow((mu*V(in,out)/(Vsat*L)),5)+1),(-4.0/5.0)));
 // Assign to I
 //
V(in,out) <+ I(in,out)*((RC/(Per))+((StoD-
(L+StoG))/(TS*Per*Nd*mu*`P_Q)));

end // analog
 endmodule
```

APPENDIX C: VERILOGA CODE FOR DRAIN CURRENT

```
`include "disciplines.vams"
`include "constants.vams"

// ************************************************************
 // * Ga2O3 linear/saturation model (surface potential) version 1.0
 // ************************************************************

module surPotGa2O3(d,g,s,b);
 //
 // Node definitions
 //
         inout           d,g,s,b ;   // external nodes
         electrical      d,g,s,b, dprime, sprime ;   // external nodes
 //
 //*** Local variables
 //
 real VG, VS, VD;
 real workS, VFB, COX, VTH, ID, Per, mu_eff, delVg;
 real KA, para; //These are constants used to simplify the solution of
the intergral
 //
 //*** material parameters
 //
 parameter real workM  =  4.33         from[0.0:inf];
 parameter real affS   =  4.0          from[0.0:inf];
 parameter real affO   =  0.95         from[0.0:inf];
 parameter real EgS    =  4.8          from[0.0:inf];
 parameter real EgO    =  7.0          from[0.0:inf];
 parameter real relS   =  10.0         from[0.0:inf];
 parameter real relO   =  22.3         from[0.0:inf];
 parameter real epsS   =  relS*`P_EPS0 from[0.0:inf];
 parameter real epsO   =  relO*`P_EPS0 from[0.0:inf];
 parameter real NcS    =  3.72e24      from[0.0:inf];
 parameter real mu     =  42.7e-4      from[0.0:inf];
 parameter real StoD   =  15e-6        from[0.0:inf];
 parameter real StoG   =  0.5e-6       from[0.0:inf];
 parameter real Vsat   =  1.1e5        from[0.0:inf];

 //
 //     ***geometry parameters
 parameter real TOX    =  20e-9        from[0.0:inf];
 parameter real TS     =  100e-9       from[0.0:inf];
 parameter real Nd     =  4.66e23      from[0.0:inf];
 parameter real W      =  422e-6       from[0.0:inf];
```

```
 parameter real L      =  2e-6         from[0.0:inf];
 parameter real Nf     =  1.0          from[1.0:inf];
 parameter real RC     =  62.5e-3      from[0.0:inf];


analog begin // Ga2O3 surface potential model

VG = V(g, b); VS = V(s, b); VD = V(d, b);

// calculated material and device parameters
 workS = affS-$vt*log(Nd/NcS);  //the work function of the
semiconductor
 VFB   = workM-workS;
 COX   = epsO/TOX;
 Per   = W*Nf;
 VTH   = VFB-`P_Q*Nd*(pow(TS,2))/(2*epsS)-(`P_Q*Nd*TS)/(epsO/TOX);

// calculate the integral constants
 KA = sqrt(2*`P_Q*Nd*epsS/(2*COX));

delVg = 2.12;//(0.58367)+(0.92081*exp(0.15438*(VG-VS)));
 if (VD-VS>=VG-VS-delVg-VTH)
      para=VG-VS-delVg-VTH;
 else
    para=VD-VS;
 mu_eff = mu*(pow((pow((mu*(para)/(Vsat*L)),5)+1),(-4.0/5.0)));
//Surface potential based calculation of ID in the linear region
 if ((VG-VS-delVg)< VFB)
      ID =
(`P_Q*Nd*mu*Per/L)*((para)*(TS+epsS/COX)+(2.0/3.0)*sqrt(2*epsS/(`P_Q*Nd
))*(pow((pow(KA,2)-(VG-VS-delVg)+VFB),(3.0/2.0))-pow((pow(KA,2)-(VG-VS-
delVg)+VFB+(para)),(3.0/2.0))));
 else
      ID = (COX*(VG-VS-delVg-
VFB)*mu*para*Per/L)+(`P_Q*Nd*mu*Per/L)*((para)*(TS+epsS/COX)+(2.0/3.0)*
sqrt(2*epsS/(`P_Q*Nd))*(pow((pow(KA,2)),(3.0/2.0))-
pow((pow(KA,2)+(para)),(3.0/2.0))));
// Assign to I
 //
 I(d,s) <+ ID;

end // analog
 endmodule
```

REFERENCES

[1] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Second. Cambridge, UK: Cambridge University Press, 2009.

[2] J. L. Hudgins, G. S. Simin, E. Santi, and M. A. Khan, "An assessment of wide bandgap semiconductors for power devices," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 907–914, 2003.

[3] K. Ghosh and U. Singisetti, "Impact Ionization in Monoclinic β-Ga_2O_3," *arXiv Prepr. arXiv ...*, no. 1705.09203v1, pp. 1–5, 2017.

[4] M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Gallium oxide (Ga_2O_3) metal-semiconductor field-effect transistors on single-crystal β-Ga_2O_3 (010) substrates," *Appl. Phys. Lett.*, vol. 100, no. 1, pp. 1–4, 2012.

[5] R. K. Williams, M. N. Darwish, T. J. Letavic, and M. Ostling, "Power Devices and ICs," in *Guide to state-of-the-art electron devices*, J. N. Burghartz, Ed. West Sussex, UK: Wiley-Blackwell, 2013, pp. 203–212.

[6] IHS Markit Press Release, "Power semiconductor market revenues decline," *Solid State Technology*, p. 1, 2016.

[7] Markets and Markets, "RF Power Semiconductor Market - Global Forecast to 2022 (Press Release)," 2016. [Online]. Available: http://marketsandmarkets.com. [Accessed: 10-Mar-2017].

[8] B. J. Baliga, "Power Semiconductor Device Figure of Merit for High-Frequency Applications," *IEEE Electron Device Lett.*, vol. 10, no. 10, pp. 455–457, 1989.

[9] MACOM, "GaN Wideband Transistor," *MAGX-011086*, 2011.

[10] Microsemi, "GaN on SiC Wideband Transistor," *DC35GN-15-Q4*.

[11] Mitsubishi, "MOSFET Module: High Power Switching Use Insulated Package," *FM200TU-3A*.

[12] Fairchild Semiconductor, "F1 Module solution for PV-Application," *FPF1C2P5BF07A*, 2014.

[13] Infineon, "IGBT: Low Loss DuoPack: IGBT in TRENCHSTOP and Fieldstop Technology with soft, fast recovery antiparallel Emitter Controlled diode," *IKQ100N60TA*.

[14] E. Johnson, "Physical limitations on frequency and power parameters of transistors," *IRE Int. Conv. Rec.*, vol. 13, pp. 27–34, 1966.

[15] L. de Boisbaudran, "On the chemical and spectroscopic characters of a new metal (gallium)," *Philosophical Magazine Series 4*, vol. 50, no. 332, London, pp. 414–416, Nov-1875.

[16] A. E. Romanov, S. I. Stepanov, V. I. Nikolaev, and V. E. Bougrov, "GALLIUM

OXIDE: PROPERTIES AND APPLICATIONS - A REVIEW," *Rev. Adv. Mater. Sci*, vol. 44, pp. 63–86, 2016.
[17] M. Bartic, C.I. Baban, H. Suzuki, M. Ogita, and M. Isai, "β-Gallium Oxide as Oxygen Gas Sensors at a High Temperature," *J. Am. Ceram. Soc.*, vol. 90, no. 9, pp. 2879–2884, 2007.
[18] R. Suzuki, S. Nakagomi, and Y. Kokubun, "Solar-blind photodiodes composed of a Au Schottky contact and a β-Ga_2O_3 single crystal with a high resistivity cap layer," *Appl. Phys. Lett.*, vol. 98, no. 13, pp. 8–11, 2011.
[19] K. Matsuzaki, H. Hiramatsu, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, "Growth, structure and carrier transport properties of Ga_2O_3 epitaxial film examined for transparent field-effect transistor," *Thin Solid Films*, vol. 496, no. 1, pp. 37–41, 2006.
[20] M. Grundmann, H. Frenzel, A. Lajn, M. Lorenz, F. Schein, and H. Von Wenckstern, "Transparent semiconducting oxides: Materials and devices," *Phys. Status Solidi Appl. Mater. Sci.*, vol. 207, no. 6, pp. 1437–1449, 2010.
[21] M. Zinkevich and F. Aldinger, "Thermodynamic Assessment of the Gallium-Oxygen System," *J. Am. Ceram. Soc.*, vol. 87, no. 4, pp. 683–691, 2001.
[22] H. He, R. Orlando, M. A. Blanco, R. Pandey, E. Amzallag, I. Baraille, and M. Rérat, "First-principles study of the structural, electronic, and optical properties of Ga_2O_3 in its monoclinic and hexagonal phases," *Phys. Rev. B*, vol. 74, no. 195123, pp. 1–8, 2006.
[23] R. Roy, V. G. Hill, and E. F. Osborn, "Polymorphism of Ga_2O_3 and the System Ga_2O_3—H_2O," *J. Am. Chem. Soc.*, vol. 74, no. 3, pp. 719–722, Feb. 1952.
[24] F. Boschi, M. Bosi, T. Berzina, E. Buffagni, C. Ferrari, and R. Fornari, "Hetero-epitaxy of ε-Ga2O3 layers by MOCVD and ALD," *J. Cryst. Growth*, vol. 443, pp. 25–30, 2016.
[25] Y. Oshima, E. G. Víllora, Y. Matsushita, S. Yamamoto, and K. Shimamura, "Epitaxial growth of phase-pure ε -Ga_2O_3 by halide vapor phase epitaxy," Journal of Applied Physics, vol. 118, no. 08531, pp. 1-5, 2016.
[26] Y. Oshima, E. G. Víllora, and K. Shimamura, "Halide vapor phase epitaxy of twin-free α-Ga_2O_3 on sapphire (0001) substrates," *Appl. Phys. Express*, vol. 8, no. 5, p. 55501, 2015.
[27] G. T. Dang, T. Kawaharamura, M. Furuta, and M. W. Allen, "Mist-CVD Grown Sn-Doped α-Ga_2O_3 MESFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3640–3644, 2015.
[28] R. Huang, H. Hayashi, F. Oba, and I. Tanaka, "Microstructure of Mn-doped γ-Ga_2O_3 epitaxial film on sapphire (0001) with room temperature ferromagnetism," *J. Appl. Phys.*, vol. 101, no. 63526, pp. 1–7, 2007.
[29] H. Y. Playford, A. C. Hannon, E. R. Barney, and R. I. Walton, "Structures of uncharacterised polymorphs of gallium oxide from total neutron diffraction," *Chem. - A Eur. J.*, vol. 19, no. 8, pp. 2803–2813, 2013.
[30] M. Marezio and J. P. Remeika, "Bond Lengths in the α−Ga_2O_3 Structure and the High-Pressure Phase of $Ga_{2-x}Fe_xO_3$," *J. Chem. Phys.*, vol. 46, no. 5, pp. 1862–1865, 1967.

[31] D. Shinohara and S. Fujita, "Heteroepitaxy of Corundum-Structured α-Ga_2O_3 Thin Films on α-Al_2O_3 Substrates by Ultrasonic Mist Chemical Vapor Deposition," *Jpn. J. Appl. Phys.*, vol. 47, no. 9, pp. 7311–7313, 2008.
[32] J. Ahman, G. Svensson, and J. Albertsson, "A Reinvestigation of β-Gallium Oxide," *Acta Cryst.*, vol. 52, no. C, pp. 1336–1338, 1996.
[33] A. Taylor and D. S. Laidler, "The Formation and Crystal Structure of Silicon Carbide," *Br. J. Appl. Phys.*, vol. 1, pp. 174–181, 1950.
[34] W. Paszkowicz, S. Podsiadło, and R. Minikayev, "Rietveld-refinement study of aluminium and gallium nitrides," *J. Alloys Compd.*, vol. 382, no. 1–2, pp. 100–106, 2004.
[35] J. S. Blakemore, "Semiconducting and other major properties of gallium arsenide," *J. Appl. Phys.*, vol. 53, no. 10, 1982.
[36] C. P. Herrero, "The isotopic mass and lattice parameter of diamond; a path-integral simulation," *J. Phys. Condens. Matter*, vol. 13, no. 22, pp. 5127–5134, 2001.
[37] J. . A. Kohn, G. Katz, and J. D. Broder, "Characterization of β-Ga_2O_3 and its alumina isomorph, θ-Al_2O_3," *Am. Mineral.*, vol. 42, no. 5, pp. 398–407, 1957.
[38] S. Geller, "Crystal Structure of β-Ga_2O_3," *J. Chem. Phys.*, vol. 33, no. 3, pp. 676–684, 1960.
[39] K. Momma and F. Izumi, "VESTA 3 for three-dimensional visualization of crystal, volumetric and morphology data," *J. Appl. Crystallogr.*, vol. 44, no. 6, pp. 1272–1276, Oct. 2011.
[40] M. Mohamed, C. Janowitz, I. Unger, R. Manzke, Z. Galazka, R. Uecker, R. Fornari, J. R. Weber, J. B. Varley, and C. G. Van De Walle, "The electronic structure of β-Ga_2O_3," *Appl. Phys. Lett.*, vol. 97, no. 21, pp. 1–4, 2010.
[41] C. Janowitz, V. Scherer, M. Mohamed, A. Krapf, H. Dwelk, R. Manzke, Z. Galazka, R. Uecker, K. Irmscher, R. Fornari, M. Michling, D. Schmeißer, J. R. Weber, J. B. Varley, and C. G. Van De Walle, "Experimental electronic structure of In_2O_3 and Ga_2O_3," *New J. Phys.*, vol. 13, no. 85014, pp. 1–14, 2011.
[42] G.L. Li, F. Zhang, Y.T. Cui, H. Oji, J.Y. Son, and Q. Guo, "Electronic structure of β-Ga_2O_3 single crystals investigated by hard X-ray photoelectron spectroscopy," *Appl. Phys. Lett.*, vol. 107, no. 2, p. 22109, 2015.
[43] J. B. Varley, J. R. Weber, A. Janotti, and C. G. Van De Walle, "Oxygen vacancies and donor impurities in β-Ga_2O_3," *Appl. Phys. Lett.*, vol. 97, no. 14, pp. 10–13, 2010.
[44] K. Ghosh and U. Singisetti, "Ab initio Study of High-field Transport in Low Symmetry Crystals- Velocity-Field Curves in Monoclinic β-Ga_2O_3," *arXiv Prepr. arXiv ...*, pp. 1–14, 2016.
[45] M. D. Santia, N. Tandon, and J. D. Albrecht, "Lattice thermal conductivity in β-Ga_2O_3 from first principles," *Appl. Phys. Lett.*, vol. 107, no. 4, p. 41907, 2015.
[46] Z. Guo, A. Verma, X. Wu, F. Sun, A. Hickman, T. Masui, A. Kuramata, M. Higashiwaki, D. Jena, and T. Luo, "Anisotropic thermal conductivity in single crystal β -gallium oxide," *Appl. Phys. Lett.*, vol. 106, no. 111909, pp. 1–6, 2015.
[47] K. Sasaki, A. Kuramata, T. Masui, E. G. Víllora, K. Shimamura, S. Yamakoshi, and E. G. Villora, "Device-Quality β-Ga_2O_3 Epitaxial Films Fabricated by Ozone

Molecular Beam Epitaxy," *Appl. Phys. Express*, vol. 5, no. 3, p. 35502, 2012.
[48] K. Ghosh and U. Singisetti, "Ab initio calculation of electron – phonon coupling in monoclinic β-Ga_2O_3 crystal," *Appl. Phys. Lett.*, vol. 109, no. 72102, pp. 1–5, 2016.
[49] N. Ma, N. Tanen, A. Verma, Z. Guo, T. Luo, H. G. Xing, and D. Jena, "Intrinsic electron mobility limits in β-Ga_2O_3," *Appl. Phys. Lett.*, vol. 109, no. 212101, pp. 1–6, 2016.
[50] T. Oishi, Y. Koga, K. Harada, and M. Kasu, "High-mobility β-Ga_2O_3 (-201) single crystals grown by edge-defined film-fed growth method and their Schottky barrier diodes with Ni contact," *Appl. Phys. Express*, vol. 8, no. 3, p. 31101, 2015.
[51] N. Ueda, H. Hosono, R. Waseda, and H. Kawazoe, "Anisotropy of electrical and optical properties in β-Ga_2O_3 single crystals," *Appl. Phys. Lett.*, vol. 71, no. 7, pp. 933–935, 1997.
[52] K. Irmscher, Z. Galazka, M. Pietsch, R. Uecker, and R. Fornari, "Electrical properties of β-Ga_2O_3 single crystals grown by the Czochralski method," *J. Appl. Phys.*, vol. 110, no. 6, 2011.
[53] E. G. Villora, K. Shimamura, Y. Yoshikawa, K. Aoki, and N. Ichinose, "Large-size β-Ga_2O_3 single crystals and wafers," *J. Cryst. Growth*, vol. 270, no. 3–4, pp. 420–426, 2004.
[54] A. Parisini and R. Fornari, "Analysis of the scattering mechanisms controlling electron mobility in β-Ga_2O_3 crystals," *Semicond. Sci. Technol.*, vol. 31, no. 35023, pp. 1–13, 2016.
[55] Z. Galazka, R. Uecker, K. Irmscher, M. Albrecht, D. Klimm, M. Pietsch, M. Brützam, R. Bertram, S. Ganschow, and R. Fornari, "Czochralski growth and characterization of β-Ga_2O_3 single crystals," *Cryst. Res. Technol.*, vol. 45, no. 12, pp. 1229–1236, Dec. 2010.
[56] K. Irmscher, Z. Galazka, M. Pietsch, R. Uecker, and R. Fornari, "Electrical properties of β-Ga_2O_3 single crystals grown by the Czochralski method," *J. Appl. Phys.*, vol. 110, no. 6, 2011.
[57] W. S. Hwang, A. Verma, H. Peelaers, V. Protasenko, S. Rouvimov, H. G. Xing, A. Seabaugh, W. Haensch, C. Van De Walle, Z. Galazka, M. Albrecht, R. Fornari, and D. Jena, "High-voltage field effect transistors with wide-bandgap β-Ga_2O_3 nanomembranes," vol. 104, no. 203111, pp. 1–6, 2014.
[58] K. Ghosh and U. Singisetti, "*Ab initio* velocity-field curves in monoclinic β-Ga_2O_3," *J. Appl. Phys.*, vol. 122, no. 3, p. 35702, 2017.
[59] H. Aida, K. Nishiguchi, H. Takeda, N. Aota, K. Sunakawa, and Y. Yaguchi, "Growth of β-Ga_2O_3 single crystals by the edge-defined, film fed growth method," *Jpn. J. Appl. Phys.*, vol. 47, no. 11, pp. 8506–8509, 2008.
[60] Z. Galazka, K. Irmscher, R. Uecker, R. Bertram, M. Pietsch, A. Kwasniewski, M. Naumann, T. Schulz, R. Schewski, D. Klimm, and M. Bickermann, "On the bulk β-Ga_2O_3 single crystals grown by the Czochralski method," *J. Cryst. Growth*, vol. 404, pp. 184–191, 2014.
[61] M. Higashiwaki, K. Sasaki, H. Murakami, Y. Kumagai, A. Koukitu, A. Kuramata, T. Masui, and S. Yamakoshi, "Recent progress in Ga_2O_3 power devices," *Semicond. Sci. Technol.*, vol. 31, no. 3, p. 34001, 2016.

[62] M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Anomalous Fe diffusion in Si-ion-implanted β-Ga_2O_3 and its suppression in Ga_2O_3 transistor structures through highly resistive buffer layers," *Appl. Phys. Lett.*, vol. 106, no. 3, 2015.
[63] N. Ueda, H. Hosono, R. Waseda, and H. Kawazoe, "Synthesis and control of conductivity of ultraviolet transmitting β-Ga_2O_3 single crystals," *Appl. Phys. Lett.*, vol. 70, no. 26, p. 3561, 1997.
[64] E. G. Villora, K. Shimamura, Y. Yoshikawa, T. Ujiie, and K. Aoki, "Electrical conductivity and carrier concentration control in β-Ga_2O_3 by Si doping," *Appl. Phys. Lett.*, vol. 92, no. 20, pp. 174–177, 2008.
[65] T. Onuma, S. Fujioka, T. Yamaguchi, M. Higashiwaki, K. Sasaki, T. Masui, and T. Honda, "Correlation between blue luminescence intensity and resistivity in β-Ga_2O_3 single crystals," *Appl. Phys. Lett.*, vol. 103, no. 4, pp. 174–177, 2013.
[66] G. Wagner, M. Baldini, D. Gogova, M. Schmidbauer, R. Schewski, M. Albrecht, Z. Galazka, D. Klimm, and R. Fornari, "Homoepitaxial growth of β-Ga_2O_3 layers by metal-organic vapor phase epitaxy," *Phys. Stat. Sol.*, vol. 211, no. 1, pp. 27–33, 2014.
[67] S. Rafique, L. Han, M. J. Tadjer, J. A. Frietas Jr, N. A. Mahadik, and H. Zhao, "Homoepitaxial growth of β-Ga_2O_3 thin films by low pressure chemical vapor deposition," *Appl. Phys. Lett.*, vol. 108, no. 182105, pp. 3–8, 2016.
[68] V. I. Nikolaev, A. I. Pechnikov, S. I. Stepanov, I. P. Nikitina, A. N. Smirnov, A. V. Chikiryaka, S. S. Sharofidinov, V. E. Bougrov, and A. E. Romanov, "Epitaxial growth of (-201) β-Ga_2O_3 on (0001) sapphire substrates by halide vapour phase epitaxy," *Mater. Sci. Semicond. Process.*, vol. 47, pp. 16–19, 2016.
[69] M. Orita, H. Ohta, M. Hirano, and H. Hosono, "Deep-ultraviolet transparent conductive β-Ga_2O_3 thin films," *Appl. Phys. Lett.*, vol. 77, no. 25, pp. 4166–4168, 2000.
[70] D. J. Comstock and J. W. Elam, "Atomic Layer Deposition of Ga_2O_3 Films Using Trimethylgallium and Ozone," *Chem. Mater.*, vol. 24, p. 4011, 2012.
[71] T. Kuech, *Handbook of Crystal Growth : Handbook of Crystal Growth : Thin Films and Epitaxy (2)*, 2nd ed. Amsterdam, NL: Elsevier, 2014.
[72] J. R. Arthur, "Molecular beam epitaxy," *Surf. Sci.*, vol. 500, pp. 189–217, 2002.
[73] S. Krishnamoorthy, Z. Xia, S. Bajaj, M. Brenner, and S. Rajan, "Delta- doped β - Gallium Oxide Field Effect Transistor," *arXiv Prepr. arXiv ...*, 2017.
[74] E. Ahmadi, O. S. Koksaldi, S. W. Kaun, Y. Oshima, D. B. Short, K. Umesh, and J. S. Speck, "Ge doping of β-Ga_2O_3 films grown by plasma-assisted molecular beam epitaxy," *Appl. Phys. Exp.*, vol. 10, no. 4, pp. 041102, 2017.
[75] M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Field-Plated Ga_2O_3 MOSFETs With a Breakdown Voltage of Over 750 V," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 212-215, 2016.
[76] M. Baldini, M. Albrecht, A. Fiedler, K. Irmscher, R. Schewski, and G. Wagner, "Editors' Choice—Si- and Sn-Doped Homoepitaxial β-Ga_2O_3 Layers Grown by MOVPE on (010)-Oriented Substrates," *ECS J. Solid State Sci. Technol.*, vol. 6, no. 2, pp. Q3040–Q3044, 2017.

[77] M. Baldini, M. Albrecht, A. Fiedler, K. Irmscher, D. Klimm, R. Schewski, and G. Wagner, "Semiconducting Sn-doped β-Ga_2O_3 homoepitaxial layers grown by metal organic vapour-phase epitaxy," *J. Mater. Sci.*, vol. 51, no. 7, pp. 3650–3656, 2016.
[78] F. Zhang, K. Saito, T. Tanaka, M. Nishio, and Q. Guo, "Electrical properties of Si doped Ga_2O_3 films grown by pulsed laser deposition," *J. Mater. Sci. Mater. Electron.*, vol. 26, no. 12, pp. 9624–9629, 2015.
[79] F. Zhang, M. Arita, X. Wang, Z. Chen, K. Saito, T. Tanaka, M. Nishio, T. Motooka, and Q. Guo, "Toward controlling the carrier density of Si doped Ga_2O_3 films by pulsed laser deposition," *Appl. Phys. Lett.*, vol. 109, no. 102105, pp. 1–5, 2016.
[80] K. Sasaki, M. Higashiwaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Si-Ion implantation doping in β-Ga_2O_3 and its application to fabrication of low-resistance ohmic contacts," *Appl. Phys. Express*, vol. 6, no. 8, 2013.
[81] N. Moser, J. McCandless, A. Crespo, K. Leedy, A. Green, A. Neal, S. Mou, E. Ahmadi, J. Speck, K. Chabak, N. Peixoto, and G. Jessen, "Ge-doped β-Ga_2O_3 MOSFETs," *IEEE Electron Device Lett.*, vol. 38, no. 6, 2017.
[82] M. Higashiwaki, K. Sasaki, T. Kamimura, M. Hoi Wong, D. Krishnamurthy, A. Kuramata, T. Masui, and S. Yamakoshi, "Depletion-mode Ga_2O_3 metal-oxide-semiconductor field-effect transistors on β-Ga_2O_3 (010) substrates and temperature dependence of their device characteristics," *Appl. Phys. Lett.*, vol. 103, no. 12, pp. 1–5, 2013.
[83] Y. Kang, K. Krishnaswamy, H. Peelaers, and C. G. Van De Walle, "Fundamental limits on the electron mobility of β-Ga_2O_3," *J. physics. Condens. matter*, vol. 29, p. 234001, 2017.
[84] M. Passlack, N. E. J. Hunt, E. F. Schubert, G. J. Zydzik, M. Hong, J. P. Mannaerts, R. L. Opila, and R. J. Fischer, "Dielectric properties of electron-beam deposited Ga_2O_3 films," *Appl. Phys. Lett.*, vol. 64, no. 20, p. 2715, 1994.
[85] M. Ostling, "High power devices in wide bandgap semiconductors," *Sci. China Inf. Sci.*, vol. 54, no. 5, pp. 1087–1093, 2011.
[86] K. Takahashi, A. Yoshikawa, and A. Sandhu, *Wide Bandgap Semiconductors: Fundamental Properties and Modern Photonic and Electronic Devices*. Berlin: Springer-Verlag Berlin Heidelberg, 2007.
[87] L. Reggiani, S. Bosi, C. Canali, F. Nava, and S. F. Kozlov, "Hole-drift velocity in natural diamond," *Phys. Rev. B*, vol. 23, no. 6, pp. 3050–3057, 1981.
[88] P. C. Chang, Z. Fan, W. Y. Tseng, A. Rajagopal, and J. G. Lu, "β-Ga_2O_3 nanowires: Synthesis, characterization, and p-channel field-effect transistor," *Appl. Phys. Lett.*, vol. 87, no. 22, pp. 1–3, 2005.
[89] K. Matsuzaki, H. Yanagi, T. Kamiya, H. Hiramatsu, K. Nomura, M. Hirano, and H. Hosono, "Field-induced current modulation in epitaxial film of deep-ultraviolet transparent oxide semiconductor Ga_2O_3," *Appl. Phys. Lett.*, vol. 88, no. 9, pp. 8–11, 2006.
[90] W. Hwang, A. Verma, and H. Peelaers, "High-Voltage Field Effect Transistors with Wide-Bandgap β-Ga_2O_3 Nanomembranes," *arXiv Prepr. arXiv ...*, pp. 1–16,

2013.
[91] H. Zhou, M. Si, S. Alghamdi, G. Qiu, L. Yang, and P. D. Ye, "High Performance Depletion / Enhancement- Mode β-Ga_2O_3 on Insulator (GOOI) Field-effect Transistors with Record Drain Currents of 600 / 450 mA / mm," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 103-106, 2016.
[92] A. J. Green, K. D. Chabak, E. R. Heller, R. C. Fitch, M. Baldini, A. Fiedler, K. Irmscher, G. Wagner, Z. Galazka, S. E. Tetlak, A. Crespo, K. Leedy, and G. H. Jessen, "3.8-MV / cm Breakdown Strength of MOVPE-Grown Sn-Doped β-Ga_2O_3 MOSFETs," *IEEE Electron Device Lett.*, vol. 37, no. 7, pp. 902–905, 2016.
[93] K. Sasaki, M. Higashiwaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Ga_2O_3 Schottky Barrier Diodes Fabricated by Using Single-Crystal β-Ga_2O_3 (010) Substrates," *IEEE Electron Device Lett.*, vol. 34, no. 4, pp. 493–495, 2013.
[94] M. Mohamed, K. Irmscher, C. Janowitz, Z. Galazka, R. Manzke, and R. Fornari, "Schottky barrier height of Au on the transparent semiconducting oxide β-Ga_2O_3," *Appl. Phys. Lett.*, vol. 101, no. 13, pp. 3–8, 2012.
[95] S. Müller, H. von Wenckstern, F. Schmidt, D. Splith, F.-L. Schein, H. Frenzel, and M. Grundmann, "Comparison of Schottky contacts on β-gallium oxide thin films and bulk crystals," *Appl. Phys. Express*, vol. 8, no. 12, p. 121102, 2015.
[96] T. Oshima, R. Wakabayashi, M. Hattori, A. Hashiguchi, N. Kawano, K. Sasaki, T. Masui, A. Kuramata, S. Yamakoshi, K. Yoshimatsu, A. Ohtomo, T. Oishi, and M. Kasu, "Formation of indium – tin oxide ohmic contacts for β-Ga_2O_3," *Jpn. J. Appl. Phys.*, vol. 55, no. 1202B7, pp. 1–3, 2016.
[97] T. Kamimura, K. Sasaki, M. Hoi Wong, D. Krishnamurthy, A. Kuramata, T. Masui, S. Yamakoshi, and M. Higashiwaki, "Band alignment and electrical properties of Al_2O_3/β-Ga_2O_3 heterojunctions," *Appl. Phys. Lett.*, vol. 104, no. 19, pp. 1–6, 2014.
[98] Y. Jia, K. Zeng, J. S. Wallace, J. A. Gardella, and U. Singisetti, "Spectroscopic and electrical calculation of band alignment between atomic layer deposited SiO_2 and β-Ga_2O_3 (-201)," *Appl. Phys. Letters*, vol. 106, no. 102107, pp. 2–5, 2015.
[99] T. Kamimura, D. Krishnamurthy, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Epitaxially grown crystalline Al_2O_3 interlayer on β-Ga_2O_3 (010) and its suppressed interface state density," *Jpn. J. Appl. Phys.*, vol. 55, no. 1202B5, pp. 1–7, 2016.
[100] J. Kim, M. A. Mastro, M. J. Tadjer, and J. Kim, "Quasi-Two-Dimensional h-BN/β-Ga_2O_3 Heterostructure Metal–Insulator–Semiconductor Field-Effect Transistor," *ACS Appl. Mater. Interfaces*, vol. 9, no. 25, pp. 21322–21327, Jun. 2017.
[101] P. H. Carey, F. Ren, D. C. Hays, B. P. Gila, S. J. Pearton, S. Jang, and A. Kuramata, "Band alignment of atomic layer deposited SiO_2 and $HfSiO_4$ with (-201) β-Ga_2O_3," *Jpn. J. Appl. Phys.*, vol. 56, no. 7, p. 71101, Jul. 2017.
[102] M. Houssa and M. M. Heyns, "High-k Gate Dielectrics," in *High k Gate Dielectrics*, Taylor & Francis, 2010.
[103] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 18,

no. 3, p. 1785, 2000.
[104] V. D. Wheeler, D. I. Shahin, M. J. Tadjer, and C. R. Eddy, “Band Alignments of Atomic Layer Deposited ZrO_2 and HfO_2 High-k Dielectrics with (-201) β-Ga_2O_3,” *ECS J. Solid State Sci. Technol.*, vol. 6, no. 2, pp. Q3052–Q3055, Dec. 2017.
[105] C. R. Dean, A. F. Young, I. Meric, C. Lee, L. Wang, S. Sorgenfrei, K. Watanabe, T. Taniguchi, P. Kim, K. L. Shepard, and J. Hone, “Boron nitride substrates for high quality graphene electronics," *Nature Nanotechnology*, Vol. 5, pp. 722-726, 2010.
[106] P. H. Carey, F. Ren, D. C. Hays, B. P. Gila, S. J. Pearton, S. Jang, and A. Kuramata, “Conduction and valence band offsets of $LaAl_2O_3$ with (−201) β-Ga_2O_3,” *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.*, vol. 35, no. 4, p. 41201, Jul. 2017.
[107] T. J. Anderson, V. D. Wheeler, D. I. Shahin, M. J. Tadjer, L. E. Luna, A. D. Koehler, K. D. Hobart, F. J. Kub, and C. R. Eddy, “Normally-Off AlGaN/GaN Mos-Hemts Using ZrO_2 Gate Dielectric with Tuneable Charge,” *ECS Meet. Abstr.*, no. MA2017-01, May 29, 2017.
[108] H. D. Sunitha and N. Keshaveni, “Reduced Surface Field Technology For LDMOS : A Review,” *Int. J. Emerg. Technol. Adv. Eng.*, vol. 4, no. 6, pp. 173–176, 2014.
[109] P. Moens, F. Bogman, H. Ziad, H. De Vleeschouwer, M. Tack, G. Loechelt, G. Grivna, J. Parsey, Y. Wu, T. Quddus, and P. Zdebel, “A Local Charge-Balanced Trench-Based 600 V Super-Junction Device,” in *Proceedings of the 23rd International Symposium on Power Semiconductor Devices & IC’s*, 2011, pp. 304–307.
[110] T. Nakamura, Y. Nakano, M. Aketa, R. Nakamura, S. Mitani, H. Sakairi, and Y. Yokotsuji, “High performance SiC trench devices with ultra-low R_{ON},” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, no. 75, pp. 599–601, 2011.
[111] E. Bahat-Treidel, F. Brunner, O. Hilt, E. Cho, J. Würfl, and G. Trankle, “AlGaN/GaN/GaN:C back-barrier HFETs with breakdown voltage of over 1 kV and low RON × A,” *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 3050–3058, 2010.
[112] E. Bahat-Treidel, O. Hilt, R. Zhytnytska, A. Wentzel, C. Meliani, J. Wurfl, and G. Trankle, “Fast-switching GaN-based lateral power schottky barrier diodes with low onset voltage and strong reverse blocking,” *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 357–359, 2012.
[113] H. S. Lee, D. Piedra, M. Sun, X. Gao, S. Guo, and T. Palacios, “3000-V 4.3-mΩ ċ cm 2 InAlN/GaN MOSHEMTs with AlGaN back barrier,” *IEEE Electron Device Lett.*, vol. 33, no. 7, pp. 982–984, 2012.
[114] I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Bour, T. Prunty, and D. Disney, “3.7 kV Vertical GaN PN Diodes,” vol. 35, no. 2, pp. 247-249, 2014.
[115] C. Tsou, K. Wei, Y. Lian, and S. S. H. Hsu, “2.07-kV AlGaN/GaN Schottky Barrier Diodes on Silicon With High Baliga's Figure-of-Merit,” *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 70–73, 2016.
[116] I. Omura, “Power semiconductor device.” IEEE EDS, Kyushu Inst. Tech., pp. 1–7,

2015.
[117] A. W. Ludikhuize, “A Review of RESURF Technology,” in *ISPSO’2000*, 2000, pp. 11–18.
[118] N. Kaminski and O. Hilt, “SiC and GaN devices – wide bandgap is not all the same,” *IET Circuits, Devices Syst.*, vol. 8, no. 3, pp. 227–236, 2014.
[119] M. Sun, Y. Zhang, and T. Palacios, “Vertical GaN Transistors for the Next Generation of Power Electronics,” in *Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2016.
[120] Y. Gao, I. Ben-Yaacov, U. K. Mishra, and E. L. Hu, “Optimization of AlGaN/GaN current aperture vertical electron transistor (CAVET) fabricated by photoelectrochemical wet etching,” *J. Appl. Phys.*, vol. 96, no. 11, pp. 6925–6927, 2004.
[121] S. Chowdhury, B. L. Swenson, and Others, “Current status and scope of gallium nitride-based vertical transistors for high-power electronics application,” *Semicond. Sci. Technol.*, vol. 28, no. 7, p. 74014, 2013.
[122] A. Q. Huang, “New unipolar switching power device figures of merit,” *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 298–301, 2004.
[123] J. Strydom, “eGaN-Silicon Power Shoot-Out: Comparing Figure of Merit (FOM),” *Power Electron. Technol.*, pp. 23–30, September, 2010.
[124] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter, and Y. Kawaguchi, “The Trench Power MOSFET: Part I—History, Technology, and Prospects,” *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 674–691, 2017.
[125] G. Ghione, F. Bonani, R. Quay, and E. Kasper, “RF and Microwave Semiconductor Technologies,” in *Guide to state-of-the-art electron devices*, West Sussex, UK: Wiley-Blackwell, 2013, pp. 189–201.
[126] S. J. Cho, C. Wang, and N. Y. Kim, “High power density AlGaAs/InGaAs/GaAs PHEMTs using an optimised manufacturing process for Ka-band applications,” *Microelectron. Eng.*, vol. 113, pp. 11–19, 2014.
[127] M. Z. Peng, Y. K. Zheng, W. J. Luo, and X. Y. Liu, “14.2 W/mm internally-matched AlGaN/GaN HEMT for X-band applications,” *Solid. State. Electron.*, vol. 64, no. 1, pp. 63–66, 2011.
[128] K. Konishi, K. Goto, H. Murakami, Y. Kumagai, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, “1-kV vertical Ga_2O_3 field-plated Schottky barrier diodes,” *Appl. Phys. Lett.*, vol. 110, no. 10, p. 103506, 2017.
[129] M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, “Field-Plated Ga_2O_3 MOSFETs With a Breakdown Voltage of Over 750 V,” *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 212–215, 2016.
[130] K. D. Chabak, N. Moser, A. J. Green, D. E. Walker, S. E. Tetlak, E. Heller, A. Crespo, R. Fitch, J. P. McCandless, K. Leedy, M. Baldini, G. Wagner, Z. Galazka, X. Li, and G. Jessen, “Enhancement-mode Ga_2O_3 wrap-gate fin field-effect transistors on native (100) β- Ga_2O_3 substrate with high breakdown voltage,” *Appl. Phys. Lett.*, vol. 109, no. 21, pp. 2–5, 2016.
[131] P. Giannozzi, S. Baroni, N. Bonini, M. Calandra, R. Car, C. Cavazzoni, D. Ceresoli, G. L. Chiarotti, M. Cococcioni, I. Dabo, A. Dal Corso, S. de Gironcoli,

S. Fabris, G. Fratesi, R. Gebauer, U. Gerstmann, C. Gougoussis, A. Kokalj, M. Lazzeri, L. Martin-Samos, N. Marzari, F. Mauri, R. Mazzarello, S. Paolini, A. Pasquarello, L. Paulatto, C. Sbraccia, S. Scandolo, G. Sclauzero, A. P. Seitsonen, A. Smogunov, P. Umari, and R. M. Wentzcovitch, "QUANTUM ESPRESSO: a modular and open-source software project for quantum simulations of materials.," *J. Phys. Condens. Matter*, vol. 21, no. 39, p. 395502, 2009.

[132] "Atlas Simulation of a Wide Bandgap Ga_2O_3 MOSFET." [Online]. Available: http://www.silvaco.com/tech_lib_TCAD/simulationstandard/2013/oct_nov_dec/a2/oct_nov_dec2013_a2.pdf. [Accessed: 06-Oct-2016].

[133] M. H. Wong, Y. Morikawa, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Characterization of channel temperature in Ga_2O_3 metal-oxide-semiconductor field-effect transistors by electrical measurements and thermal modeling," *Appl. Phys. Lett.*, vol. 109, no. 193503, pp. 1–5, 2016.

[134] M. Pinto, R. K. Smith, and A. Alam, *Padre 2.4E Users Manual*. Bell Laboratories, 1994.

[135] W. R. Curtice and M. Ettenberg, "A Nonlinear GaAs FET Model for Use in the Design of Output Circuits for Power Amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 33, no. 12, pp. 1383–1394, 1985.

[136] Y. Tajima, B. Wrona, and K. Mishima, "GaAs FET large-signal model and its application to circuit designs," *IEEE Trans. Electron Devices*, pp. 171–175, 1981.

[137] I. Angelov, V. Desmaris, K. Dynefors, P. Å. Nilsson, N. Rorsman, and H. Zirath, "On the large-signal modelling of AlGaN / GaN HEMTs and SiC MESFETs," *Eur. Gall. Arsenide Other Semicond. Appl. Symp.*, pp. 309–312, 2005.

[138] Numerous, *Nonlinear Transistor Model Parameter Extraction Techniques*, 1st ed. Cambridge, UK: Cambridge University Press, 2012.

[139] Silvaco, "Device 3D: 3D Device Simulator." 2016.

[140] Silvaco, "Victory Process: 3D Process Simulator." 2016.

[141] Synopsys, "Sentaurus TCAD: Industry-Standard Process and Device Simulators," no. 1. pp. 1–203, 2012.

[142] C. S. Rafferty, K. Smith, Y. Liu, D. Kearney, and S. Clark, "Prophet." 2016.

[143] J. Watts, C. McAndrew, C. Enz, C. Galup-Montoro, G. Gildenblat, C. Hu, R. van Langevelde, M. Miura-Mattausch, R. Rios, and C. T. Sah, "Advanced compact models for MOSFETs," *Tech. Proc. Work. Compact Model.*, pp. 3–12, 2005.

[144] H. C. Pao and C. T. Sah, "Effects of diffusion current on characteristics of metal-oxide (insulator)-semiconductor transistors," *Solid. State. Electron.*, vol. 9, no. 10, pp. 927–937, 1966.

[145] S. Khandelwal, N. Goyal, and T. A. Fjeldly, "A physics-based analytical model for 2DEG charge density in AlGaN/GaN HEMT devices," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3622–3625, 2011.

[146] N. Dasgupta and A. Dasgupta, "A new spice mosfet level 3-like model of hemt's for circuit simulation," *IEEE Trans. Electron Devices*, vol. 45, no. 7, pp. 1494–1500, 1998.

[147] F. M. Yigletu, S. Khandelwal, T. A. Fjeldly, and B. Iniguez, "Compact charge-based physical models for current and capacitances in AlGaN/GaN hemts," *IEEE*

Trans. Electron Devices, vol. 60, no. 11, pp. 3746–3752, 2013.
[148] S. Khandelwal, S. Ghosh, Y. S. Chauhan, B. Iniguez, and T. A. Fjeldly, "Surface-Potential-Based RF Large Signal Model for Gallium Nitride HEMTs," *IEEE CSICS*, Oct. 2015.
[149] *Verilog-A Language Reference Manual: Analog Extensions to Verilog HDL*, 1.0. Open Verilog International, 1996.
[150] DesignSoft, *TINA v10 The Complete Electronics Lab for Windows: Users Manual*. 2014.
[151] J. H. Klootwijk and C. E. Timmering, "Merits and limitations of circular TLM structures for contact resistance determination for novel III-V HBTs," in *Proc. IEEE 2004 Int. Conference on Microelectronic Test Structures*, 2004, pp. 247–252.
[152] M. Passlack, N. E. J. Hunt, E. F. Schubert, G. J. Zydzik, M. Hong, J. P. Mannaerts, R. L. Opila, and R. J. Fischer, "Dielectric properties of e-beam deposited Ga_2O_3 films," *Applied Physics Letters*, 1994. [Online]. Available: https://ecse.rpi.edu/~schubert/Reprints/1994 Passlack et al (APL) Dielectric properties of e-beam deposited Ga2O3 films.pdf. [Accessed: 06-Oct-2016].
[153] M. H. Wong, Y. Nakata, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Enhancement-mode Ga_2O_3 MOSFETs with Si-ion-implanted source and drain," *Appl. Phys. Express*, vol. 10, no. 41101, pp. 1–3, 2017.
[154] J. Joh, J. A. Del Alamo, U. Chowdhury, T. M. Chou, H. Q. Tserng, and J. L. Jimenez, "Measurement of channel temperature in GaN high-electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2895–2901, 2009.
[155] E. Ahmadi, O. S. Koksaldi, S. W. Kaun, Y. Oshima, D. B. Short, U. K. Mishra, and J. S. Speck, "Ge doping of β- Ga_2O_3 films grown by plasma-assisted molecular beam epitaxy," *Appl. Phys. Express*, vol. 10, no. 4, p. 41102, Apr. 2017.
[156] H. Peelaers and C. G. Van de Walle, "Brillouin zone and band structure of β-Ga_2O_3," *Phys. Status Solidi Basic Res.*, vol. 252, no. 4, pp. 828–832, 2015.
[157] J. Furthmüller and F. Bechstedt, "Quasiparticle bands and spectra of Ga_2O_3 polymorphs," *Phys. Rev. B*, vol. 93, no. 115204, pp. 1–16, 2016.
[158] M. Higashiwaki, K. Sasaki, M. H. Wong, T. Kam, D. Krishnamurthy, A. Kuramata, and T. Masui, "Depletion-mode Ga_2O_3 MOSFETs on β- Ga_2O_3 (010) substrates with Si-ion-implanted channel and contacts," *2013 Int. Electron Devices Meet.*, vol. 3, no. 10, pp. 707–710, 2013.
[159] M. J. Casto and S. R. Dooley, "AlGaN/GaN HEMT temperature-dependent large-signal model thermal circuit extraction with verification through advanced thermal imaging," in *2009 IEEE 10th Annual Wireless and Microwave Technology Conference*, 2009, pp. 1–5.
[160] S. Martin-horcajo, A. Wang, M. Romero, M. J. Tadjer, and F. Calle, "Simple and Accurate Method to Estimate Channel Temperature and Thermal Resistance in AlGaN/GaN HEMTs," *Trans. Electron Devices*, vol. 60, no. 12, pp. 4105–4111, 2013.
[161] O. Jardel, F. De Groote, C. Charbonniaud, T. Reveyrand, J. P. Teyssier, R. Quéré, and D. Floriot, "A drain-lag model for AlGaN/GaN power HEMTs," *IEEE MTT-S*

Int. Microw. Symp. Dig., vol. 0, pp. 601–604, 2007.
[162] B. Lu and T. Palacios, "AlGan/Gan vertical Power transistors," Online report: http://www-mtl.mit.edu/research/annual_reports/2009/files/de/de_29.pdf, 2009.
[163] T. Mimura, S. Hiyamizu, T. Fujii, and K. Nanbu, "A New Field-Effect Transistor with Selectively Doped GaAs / n-Al_xGa_{1-x} As Heterojunctions," *Jpn. J. Appl. Phys.*, vol. 19, no. 5, pp. L225–L227, 1980.
[164] R. Dingle, H. L. Stormer, A. C. Gossard, and W. Wiegmann, "Electron mobilities in modulation-doped semiconductor heterojunction superlattices," *Appl. Phys. Lett.*, vol. 33, no. 7, pp. 665–667, 1978.
[165] S. W. Kaun, F. Wu, and J. S. Speck, "β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ (010) heterostructures grown on β-Ga_2O_3 (010) substrates by plasma-assisted molecular beam epitaxy," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 33, no. 4. p. 41508, 2015.
[166] E. Ahmadi, O. S. Koksaldi, X. Zheng, T. Mates, Y. Oshima, U. K. Mishra, and J. S. Speck, "Demonstration of β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ modulation doped field-effect transistors with Ge as dopant grown via plasma-assisted molecular beam epitaxy," *Appl. Phys. Express*, vol. 10, no. 7, p. 71101, Jul. 2017.
[167] S. Krishnamoorthy, Z. Xia, S. Bajaj, M. Brenner, and S. Rajan, "Delta-doped β-gallium oxide field-effect transistor," *Appl. Phys. Express*, vol. 10, no. 51102, pp. 1–4, 2017.
[168] S. Krishnamoorthy, Z. Xia, C. Joishi, Y. Zhang, J. McGlone, J. Johnson, M. Brenner, A. R. Arehart, J. Hwang, S. Lodha, and S. Rajan, "Modulation-doped β-$(Al_{0.2}Ga_{0.8})_2O_3/Ga_2O_3$ field-effect transistor," *Appl. Phys. Lett.*, vol. 111, no. 2, p. 23502, 2017.
[169] T. Oshima, Y. Kato, N. Kawano, A. Kuramata, S. Yamakoshi, S. Fujita, T. Oishi, and M. Kasu, "Carrier confinement observed at modulation-doped β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ heterojunction interface," *Appl. Phys. Express*, vol. 10, no. 3, p. 35701, 2017.

BIOGRAPHY

Neil Austin Moser graduated from Crestview High School, Convoy, Ohio, in 1998. He received his Bachelor of Science in Electrical Engineering from University of Michigan-Ann Arbor in 2002, Summa Cum Laude and his Master of Science in Electrical and Computer Engineering from George Mason University in 2013. From 2002 to 2009 he was an officer in the United States Air Force acting as a developmental engineer first at the Air Force Research Laboratory, Wright Patterson AFB, OH and then at the Launch and Range Systems Wing, Los Angeles, AFB, CA. After a one year position working as a contractor for Marine Corps Systems Command, Quantico, VA, he began federal civilian service as a technical intelligence officer in the Central Intelligance Agency in 2010 working first for the Advanced Systems and Technology Directorate, National Reconnaissance Office, Chantilly, VA and then for the Directorate of Science and Technology, Reston, VA. In 2014, Neil left federal civilian service to pursue his Doctorate of Philosophy full time at George Mason University through the award of a SMART Scholarship for Service from the Department of Defense.

Neil married his wife Morgan in 2011. In 2014, they welcomed their daughter Schaefer to the family. Neil's extended family still resides in the Convoy, Ohio area. Schaefer, Morgan, and Neil enjoying traveling and outdoor adventures such as snowboarding and beach volleyball.